

BGB741L7ESD and BGS12AL7

LNA and RF switch for mobile TV
Applications

Application Note AN206

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1 Product Description

1.1 BGB741L7ESD: Broadband MMIC Low Noise Amplifier

The MMIC LNA BGB741L7ESD from Infineon Technologies is a high performance broadband amplifier for wireless solutions.

Built up with Silicon Germanium: Carbon (SiGe: C) technology, the BGB741L7ESD offers an excellent noise figure over broad frequency band. The biasing and stabilization circuits built inside the BGB741L7ESD reduce the number of external parts down to 6 and make the BGB741L7ESD interesting for compact and high performance LNA designs.

The component can be used from 1.8V until 4.0V and from 5mA to 30mA.

Furthermore, this device includes an integrated ESD protection circuit on chip which protects the device upto 4.0kV at the input pin and 2.5kV at the output pin (according to Human Body Model). A CMOS-technology compliant power-on/off function is also integrated in the device.

The first figure presents the block diagram of the BGB741L7ESD. The device is packaged in TSLP-7-1 format and the pinning information is summarized in the table 1.

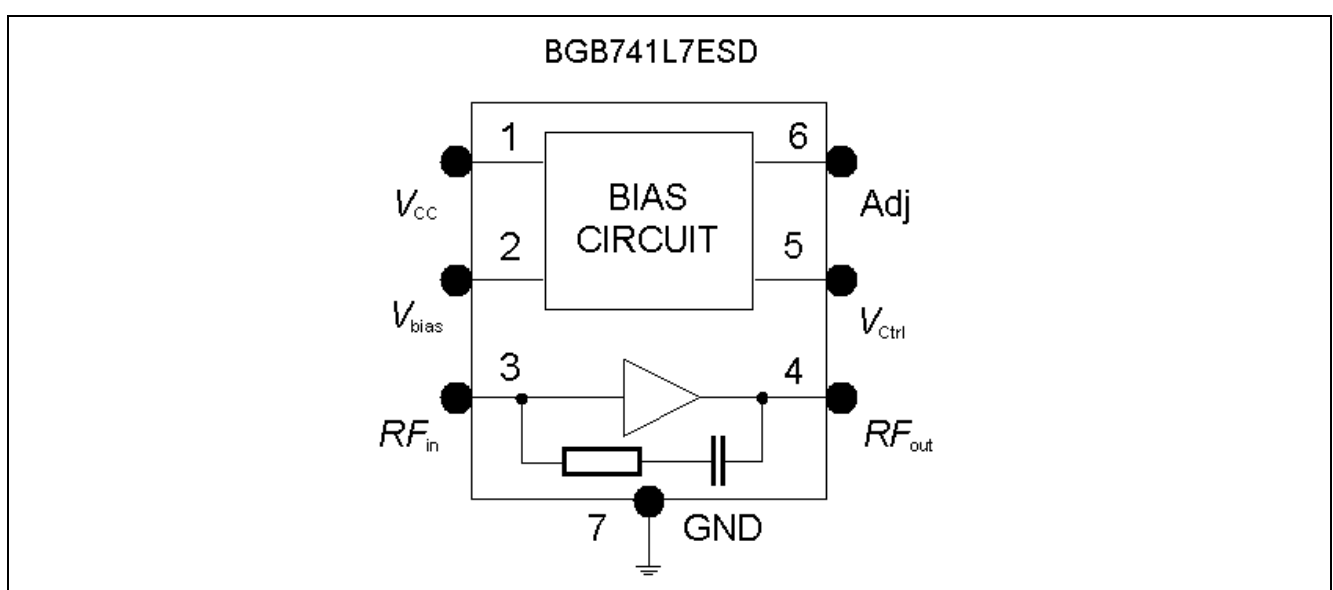


Figure 1 Block Diagram of the BGB741L7ESD.

Table 1 Pin definition and function

Pin N°	Name	Function
1	Vcc	Voltage supply
2	Vbias	Output of biasing circuitry to the transistor base
3	RFin	RF input of the BGB741L7ESD LNA
4	RFout	RF output of the LNA
5	Vctrl	Power off/on mode Function
6	Adj	Current adjustment
7	GND	Ground of the BGB741L7ESD

For more details please refer to the datasheet of the BGB741L7ESD available in the Infineon internet pages

1.2 SPDT RF Switch BGS12AL7-4

The BGS12AL7-4 General Purpose RF MOS switch is designed to cover a broad range of applications from 30 MHz to 3 GHz. The symmetric design of its single pole double throw configuration, as shown in Figure 2 offers high design flexibility. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. The 0.1 dB compression point exceeds the switch's maximum input power level of 21 dBm, resulting in linear performance at all signal levels. The RF switch has a very low insertion loss of 0.4 dB in the 1 GHz and 0.5 dB in the 2 GHz range.

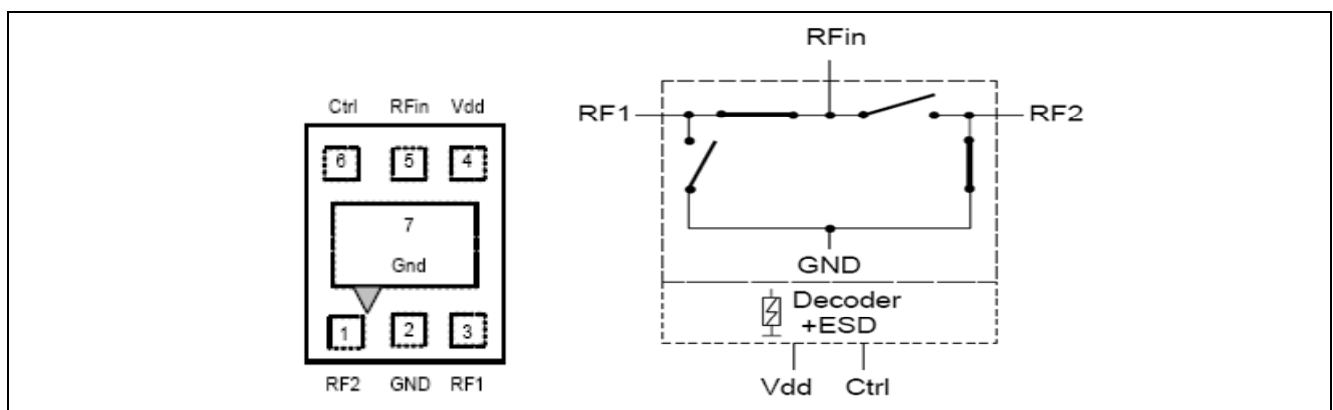


Figure 2 Functional and Pinout Diagram of BGS12AL7-4

In the table 2 the the pin names, corresponding with the pinout in figure 2 are described.

Table 2 Pin definition and function

Pin N°	Name	Function
1	RF2	RF Port 2 Out
2	GND	Ground
3	RF1	RF Port 1 Out
4	Vdd	Supply Voltage
5	RFin	RF Port In
6	Ctrl	Control Pin
7	GND	Ground

For more details please refer to the datasheet of the BGS12AL7-4 available in the Infineon internet pages

2 Application Information

This application note presents the BGB741L7ESD as LNA combined with the RF switch BGS12AL7-4 for mobile TV in the Frequency range 30 to 850 MHz. One typical application is the combined reception of TV and FM with one antenna and two separated receiver ICs.

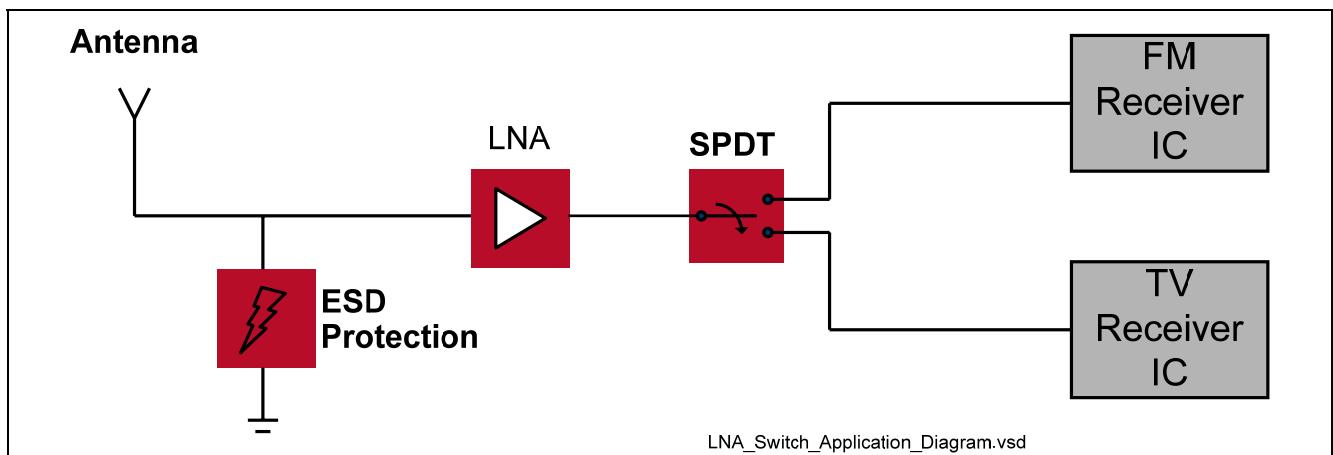


Figure 3 Block diagram of of TV and FM reception in mobile phone application.

Another application could be the reception of separated RX paths of analog and digital TV.

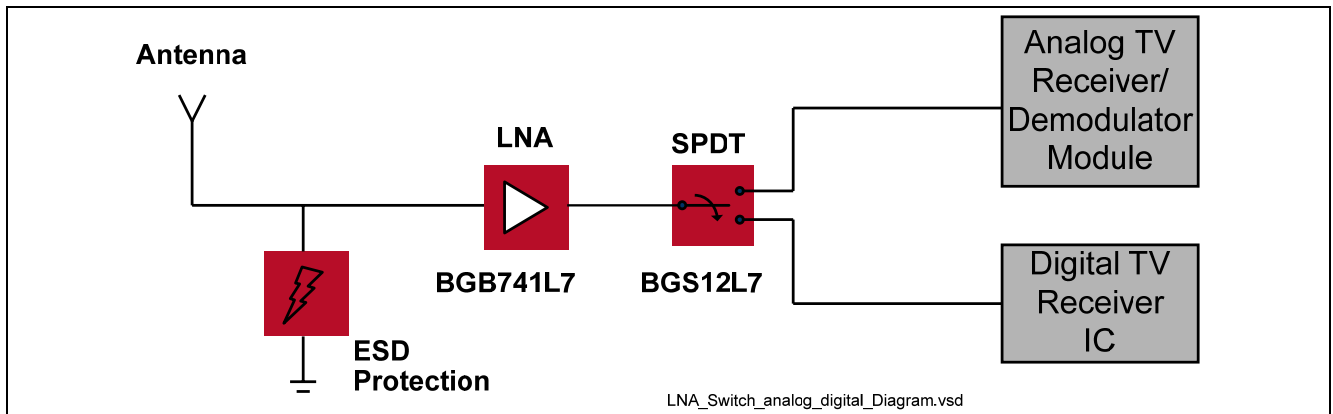


Figure 4 Block Diagram of an application for analog and digital TV

Both applications use an antenna with close to 50 Ohm impedance and the receiver also have 50 Ohm inputs.

3 BGB741L7ESD and BGS12AL7-4 Application Schematics

3.1 Evaluation boards BGB741L7

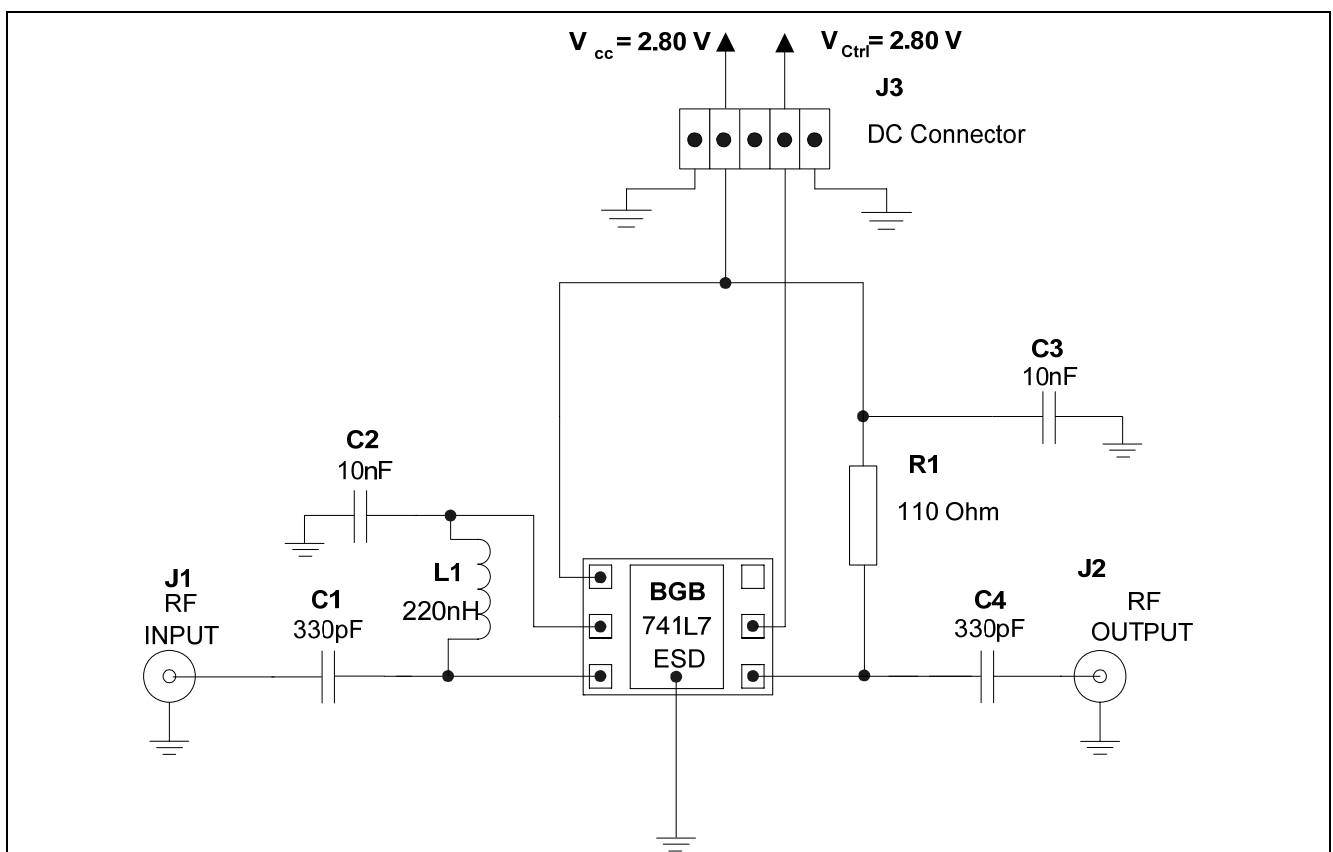


Figure 5 Schematics of the BGB741L7ESD application.

Table 3 Bill-of-Materials

Symbol	Value	Unit	Size	Manufacturer	Comment
C1	330	pF	0402	Various	DC block/Input matching
C2	10	nF	0402	Various	RF grounding
C3	10	nF	0402	Various	RF grounding
C4	330	pF	0402	Various	DC block/Output matching
L1	220	nH	0402	Murata LQG15A	DC feed/ Input matching
R1	110	Ω	0402	Various	Output matching/ Stability
N1	BGB741L7		TSLP-7-1	Infineon Technologies	SiGe:C MMIC LNA

3.2 Evaluation board BGS12AL7-4

Application schematic of the SPDT switch offered by Infineon is shown below. It is a one chip solution integrating RF switch and the control logic. The switch can be connected to the respective RF and DC ports in an application directly without the need for any external components. The device also integrates ESD protection devices which protect it against ESD events up to 1 kV (Human Body Model; IEC61340-3-1) on all ports

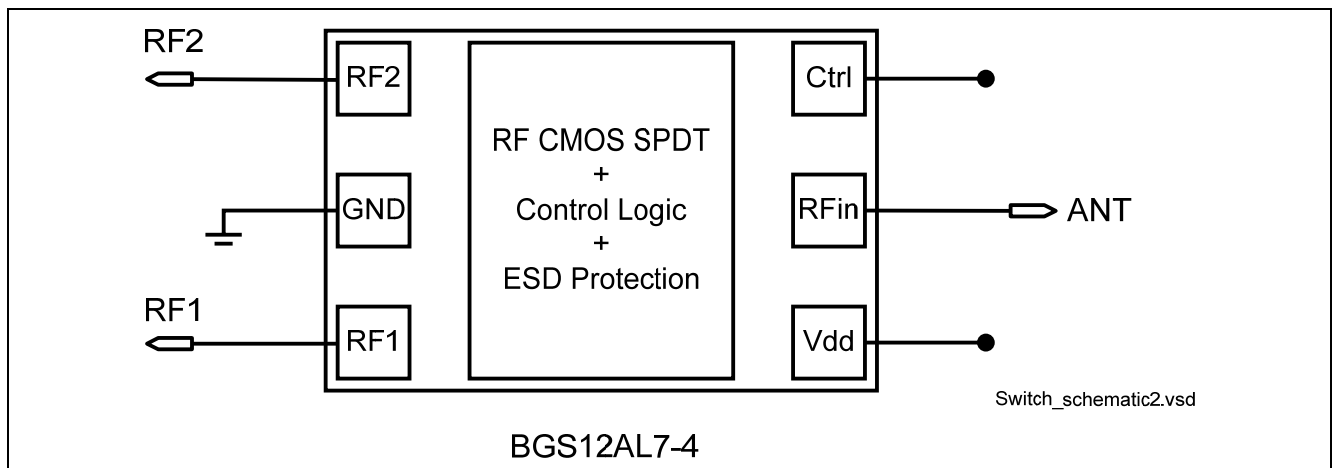


Figure 6 Schematic of the BGS12AL7-4 application.

3.3 Test setup for combination LNA and Switch

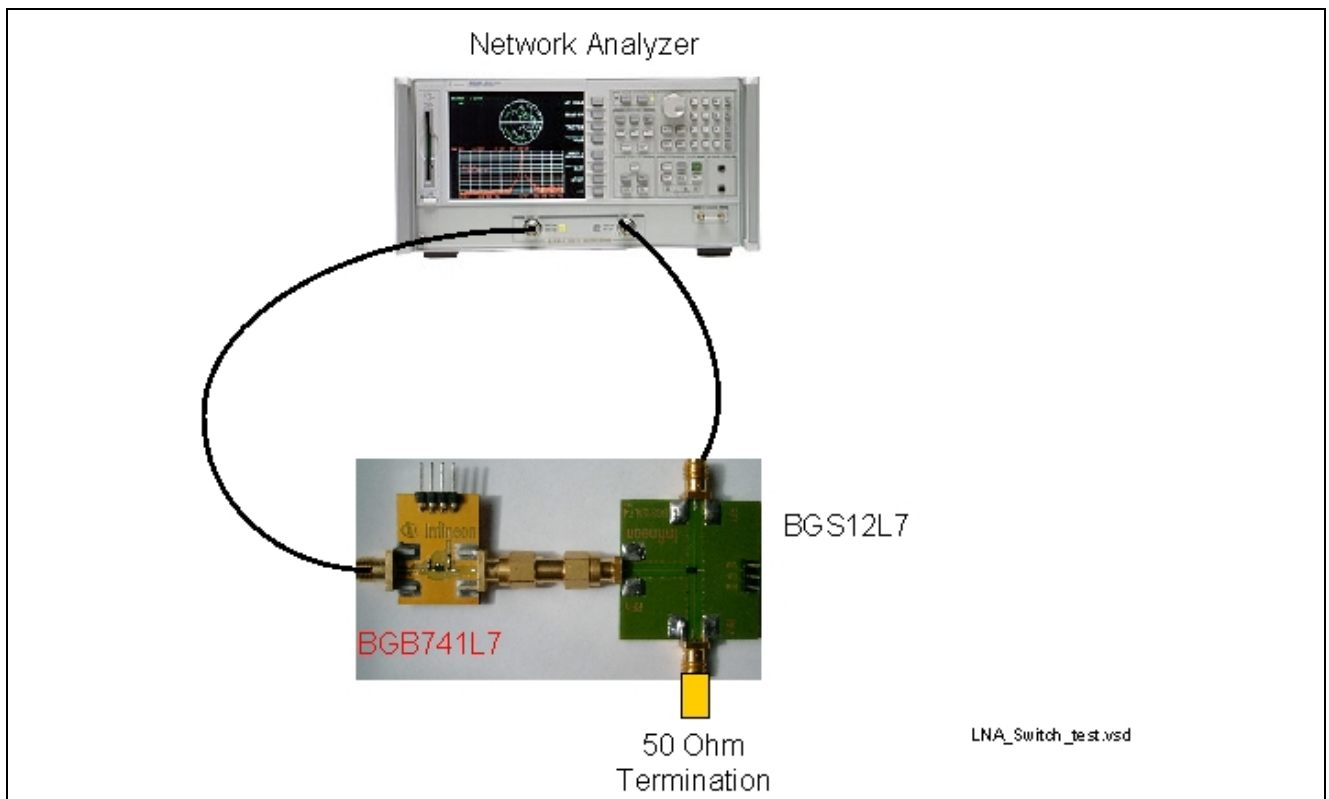


Figure 7 Test Set-up for LNA/Switch configuration

In our test set-up we connect an evaluation board of the BGB741L7 with an eva board of the BGS12AL7-4 and test the combination in a 50 Ohm test environment.

4 Measurement Results Summary

In table 4 a summary of the measured results is shown. V_{cc} , V_{ctrl} = 2.8V, I = 5.4mA

Table 4 Summary of Measurement Results

Parameter	Symbol	Value			Unit	Note/Test Condition
Frequency Range	Freq	50	450	850	MHz	
DC Voltage	V_{cc}	2.8			V	
DC Current	I_{cc}	5.4			mA	
Gain	G	15.1	15.0	14.7	dB	Power @ port1 = -30 dBm
Noise Figure	NF	2.2	1.2	1.5	dB	Including SMA connectors and PCB losses of 0.1dB
Input Return Loss	RL_{in}	-7.6	-10	-8.2	dB	
Output Return Loss	RL_{out}	-9.2	-26	-22	dB	
Reverse Isolation	$ I_{Rev} $	24	27.8	25.5	dB	Power @ port2 = -10 dBm
Input IP3	IIP3	-3			dBm	Power @ Input = -30 dBm Measured @ f_1 = 840MHz Δf = 1 MHz
Output IP3	OIP3	11.9			dBm	
Stability	k	>1.4			--	Stability measured up to 10GHz

5 Measured Graphs

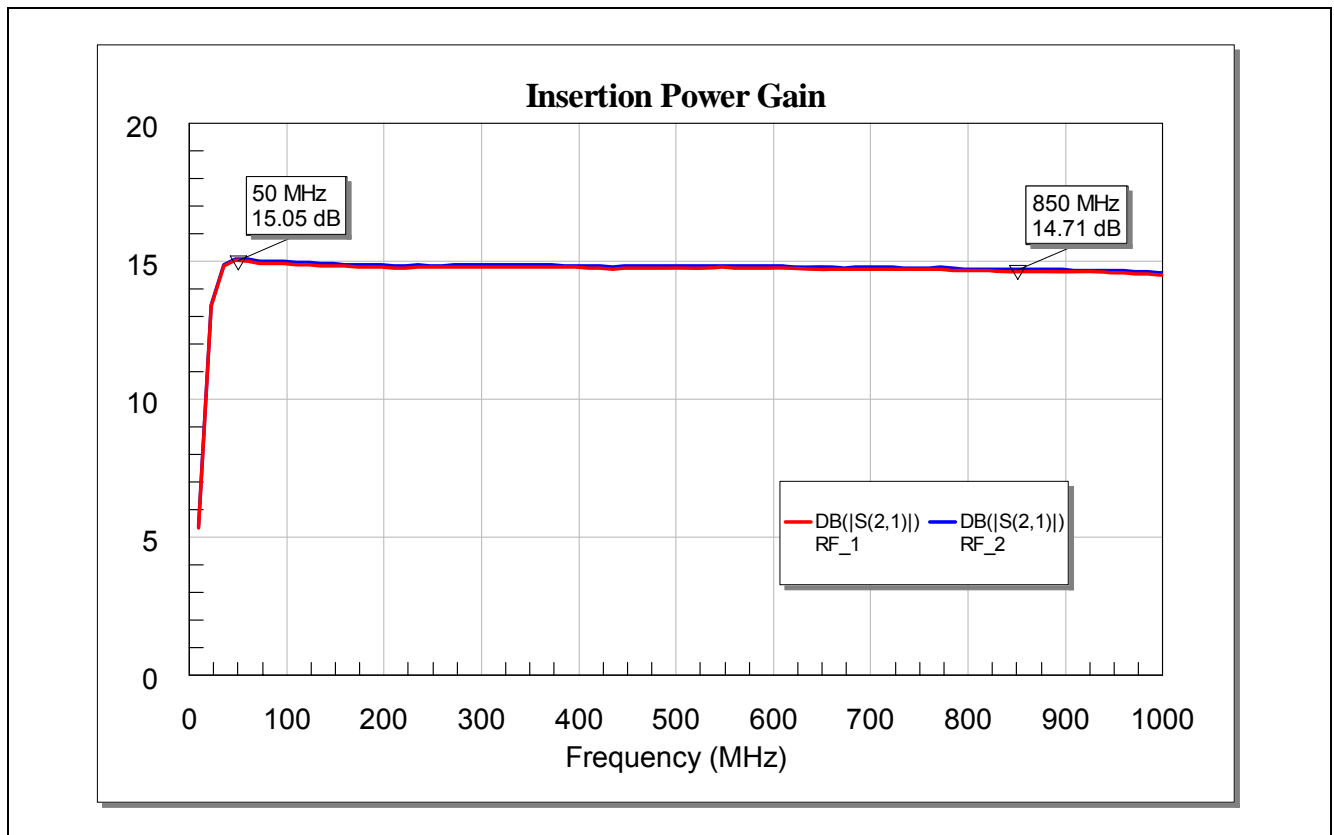


Figure 8 Insertion Power Gain on RF1 and RF2 Outputs.

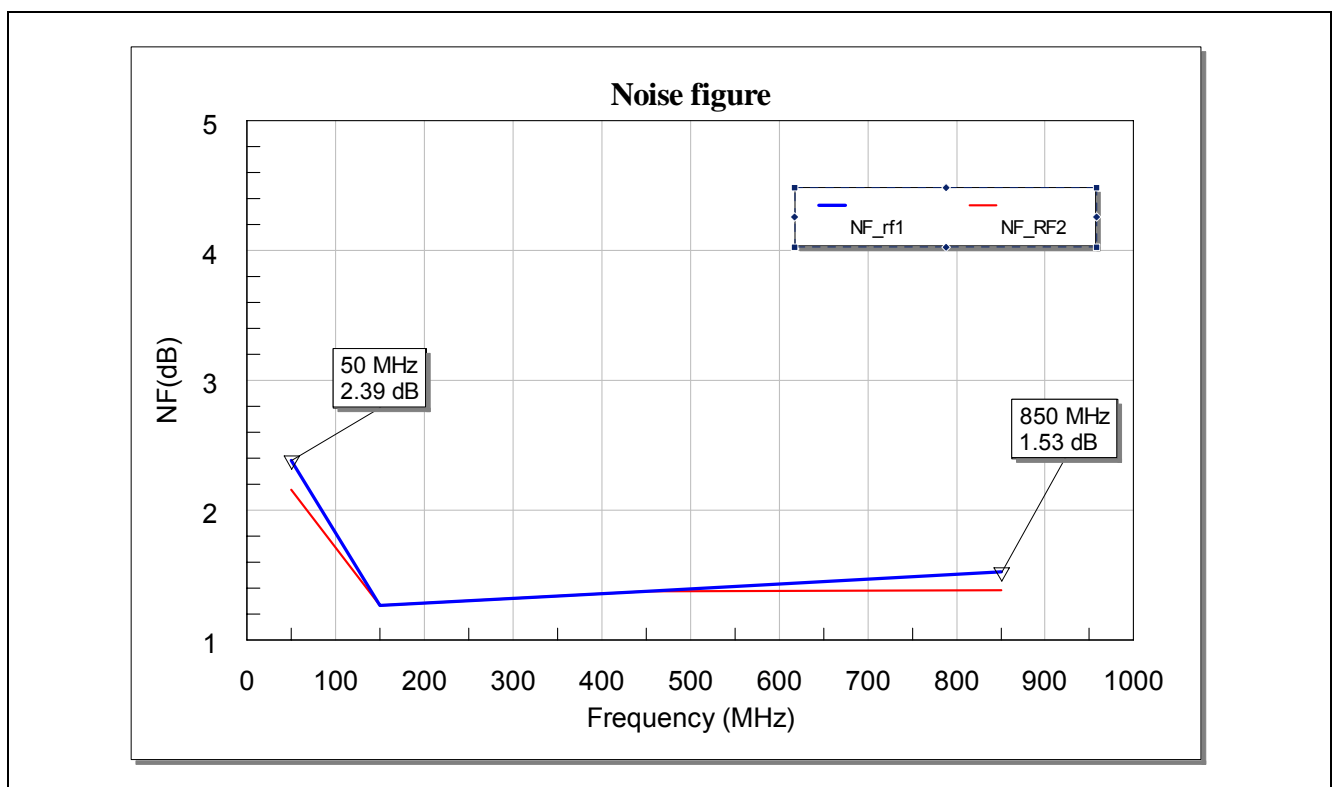


Figure 9 Noise figure

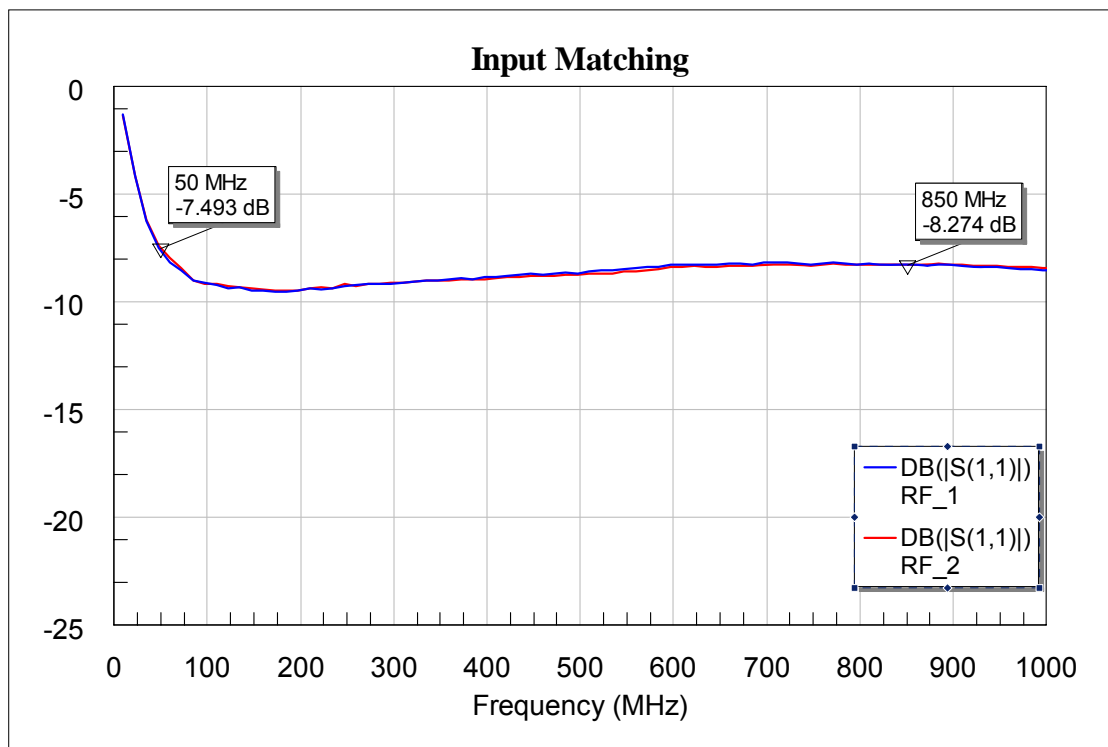


Figure 10 Input Matching

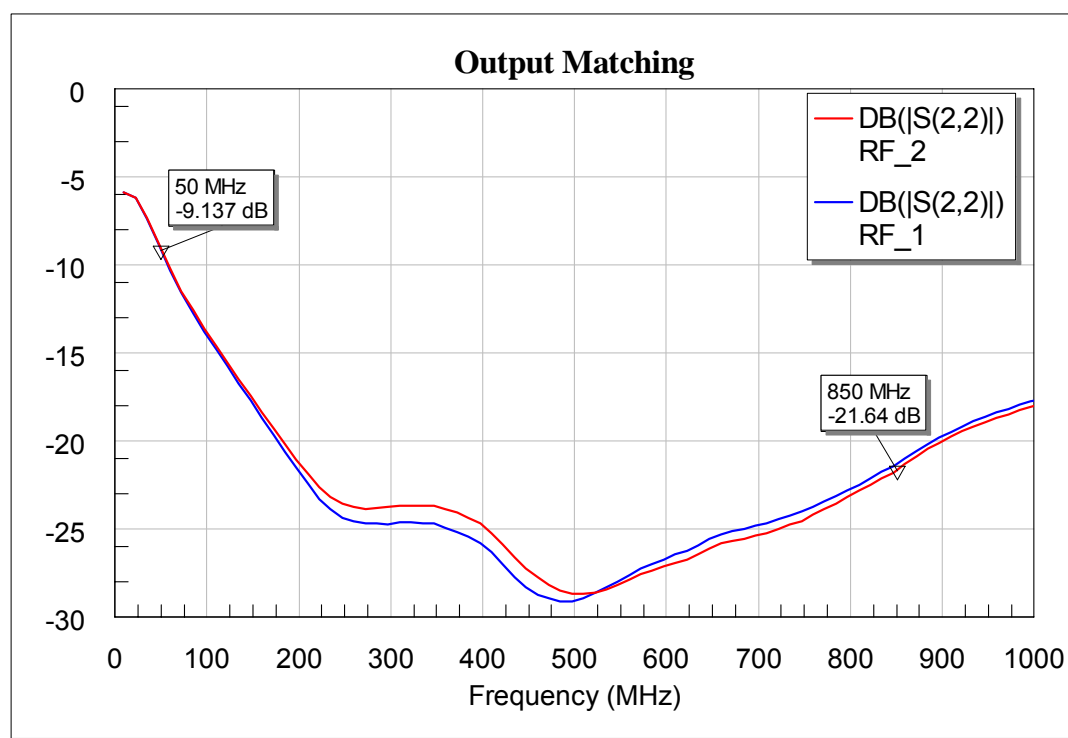


Figure 11 Output Matching

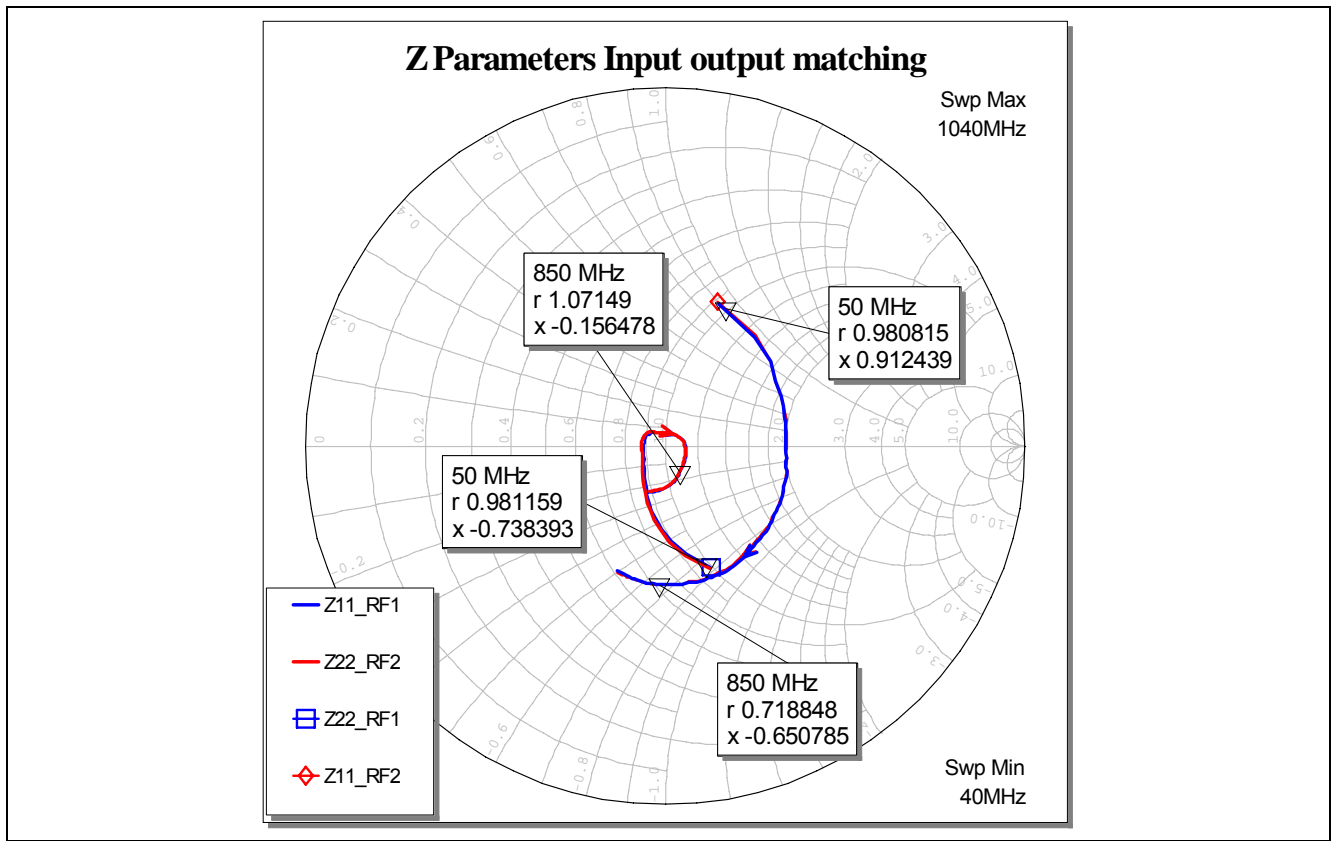


Figure 12 Z Parameters of In- and Output Matching

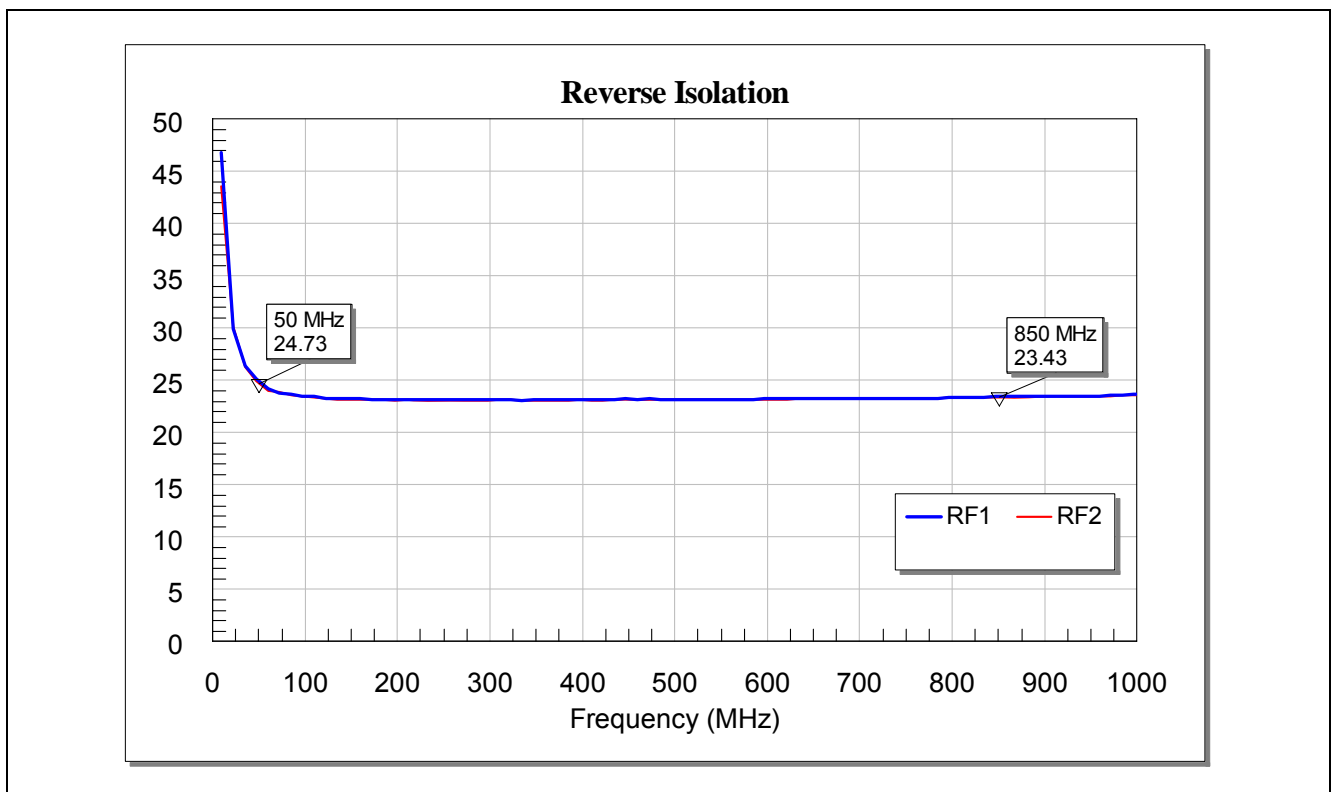


Figure 13 Reverse Isolation of the BGB741L7ESD

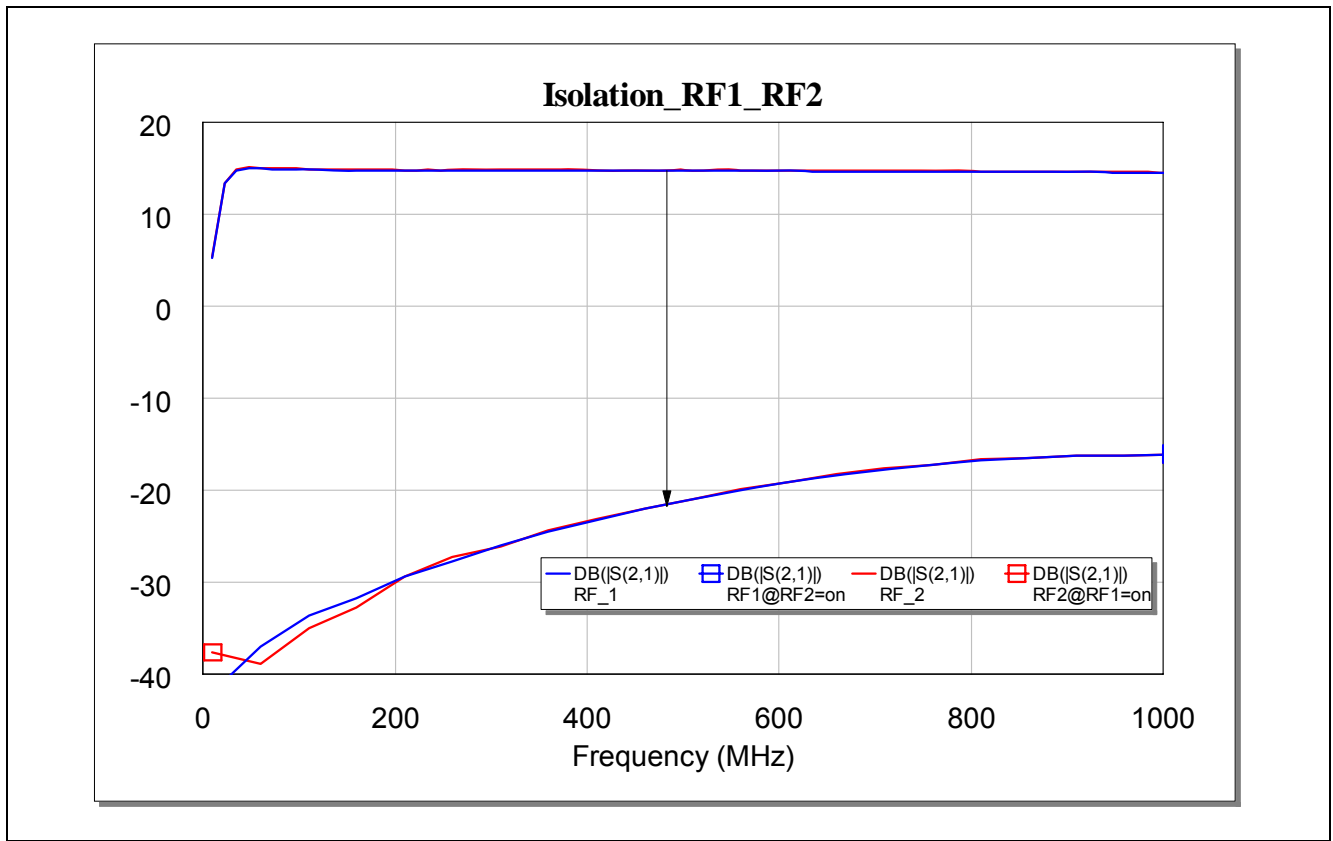


Figure 14 Isolation of RF1 and RF2

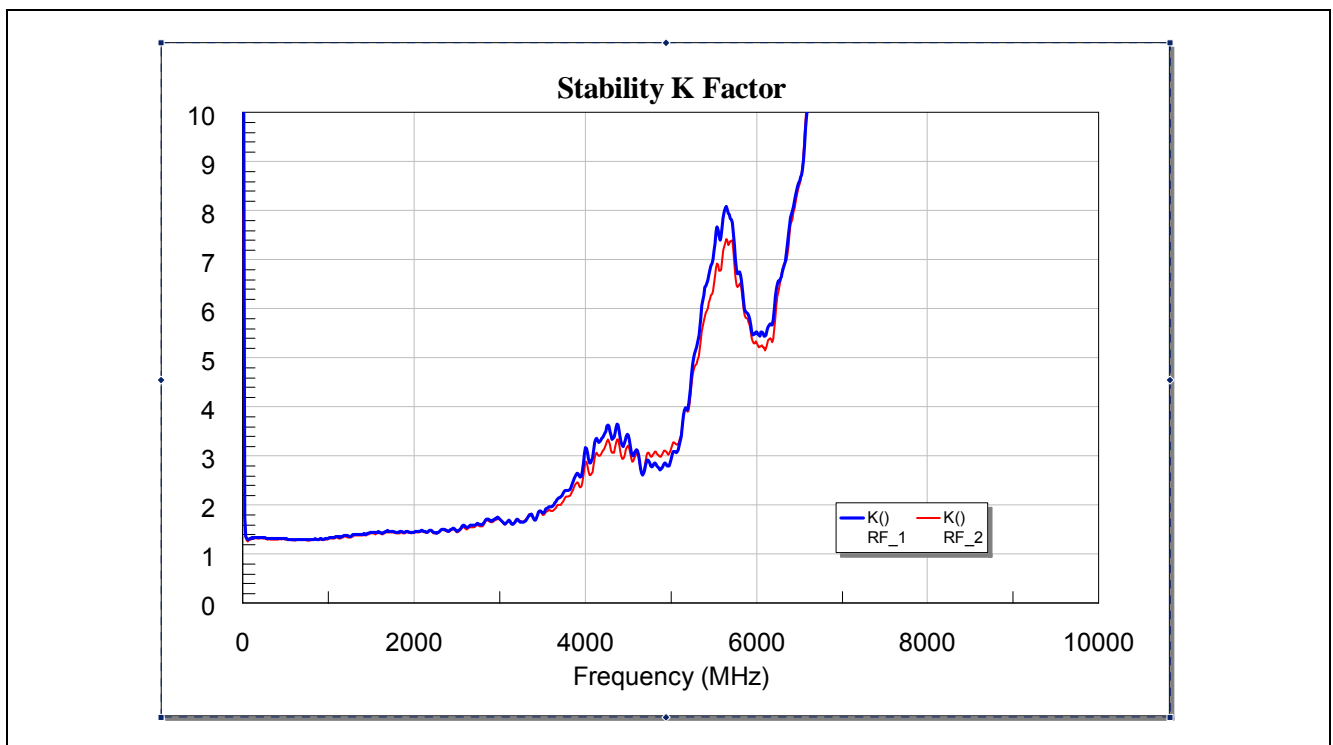


Figure 15 Stability shown in k Factor

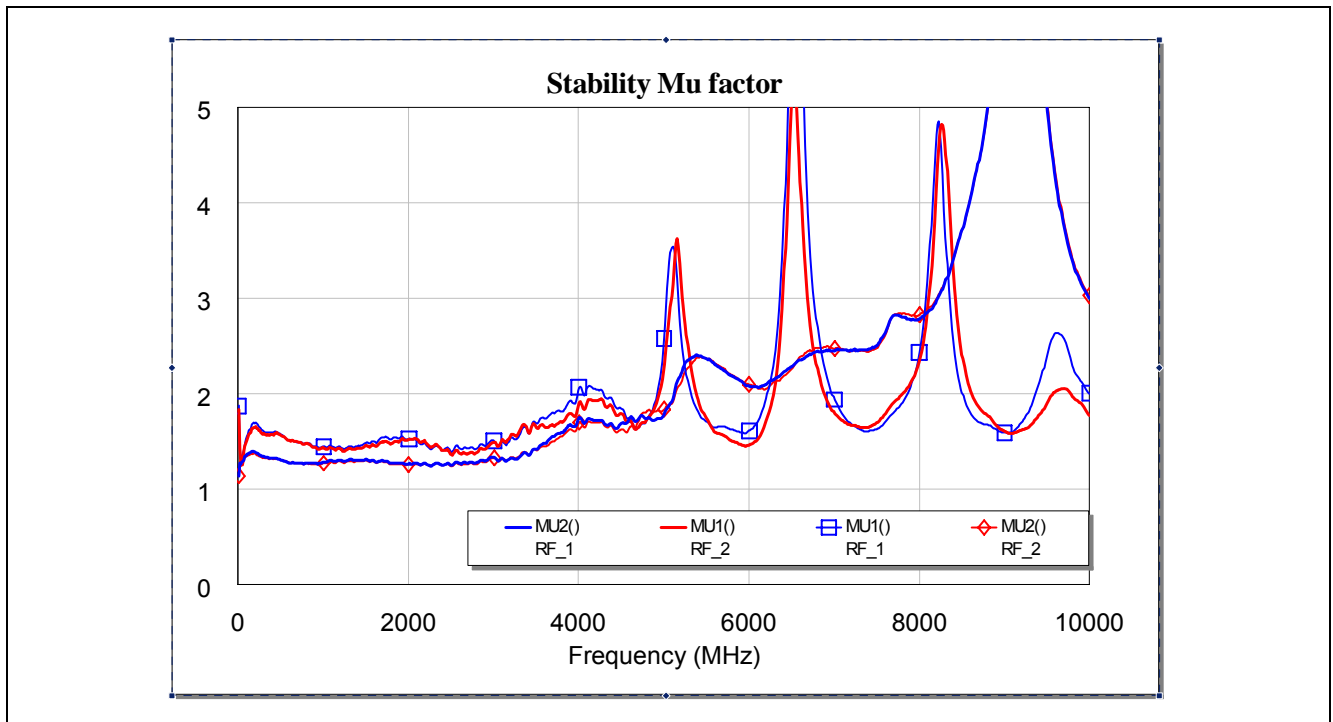


Figure 16 Stability shown in MU Factor

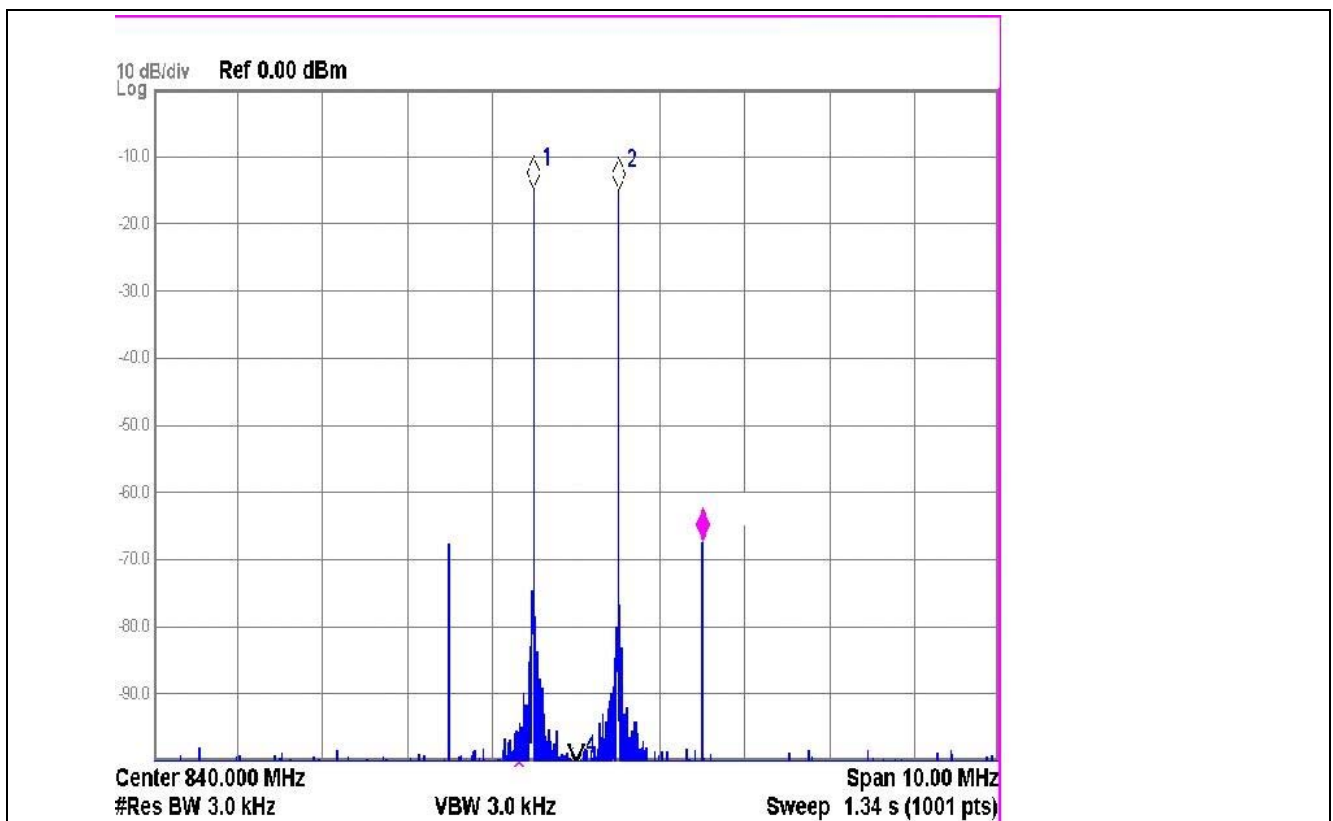


Figure 17 IM 3 Measurement

Input Stimulus for Amplifier Two-Tone Test.

$f_1 = 839.5 \text{ MHz}$, $f_2 = 840.5 \text{ MHz}$, -30 dBm each tone.

Input $IP_3 = -30 + (53.8 / 2) = -3.1 \text{ dBm}$

Output $IP_3 = -3.1 + 15 = +11.9 \text{ dBm}$

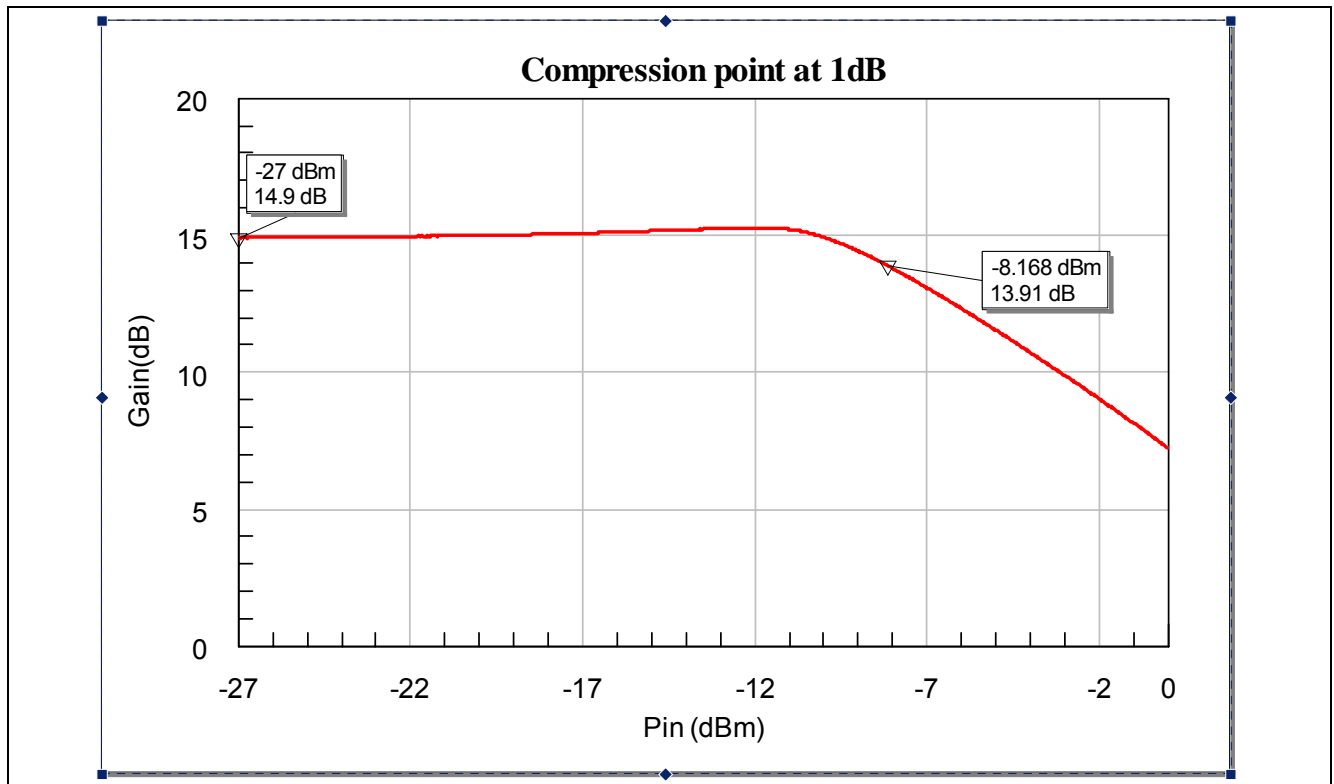


Figure 18 1dB Compression Characteristic

6 Evaluation Board and layout Information

6.1 BGB741L7 Evaluation Board

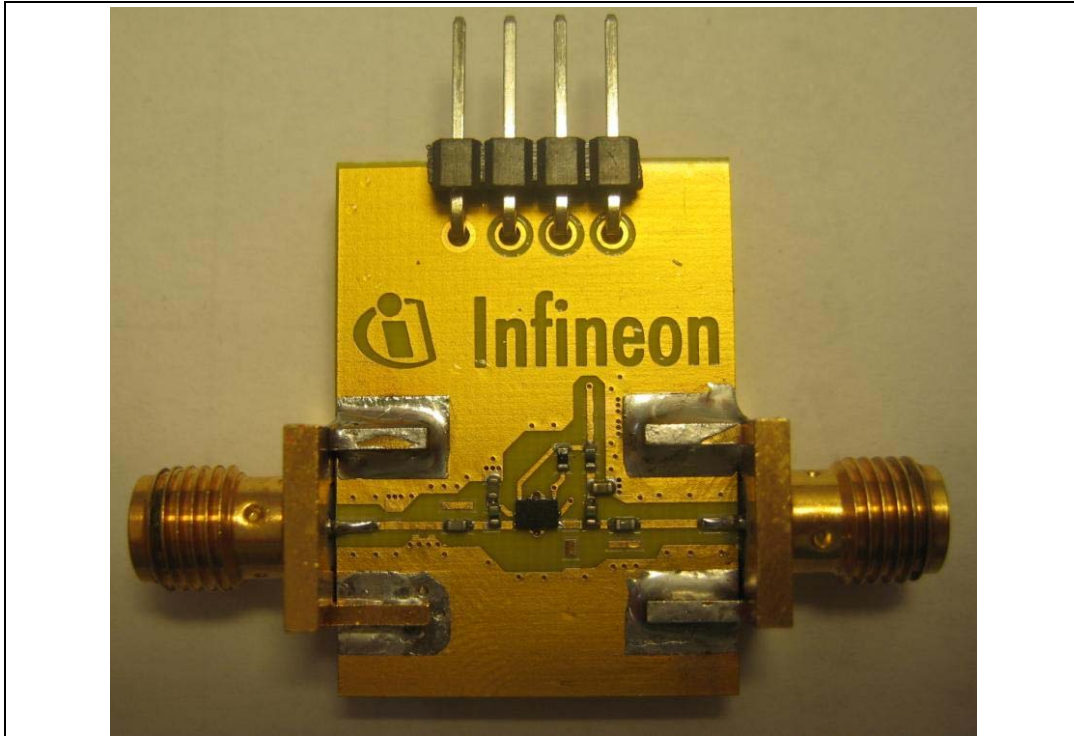


Figure 19 Photo of Evaluation Board

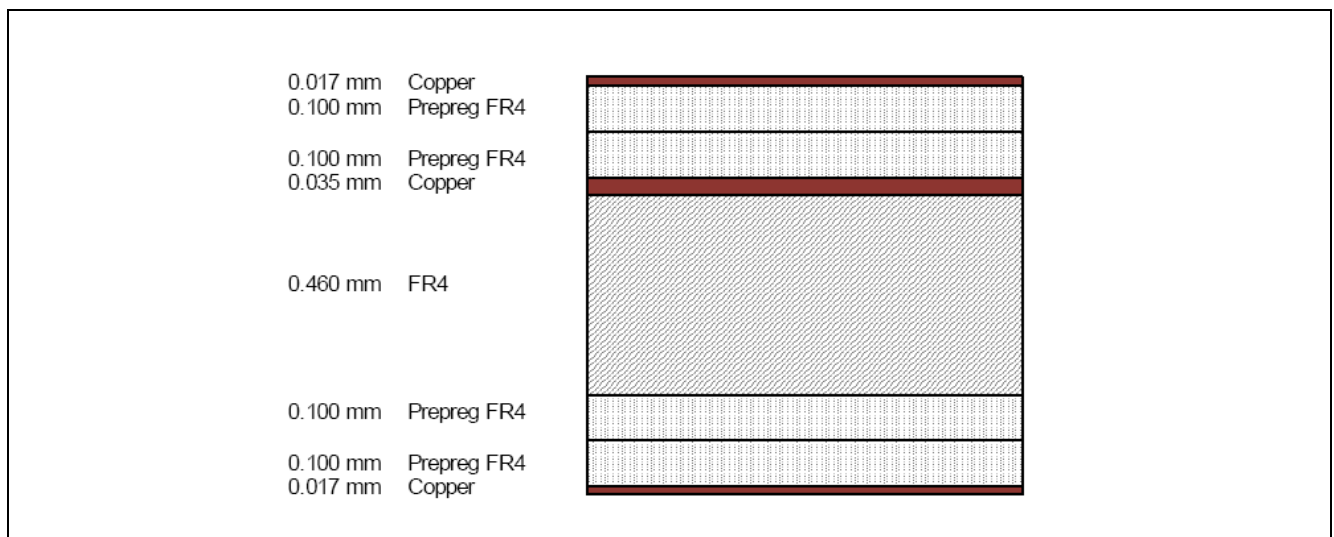


Figure 20 PCB Layer Information

6.2 BGS12A Eva Board

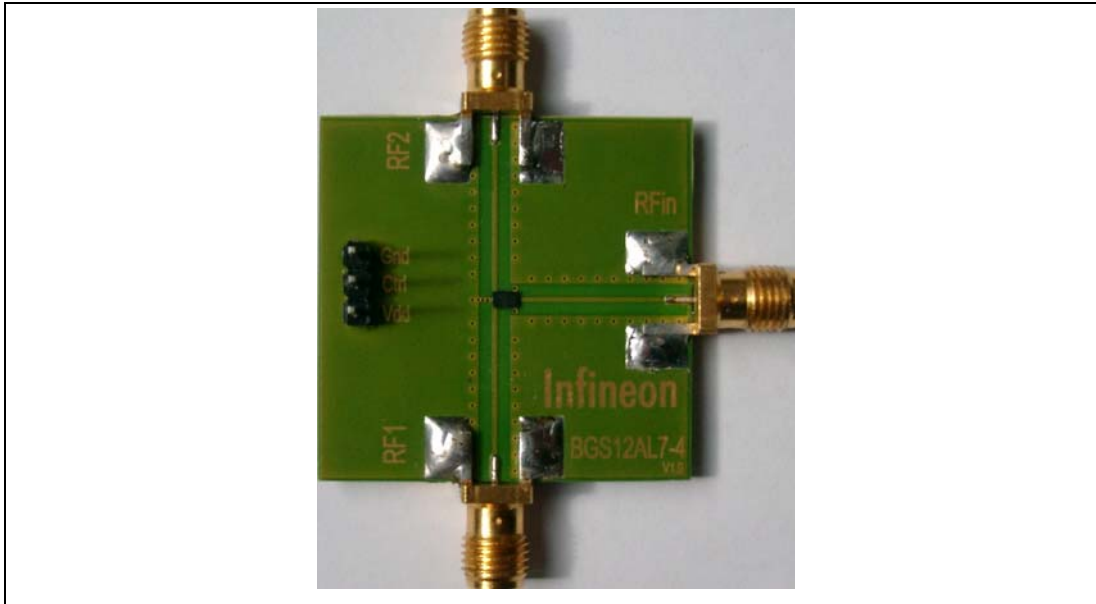


Figure 21 Photo of BGS12A eva board

This section deals with some tips and recommendations for the PCB design. Standard FR4 can be used as the PCB substrate material, but in order to keep the losses as low as possible, Rogers 4003 is used for the application boards provided by Infineon for switch evaluation. In addition, to attain mechanical strength, a layer of FR4 can be used in a multilayer configuration as shown in Figure 13. Signal grounding is a prime concern for RF circuits and thus it is recommended to have via holes under the chip for an optimum RF grounding. The vias under the chip also act as a good heat sink. For the given PCB structure, the microstrip line width is 0.45 mm, with a spacing of 1.2 mm to the coplanar ground plane.

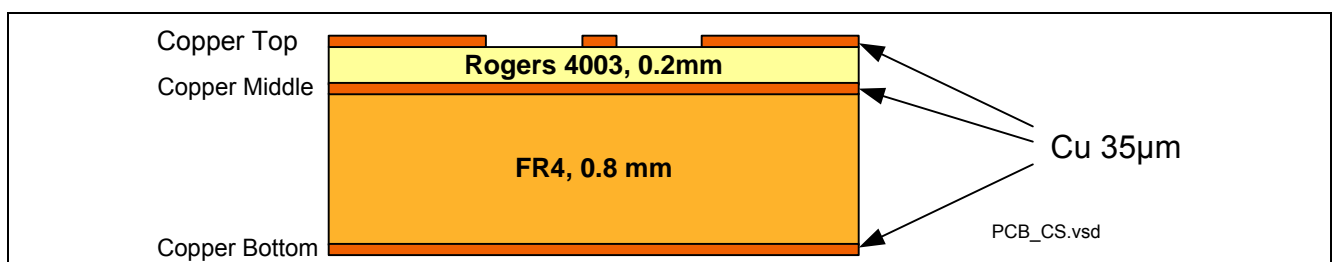


Figure 22 PCB Structure of the Eva Board

Appendix 1: ESD protection circuit for system level ESD robustness

Introduction

With the advancement in miniaturization of semiconductor structures, ESD handling capability of the devices is becoming a concern. Increasing ESD handling capability of the I/O ports costs additional chip size and affects the I/O capacitance significantly. This is very important for high frequency devices, especially when high linearity is required. Therefore, tailored and cost effective ESD protection devices can be used to build up an ESD protection circuit. To handle ESD events during assembly, devices normally have on-chip ESD protection according to the device level standards e.g. "Human Body Model" JEDEC 22-A-115. To fulfill the much more stringent system level ESD requirements according to IEC61000-4-2 as shown in Figure 23, the external ESD protection circuit has to handle the majority of the ESD strike. The best external ESD protection is achieved using a TVS diode assisted by additional passive components.

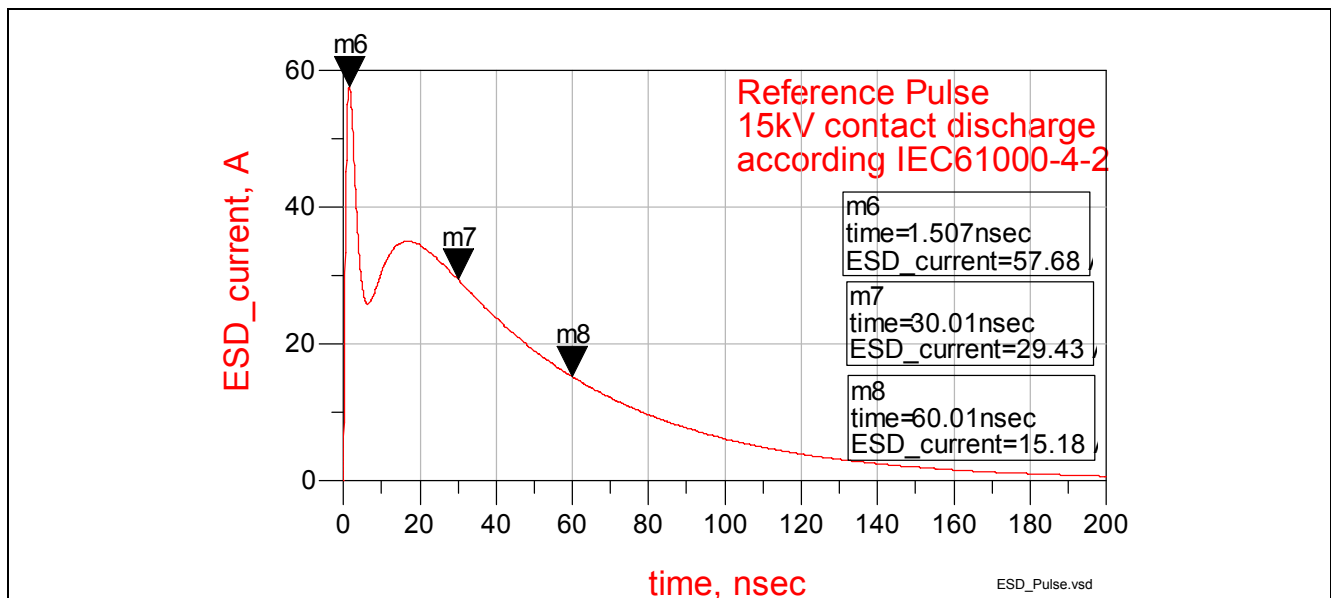


Figure 23 ESD test pulse according to system level specification IEC61000-4-2 – Contact Discharge 15kV

Some examples of RF applications addressed by the Infineon ESD protection proposal are given below:

- FM Radio (76 MHz -110 MHz)
- Portable TV (50 MHz – 850 MHz)
- WLAN 802.11b/g/n (2.4 GHz, Tx ~ +20 dBm)
- Bluetooth (2.4 GHz, Tx ~ +20 dBm)
- Automatic Meter Reading, AMR (900 MHz, TX ~ +20 dBm)
- Remote Keyless Entry, RKE (315 MHz - 434 MHz - 868 MHz - 915 MHz, Tx~13 dBm)
- GPS (1575 MHz, Rx only but can be affected by RF interferer)

For an ESD protection device tailored for medium power RF signals ($\leq +20$ dBm), following requirements are essential:

Appendix 1: ESD protection circuit for system level ESD robustness

1. RF requirements

- a) Bidirectional characteristic to handle DC free signals without clipping / signal distortion
- b) A highly symmetrical behavior of the ESD device for positive and negative voltage swings is mandatory to keep the power level of even Harmonics low
- c) Breakdown voltage of 5 V-10V, to avoid signal distortion at high RF voltage swing applied at the TVS diode, located close to the antenna
- d) High linearity
- e) Low leakage current and stable diode capacitance vs. RF voltage swing
- f) Ultra low diode capacitance is mandatory

2. ESD requirements

- a) Lowest dynamic resistance R_{dyn} to offer best protection for the RFIC; R_{dyn} is characterized by Transmission Line Pulse (TLP) measurement
- b) Very fast switch-on time ($< 1\text{ nsec}$) to ground the initial peak of an ESD strike according to IEC61000-4-2
- c) No performance degradation over a large number of ESD zaps (> 1000)

Two-step ESD Protection approach

General structure for a 2-step ESD approach according to Figure 24 enables to split the entire ESD current between the internal and external ESD protection device. The external device is much more robust and handles the majority of the ESD current. To avoid any impact on the RF behavior of the system and to minimize non linearity effects, the TVS diode should possess an ultra low device capacitance.

Therefore the bi-directional (symmetrical) Infineon TVS Diode ESD0P2RF is well suited, which provides a diode capacitance as low as 0.2 pF and a R_{dyn} of only 1 Ohm. ESD robustness can be improved one step more by adding a small serial resistor between the external TVS diode and the RF amplifier input. A resistor of $\sim 2.2\text{ Ohm}$ is a good compromise between additional ESD performance and insertion loss. The TVS diode ESD0P2RF in combination with the 2.2 Ohm ESD resistor would incur less than 0.23dB insertion loss up to 3 GHz.

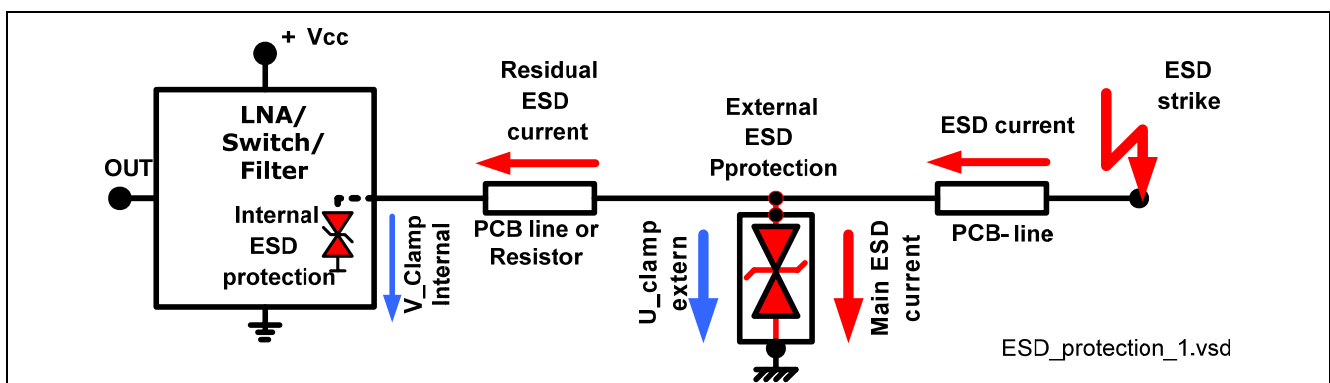


Figure 24 Smart 2-step ESD protection approach based on external and internal ESD protection structure

Appendix 1: ESD protection circuit for system level ESD robustness

For further ESD improvement it is highly recommend to add a serial capacitor (C1). The capacitor cuts off most of the high energy created by the ESD strike. For better ESD robustness, C1 should be as small as possible, but has to match to the intended application frequency as well. For a broadband ESD protection (80MHz...3GHz) C1 should be about 100pF...150pF. Optional matching can be implemented with a serial inductor L1 for a dedicated frequency. In combination with L1, C1 can be reduced significantly which improves the ESD performance.

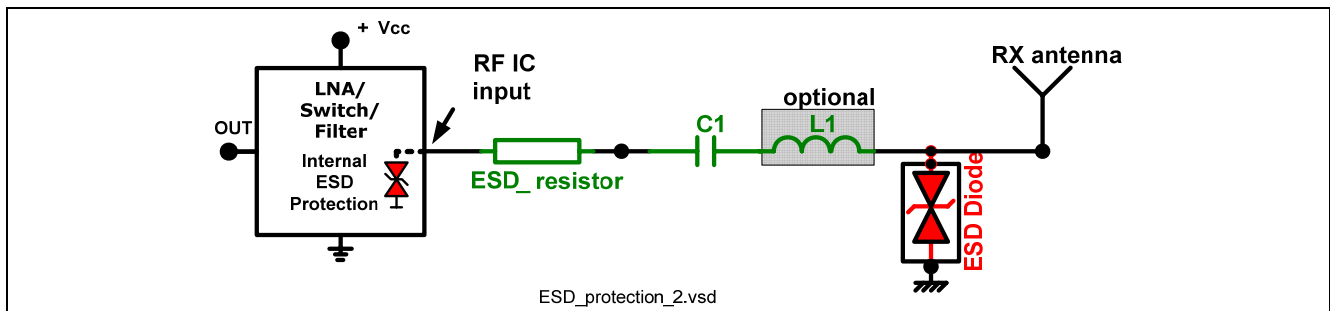


Figure 25 Standard ESD protection topology with optional ESD resistor, blocking capacitor and a serial inductor

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