Application Note No. 013

800 - 1000 MHz PIN-Diode Transmit-Receive Switch

RF & Protection Devices

Never stop thinking

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800 - 1000 MHz PIN-Diode Transmit-Receive Switch
Revision History: 2006-10-20, Rev. 2.0

Previous Version: 2000-07-27

Page	Subjects (major changes since last revision)
All	Document layout change

1 800 - 1000 MHz PIN-Diode Transmit-Receive Switch

This application is designed to serve as a non mechanical transmit-receive switch for AMPS, GMS and PDC mobile telephones.

Advantages

- No power consumption in receive state
- No negative voltage required
- Low component count
- Low cost

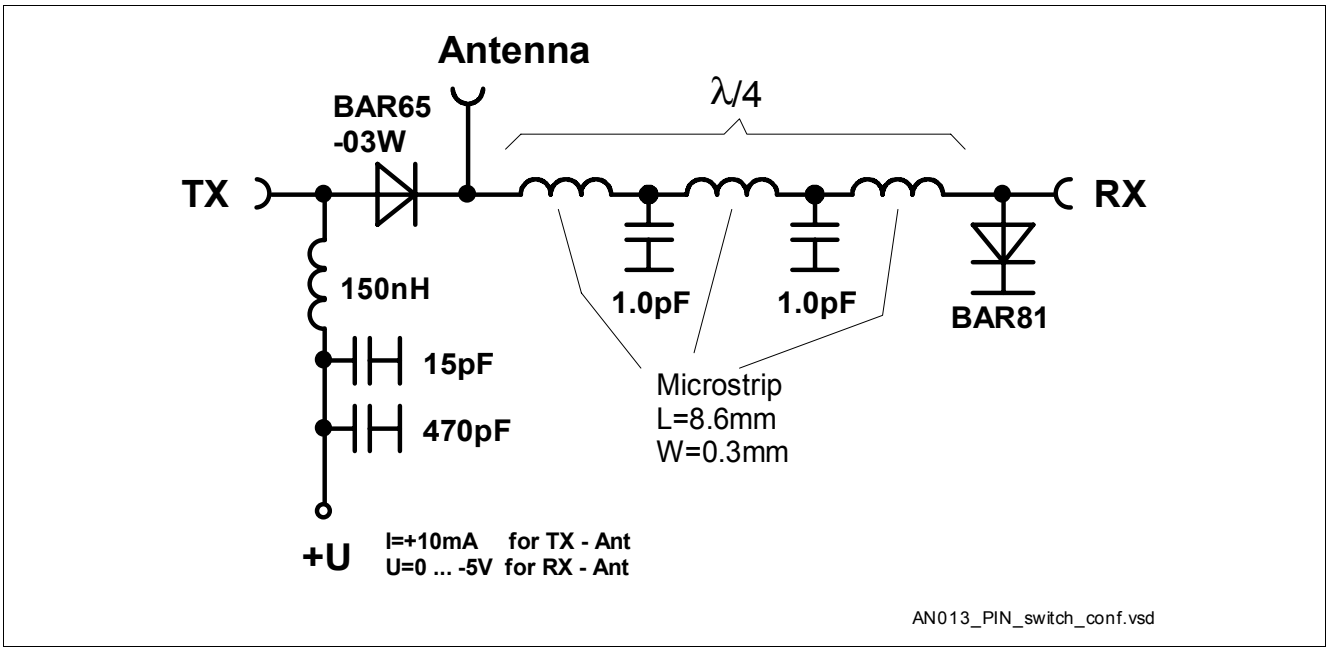

Figure 1 PIN diode switch configuration

Table 1 Performance Data at 800 - 1000 MHz

Transmit-state (I = +10 mA ... 1 mA)		**Receive-state (U = -5 V)**	
TX-Ant. Loss	0.3 ... 0.4 dB[1)]	RX-Ant. Loss	0.55 ... 0.6 dB[1)]
Ant.-RX Isolation	35 ... 32 dB	TX-RX Isolation	17 ... 16 dB
TX-RX Isolation	35 ... 33 dB	TX-Ant. Isolation	19 ... 17 dB

1) These values are the overall losses, evaluation of a dummy-circuit with diodes replaced by open / short show 0.15 dB loss in TX-Antenna path and 0.2 dB from Antenna to RX.

2 Harmonic Distortion Characteristics Measurements

2.1 Measurement Setup

TX-Port: f = 890 MHz, 33 dBm power, harmonic suppression > 95 dBc
RX-Port: DC- blocked 50 Ω termination
Ant.-Port: DC-blocked spectrum analyzer

Values referred to input power level at TX-Port:

Table 2 Input power level at TX-Port

	1. Harmonic @ 1.78 GHz	2. Harmonic @ 2.67 GHz
I = 5 mA	72 dBc	> 95 dBc
I = 10 mA	75 dBc	> 95 dBc

2.2 Functional Description

- In transmit mode both diodes are forward biased and therefore conduct. The short-circuit BAR80 diode at the RF-port is transformed into an open-circuit at the Antenna-port by a λ/4 line.
- In receive mode, both diodes are reverse biased and therefore non conducting. The RF signal passes from Antenna- to RX-port via λ/4 line.

Further improvement of the circuit can be achieved by compensation of the remaining diode-capacitance in off-state with shunt-inductors.

The λ/4 line is realized by microstripline inductors and SMD capacitors to reduce the length of the assembly.

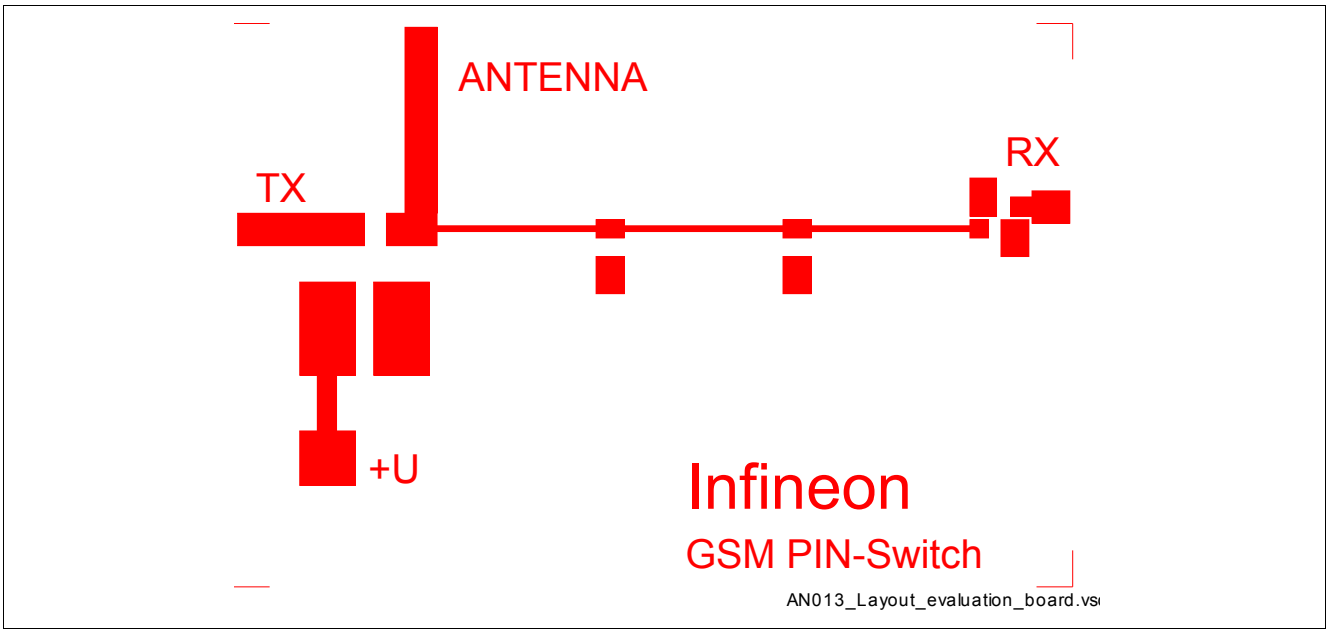

Figure 2 Layout of the evaluation board (size: 30 mm x 45 mm)

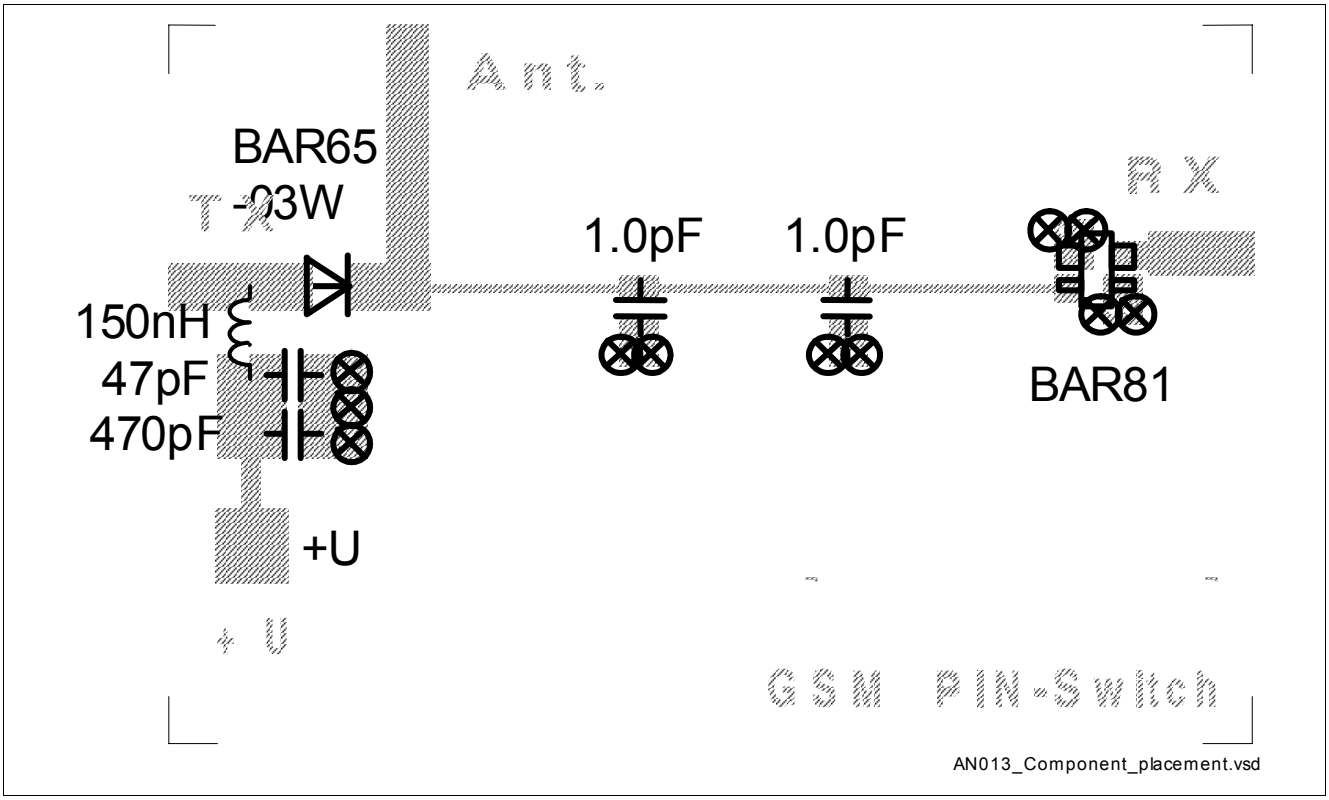

Figure 3 Component placement

Table 3 Part List

BAR81	PIN diode	MW-4	Infineon
BAR65-03W	PIN diode	SOD323	Infineon
1.0 pF	Cap.	0805	S+M
15 pF	Cap.	0805	S+M
470 pF	Cap.	0805	S+M
150 nH	Ind.	SIMID01	S+M
Board	1 mm Epoxy FR4, 30 x 45 mm		

2.3 Simulation

For simulation with Microwave Harmonica V6.0. the PIN-Switch structure is divided into several elements:

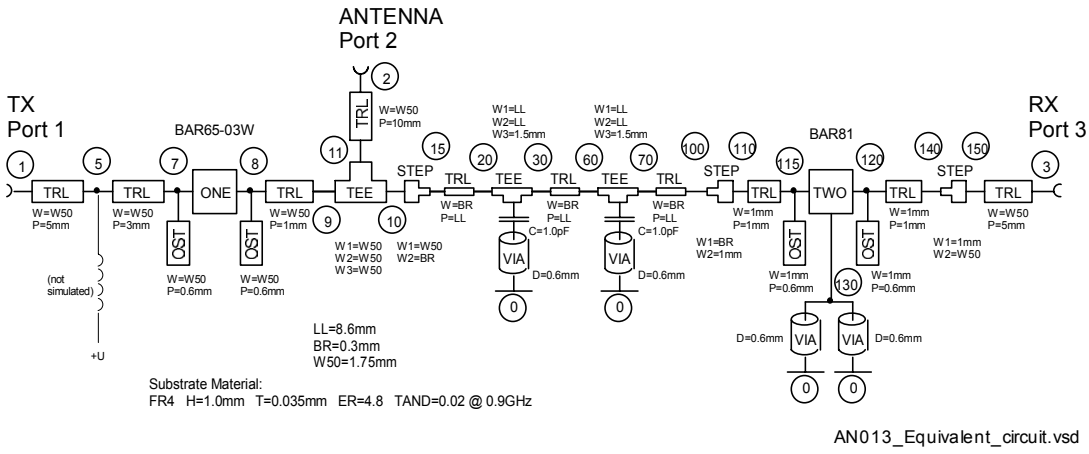

Figure 4 Several PIN-Switch elements for simulation with Microwave Harmonica

These Elements must be placed into a description file:

```
*********************************************************************
* 800-1000 MHz    T/R-Switch with BAR81/BAR65-03W
*********************************************************************
*
*                ANT
*               Port 2
*                 O
*                 |    Ind.      Ind.      Ind.
*           |\    |   /-\/-\    /-\/-\    /-\/-\
*    TX  o--| >|--o--|     |-+-|     |-+-|     |-----o-----O    RX
*  Port 1   |/    |              |         |           |        Port 3
*           BAR65               |         |         +------+
*           -03W          C --+--   C --+--         \    / BAR81
*                            --+--     --+--          \  /
*                              |         |          ---+---
*                              |         |             |
*                            ---+---   ---+---       ---+--- GND
*
*  Substrate Material:
*  FR4, H=1mm, T=0.035mm, ER=4.8, TAND=0.02 @ 0.9GHz
*
*  24.10.95     K. Brenndoerfer          HL EH PD
*  13.02.96     J.P. Schaffer            HL EH PD1
*********************************************************************
                                        AN013_Discription_file_simulation.vsd
```

Figure 5 Circuit design Simulation

```
    kap:  1.0PF    ; Capacitor to simulate quater lambda line
    ll:   8.6MM    ; length of trl (inductor) to simulate quater lambda li
    br:   0.3mm    ; width of trl (inductor) to simulate quater lambda lir
    w50:  1.75mm   ; width of 50 ohm line

BLK     ; RX-ANT ON,  TX-ANT OFF
    trl    1   5       w=w50    p=4.85mm           sub
    trl    5   7       w=w50    p=2.0mm            sub
    ost    7           w=w50    p=0.6mm            sub
    one    7   8       b65of                                ; BAR65-03W
    ost    8           w=w50    p=0.6mm            sub
    trl    8   9       w=w50    p=1.0mm            sub
    tee    9  10  11   w1=w50   w2=w50   w3=w50    sub
    trl   11   2       w=w50    p=10mm             sub

    step  10  15       w1=w50   w2=br              sub
    trl   15  20       w=br     p=ll               sub
    tee   20  30  40   w1=br     w2=br    w3=1.0mm  sub
    cap   40  50       c=kap
    via   50           d=0.5mm                     sub
    via   50           d=0.5mm                     sub
    trl   30  60       w=br     p=ll               sub
    tee   60  70  80   w1=br     w2=br    w3=1.0mm  sub
    cap   80  90       c=kap
    via   50           d=0.5mm                     sub
    via   50           d=0.5mm                     sub
    trl   70 100       w=br     p=ll               sub
    step 100 110       w1=br    w2=1mm             sub
    trl  110 115       w=1mm    p=1mm              sub
    ost  115           w=1mm    p=0.6mm            sub
    two  115 120 130   b81of                                ; BAR81
    ost  120           w=1mm    p=0.6mm            sub
    via  130           d=0.5mm                     sub
    via  130           d=0.5mm                     sub
    trl  120 140       w=1mm    p=1.2mm            sub
    step 140 150       w1=1mm   w2=w50             sub
    trl  150   3       w=w50    p=3mm              sub
    rxan:  3por  1  2  3                                   ; 1=TX  2=ANT  3=
END
```

AN013_Discription_file_simulation1.vsd

Figure 6 Simulation Data 1

```
BLK        ; RX-ANT OFF,  TX-ANT ON
   trl     1    5       w=w50     p=4.85mm           sub
   trl     5    7       w=w50     p=2.0mm            sub
   ost     7            w=w50     p=0.6mm            sub
   one     7    8       b65on                                  ; BAR65-03W
   ost     8            w=w50     p=0.6mm            sub
   trl     8    9       w=w50     p=1.0mm            sub
   tee     9   10   11  w1=w50    w2=w50    w3=w50   sub
   trl    11    2       w=w50     p=10mm             sub
   step   10   15       w1=w50    w2=br              sub
   trl    15   20       w=br      p=ll               sub
   tee    20   30   40  w1=br     w2=br     w3=1.0mm sub
   cap    40   50       c=kap
   via    50            d=0.5mm                      sub
   via    50            d=0.5mm                      sub
   trl    30   60       w=br      p=ll               sub
   tee    60   70   80  w1=br     w2=br     w3=1.0mm sub
   cap    80   90       c=kap
   via    50            d=0.5mm                      sub
   via    50            d=0.5mm                      sub

   trl    70  100       w=br      p=ll               sub
   step  100  110       w1=br     w2=1mm             sub
   trl   110  115       w=1mm     p=1mm              sub
   ost   115            w=1mm     p=0.6mm            sub
   two   115  120  130  b81on                                  ; BAR81
   ost   120            w=1mm     p=0.6mm            sub
   via   130            d=0.5mm                      sub
   via   130            d=0.5mm                      sub
   trl   120  140       w=1mm     p=1.2mm            sub
   step  140  150       w1=1mm    w2=w50             sub
   trl   150    3       w=w50     p=3mm              sub
   txan:   3por   1   2   3                                    ; 1=TX   2=ANT   3
END

FREQ
   STEP    10MHz    2GHZ     10MHz
END

DATA
   SUB:   MS   H=1mm   ER=4.8   TAND=0.02   MET1=CU 35UM
   b81of:DUMMY                 FILE=a:\bar81\mv5v00u0.s2p
   b81on:DUMMY                 FILE=a:\bar81\mvv0010m.s2p
   b65of:DUMMY                 FILE=a:\bar65-3w\5w5v00u0.s1p
   b65on:DUMMY                 FILE=a:\bar65-3w\5wv0010m.s1p
END
```

AN013_Discription_file_simulation2.vsd

Figure 7 Simulation Data 2

The simulation shows the following results:

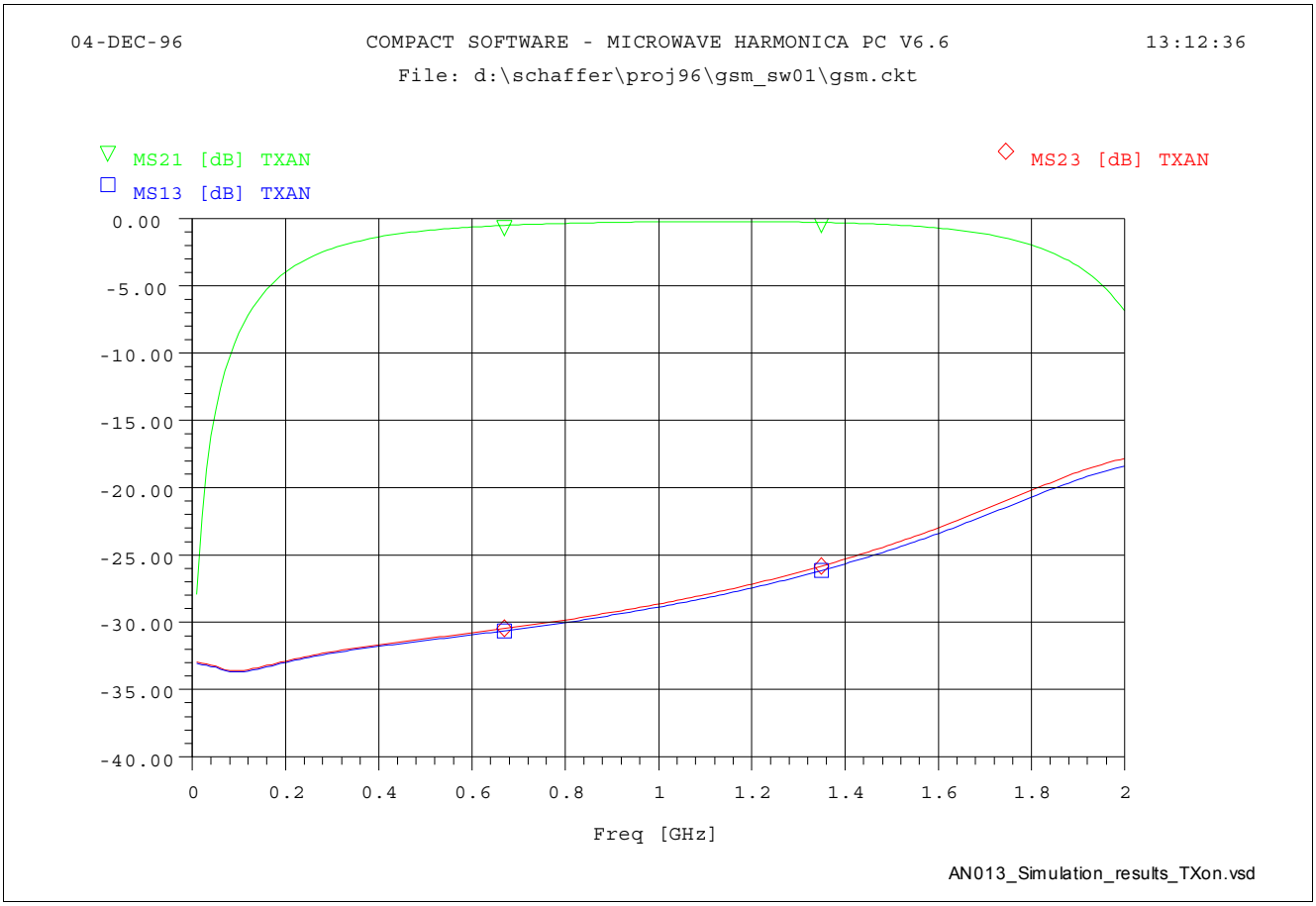

Figure 8 Simulation results: State ‘TX on’

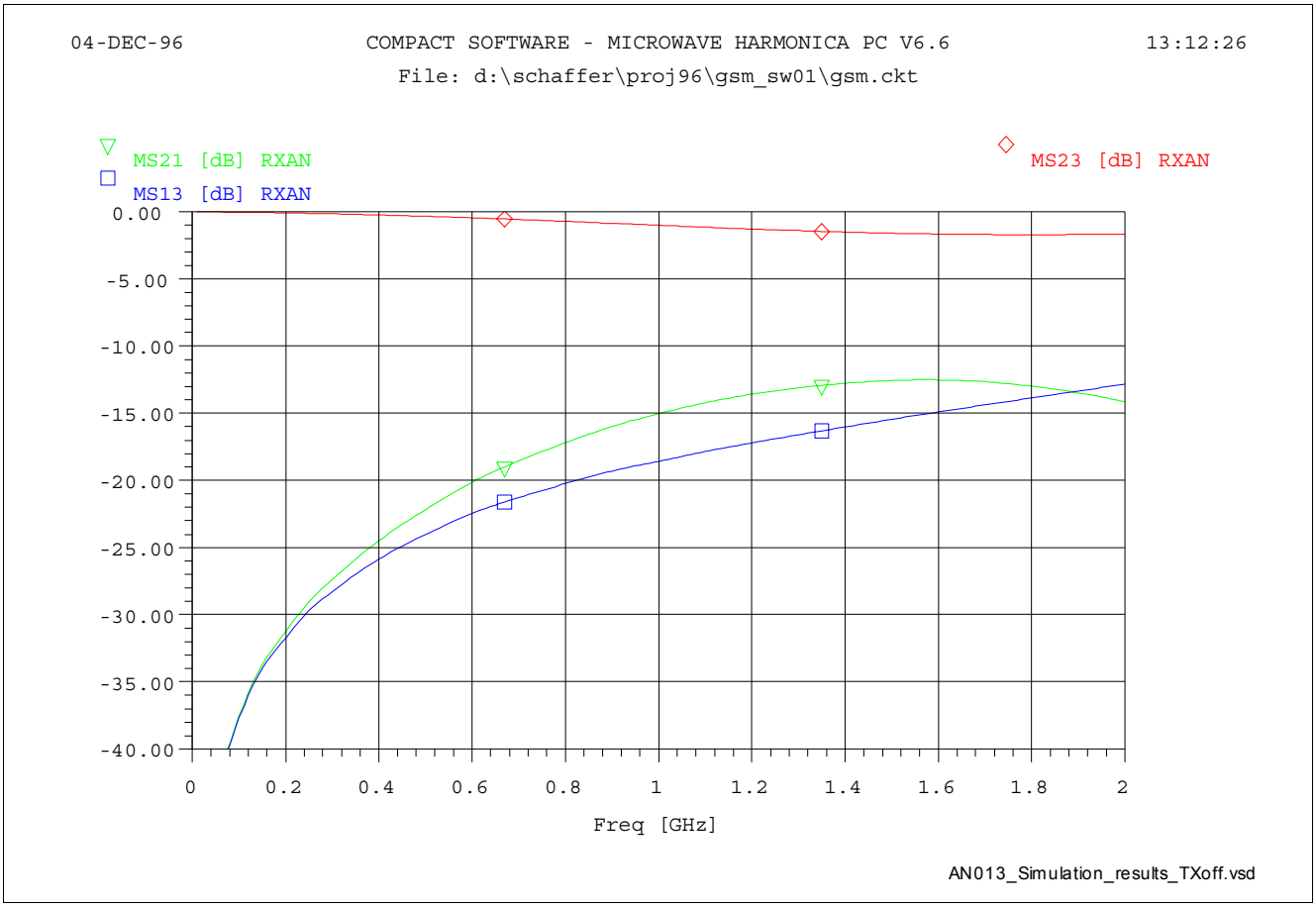

Figure 9 Simulation results: 'TX off'