**5 V Low Power EIA RS-485 Transceiver**

**ADM1485**

**FEATURES**
- Meets EIA RS-485 Standard
- 30 Mbps Data Rate
- Single 5 V Supply
- –7 V to +12 V Bus Common-Mode Range
- High Speed, Low Power BiCMOS
- Thermal Shutdown Protection
- Short-Circuit Protection
- Driver Propagation Delay: 10 ns
- Receiver Propagation Delay: 15 ns
- High-Z Outputs with Power Off
- Superior Upgrade for LTC1485

**APPLICATIONS**
- Low Power RS-485 Systems
- DTE-DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)

**GENERAL DESCRIPTION**

The ADM1485 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission and complies with both RS-485 and RS-422 EIA Standards. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled, the outputs are three-stated.

The ADM1485 operates from a single 5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if, during fault conditions, a significant temperature increase is detected in the internal driver circuitry.

Up to 32 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important, therefore, that the remaining disabled drivers do not load the bus. To ensure this, the ADM1485 driver features high output impedance when disabled and also when powered down.

This minimizes the loading effect when the transceiver is not being used. The high impedance driver output is maintained over the entire common-mode voltage range from –7 V to +12 V.

The receiver contains a fail-safe feature that results in a logic high output state if the inputs are unconnected (floating).

The ADM1485 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM1485 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at typical data rates of 30 Mbps while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in PDIP, SOIC, and small MSOP packages.
COMPARABLE PARTS
View a parametric search of comparable parts.

EVALUATION KITS
• Standard RS-485 Half-Duplex Evaluation Board, EVAL-RS485HDEBZ

DOCUMENTATION
Application Notes
• AN-1176: Component Footprints and Symbols in the Binary .Bxl File Format
• AN-960: RS-485/RS-422 Circuit Implementation Guide
Data Sheet
• ADM1485: 5 V Low Power EIA RS-485 Transceiver Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS
• ADI RS-485/RS-422 Cross Reference Guide
• RS-232 Transceivers Cross Reference Guide

TOOLS AND SIMULATIONS
• ADM1485 IBIS Model

REFERENCE MATERIALS
Solutions Bulletins & Brochures
• Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4
• Test & Instrumentation Solutions Bulletin, Volume 10, Issue 3

DESIGN RESOURCES
• ADM1485 Material Declaration
• PCN-PDN Information
• Quality And Reliability
• Symbols and Footprints

DISCUSSIONS
View all ADM1485 EngineerZone Discussions.

SAMPLE AND BUY
Visit the product page to see pricing options.

TECHNICAL SUPPORT
Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK
Submit feedback for this data sheet.

This page is dynamically generated by Analog Devices, Inc., and inserted into this data sheet. A dynamic change to the content on this page will not trigger a change to either the revision number or the content of the product data sheet. This dynamic page may be frequently modified.
### ADM1485—SPECIFICATIONS

*(V<sub>CC</sub> = 5 V ± 5%. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DRIVER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Output Voltage, V&lt;sub&gt;OD&lt;/sub&gt;</td>
<td>5.0</td>
<td>2.0</td>
<td>1.5</td>
<td>V</td>
<td>R = ∞, Test Circuit 1</td>
</tr>
<tr>
<td>V&lt;sub&gt;OD&lt;/sub&gt;</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
<td>V</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; = 5 V, R = 50 Ω (RS-422), Test Circuit 1</td>
</tr>
<tr>
<td>Δ</td>
<td>V&lt;sub&gt;OD&lt;/sub&gt;</td>
<td>for Complementary Output States</td>
<td>0.2</td>
<td>0.2</td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode Output Voltage V&lt;sub&gt;OC&lt;/sub&gt;</td>
<td>3.0</td>
<td>3.0</td>
<td>3.0</td>
<td>V</td>
<td>R = 27 Ω or 50 Ω, Test Circuit 1</td>
</tr>
<tr>
<td>Output Short-Circuit Current (V&lt;sub&gt;OUT&lt;/sub&gt; = High)</td>
<td>35</td>
<td>250</td>
<td>35</td>
<td>mA</td>
<td>–7 V ≤ V&lt;sub&gt;O&lt;/sub&gt; ≤ +12 V</td>
</tr>
<tr>
<td>Output Short-Circuit Current (V&lt;sub&gt;OUT&lt;/sub&gt; = Low)</td>
<td>35</td>
<td>250</td>
<td>35</td>
<td>mA</td>
<td>–7 V ≤ V&lt;sub&gt;O&lt;/sub&gt; ≤ +12 V</td>
</tr>
<tr>
<td>CMOS Input Logic Threshold Low, V&lt;sub&gt;INL&lt;/sub&gt;</td>
<td>2.0</td>
<td>2.0</td>
<td>2.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>CMOS Input Logic Threshold High, V&lt;sub&gt;INH&lt;/sub&gt;</td>
<td>–1.0</td>
<td>–1.0</td>
<td>–1.0</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Logic Input Current (DE, DI)</td>
<td>±1.0</td>
<td>±1.0</td>
<td>±1.0</td>
<td>μA</td>
<td></td>
</tr>
</tbody>
</table>

| **RECEIVER** |     |     |     |      |                          |
| Differential Input Threshold Voltage, V<sub>TH</sub> | –0.2 | +0.2 | V | –7 V ≤ V<sub>CM</sub> ≤ +12 V |
| Input Voltage Hysteresis, ΔV<sub>TH</sub> | 70 | 70 | mV | V<sub>CM</sub> = 0 V |
| Input Current (A, B) | 1 | 1 | mA | V<sub>IN</sub> = +12 V |
| CMOS Input Logic Threshold Low, V<sub>INL</sub> | 0.8 | 0.8 | V | V<sub>IN</sub> = –7 V |
| CMOS Input Logic Threshold High, V<sub>INH</sub> | 2.0 | 2.0 | 2.0 | V | |
| Logic Enable Input Current (RE) | ±1 | ±1 | μA | I<sub>OUT</sub> = +4.0 mA |
| CMOS Output Voltage Low, V<sub>OL</sub> | 0.4 | 0.4 | V | I<sub>OUT</sub> = –4.0 mA |
| CMOS Output Voltage High, V<sub>OH</sub> | 4.0 | 4.0 | V | V<sub>OUT</sub> = GND or V<sub>CC</sub> |
| Short-Circuit Output Current | 7 | 85 | mA | 0.4 V ≤ V<sub>OUT</sub> ≤ 2.4 V |
| Three-State Output Leakage Current | ±1.0 | ±1.0 | μA | |

| **POWER SUPPLY CURRENT** |     |     |     |      |                          |
| I<sub>CC</sub> (Outputs Enabled) | 1.0 | 2.2 | mA | Digital Inputs = GND or V<sub>CC</sub> |
| I<sub>CC</sub> (Outputs Disabled) | 0.6 | 1.0 | mA | Digital Inputs = GND or V<sub>CC</sub> |

Specifications subject to change without notice.

### TIMING SPECIFICATIONS

*(V<sub>CC</sub> = 5 V ± 5%. All specifications T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)*

<table>
<thead>
<tr>
<th>Parameter</th>
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<tr>
<td><strong>DRIVER</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Propagation Delay Input to Output t&lt;sub&gt;PLHL&lt;/sub&gt;, t&lt;sub&gt;PHL&lt;/sub&gt;</td>
<td>10</td>
<td>15</td>
<td>10</td>
<td>ns</td>
<td>R&lt;sub&gt;D&lt;/sub&gt; = 54 Ω, C&lt;sub&gt;L1&lt;/sub&gt; = C&lt;sub&gt;L2&lt;/sub&gt; = 100 pF, Test Circuit 3</td>
</tr>
<tr>
<td>Driver O/P to O/P t&lt;sub&gt;TSKREW&lt;/sub&gt;</td>
<td>1</td>
<td>5</td>
<td>1</td>
<td>ns</td>
<td>R&lt;sub&gt;D&lt;/sub&gt; = 54 Ω, C&lt;sub&gt;L1&lt;/sub&gt; = C&lt;sub&gt;L2&lt;/sub&gt; = 100 pF, Test Circuit 3</td>
</tr>
<tr>
<td>Driver Rise/Fall Time t&lt;sub&gt;R&lt;/sub&gt;, t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>8</td>
<td>15</td>
<td>8</td>
<td>ns</td>
<td>R&lt;sub&gt;D&lt;/sub&gt; = 54 Ω, C&lt;sub&gt;L1&lt;/sub&gt; = C&lt;sub&gt;L2&lt;/sub&gt; = 100 pF, Test Circuit 3</td>
</tr>
<tr>
<td>Driver Enable to Output Valid</td>
<td>10</td>
<td>25</td>
<td>10</td>
<td>ns</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 110 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Test Circuit 4</td>
</tr>
<tr>
<td>Driver Disable Timing</td>
<td>10</td>
<td>25</td>
<td>10</td>
<td>ns</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 110 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Test Circuit 4</td>
</tr>
<tr>
<td>Matched Enable Switching</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>ns</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 110 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Test Circuit 4*</td>
</tr>
<tr>
<td>Matched Disable Switching</td>
<td>0</td>
<td>2</td>
<td>0</td>
<td>ns</td>
<td>R&lt;sub&gt;L&lt;/sub&gt; = 110 Ω, C&lt;sub&gt;L&lt;/sub&gt; = 50 pF, Test Circuit 4*</td>
</tr>
</tbody>
</table>

| **RECEIVER** |     |     |     |      |                          |
| Propagation Delay Input to Output t<sub>PLHL</sub>, t<sub>PHL</sub> | 8 | 15 | 30 | ns | C<sub>L</sub> = 15 pF, Test Circuit 5 |
| Skew t<sub>PLHL</sub>–t<sub>PHL</sub> | 5 | 5 | ns | C<sub>L</sub> = 15 pF, Test Circuit 5 |
| Receiver Enable t<sub>EN1</sub> | 5 | 20 | 5 | ns | C<sub>L</sub> = 15 pF, R<sub>L</sub> = 1 kΩ, Test Circuit 6 |
| Receiver Disable t<sub>EN2</sub> | 5 | 20 | 5 | ns | C<sub>L</sub> = 15 pF, R<sub>L</sub> = 1 kΩ, Test Circuit 6 |
| TX Pulse Width Distortion | 1 | ns | 1 | ns | |
| RX Pulse Width Distortion | 1 | ns | 1 | ns | |

*Guaranteed by characterization.

Specifications subject to change without notice.
**ABSOLUTE MAXIMUM RATINGS**

*(TA = 25°C, unless otherwise noted.)*

V\text{CC} .................................................. –0.3 V to +7 V

Inputs

- Driver Input (DI) .................. –0.3 V to V\text{CC} + 0.3 V
- Control Inputs (DE, RE) .......... –0.3 V to V\text{CC} + 0.3 V
- Receiver Inputs (A, B) ........... –9 V to +14 V

Outputs

- Driver Outputs (A, B) .............. –9 V to +14 V
- Receiver Output ......................... –0.5 V to V\text{CC} + 0.5 V

Power Dissipation

- 8-Lead MSOP ......................... 900 mW
- θJA, Thermal Impedance ............. 206°C/W

- 8-Lead PDIP .......................... 500 mW
- θJA, Thermal Impedance ............. 130°C/W

- 8-Lead SOIC ......................... 450 mW
- θJA, Thermal Impedance ............. 170°C/W

Operating Temperature Range

- Commercial (J Version) ........... 0°C to 70°C
- Industrial (A Version) ............. –40°C to +85°C
- Storage Temperature Range ........ –65°C to +150°C

Lead Temperature (Soldering, 10 sec) ............. 300°C

- Vapor Phase (60 sec) ............. 215°C
- Infrared (15 sec) .................. 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.*

**PIN FUNCTION DESCRIPTIONS**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RO</td>
<td>Receiver Output. When enabled if A &gt; B by 200 mV, then RO = High. If A &lt; B by 200 mV, then RO = Low.</td>
</tr>
<tr>
<td>2</td>
<td>RE</td>
<td>Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state.</td>
</tr>
<tr>
<td>3</td>
<td>DE</td>
<td>Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state.</td>
</tr>
<tr>
<td>4</td>
<td>DI</td>
<td>Driver Input. When the driver is enabled, a logic low on DI forces A low and B high while a logic high on DI forces A high and B low.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground Connection, 0 V.</td>
</tr>
<tr>
<td>6</td>
<td>A</td>
<td>Noninverting Receiver Input A/Driver Output A.</td>
</tr>
<tr>
<td>7</td>
<td>B</td>
<td>Inverting Receiver Input B/Driver Output B</td>
</tr>
<tr>
<td>8</td>
<td>V\text{CC}</td>
<td>Power Supply, 5 V ± 5%.</td>
</tr>
</tbody>
</table>

**PIN CONFIGURATION**

**Table I. Transmitting**

<table>
<thead>
<tr>
<th>DE</th>
<th>DI</th>
<th>B</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>Z</td>
<td>Z</td>
</tr>
</tbody>
</table>

**Table II. Receiving**

<table>
<thead>
<tr>
<th>RE</th>
<th>Inputs A-B</th>
<th>Outputs RO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>≥ +0.2 V</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>≤ –0.2 V</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>Inputs Open</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>Z</td>
</tr>
</tbody>
</table>

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1485 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.
ADM1485

Test Circuits

Test Circuit 1. Driver Voltage Measurement

Test Circuit 2. Driver Voltage Measurement

Test Circuit 3. Driver Propagation Delay

Test Circuit 4. Driver Enable/Disable

Test Circuit 5. Receiver Propagation Delay

Test Circuit 6. Receiver Enable/Disable

Switching Characteristics

Figure 1. Driver Propagation Delay, Rise/Fall Timing

Figure 2. Driver Enable/Disable Timing

Figure 3. Receiver Propagation Delay

Figure 4. Receiver Enable/Disable Timing
Typical Performance Characteristics–ADM1485

TPC 1. Output Current vs. Receiver Output Low Voltage

TPC 2. Output Current vs. Receiver Output High Voltage

TPC 3. Receiver Output High Voltage vs. Temperature

TPC 4. Receiver Output Low Voltage vs. Temperature

TPC 5. Output Current vs. Driver Differential Output Voltage

TPC 6. Driver Differential Output Voltage vs. Temperature, $R_L = 26.8 \, \Omega$
ADM1485

TPC 7. Output Current vs. Driver Output Low Voltage

TPC 8. Output Current vs. Driver Output High Voltage

TPC 9. Supply Current vs. Temperature

TPC 10. Rx Skew vs. Temperature

TPC 11. Tx Skew vs. Temperature

TPC 12. Tx Pulse Width Distortion
TPC 13. Unloaded Driver Differential Outputs

TPC 14. Loaded Driver Differential Outputs

TPC 15. Driver/Receiver Propagation Delays Low to High

TPC 16. Driver/Receiver Propagation Delays High to Low

TPC 17. Driver Output at 30 Mbps
As with any transmission line, it is important that reflections are minimized. This can be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

**Figure 5. Typical RS-485 Network**

**Thermal Shutdown**

The ADM1485 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C.

**Propagation Delay**

The ADM1485 features very low propagation delay, ensuring maximum baud rate operation. The driver is well balanced, ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

**Receiver Open-Circuit Fail-Safe**

The receiver input includes a fail-safe feature that guarantees a logic high on the receiver when the inputs are open circuit or floating.
OUTLINE DIMENSIONS

Figure 6. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

Figure 7. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

COMPLIANT TO JEDEC STANDARDS MS-012-AA
COMPLIANT TO JEDEC STANDARDS MO-187-AA
ADM1485

Figure 8. 8-Lead Plastic Dual In-Line Package (PDIP)
Narrow Body
(N-8)

Dimensions shown in inches and (millimeters)

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Brand</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADM1485JNZ</td>
<td>0°C to 70°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485JRZ</td>
<td>0°C to 70°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485JR-REEL</td>
<td>0°C to 70°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485JNZ-REEL</td>
<td>0°C to 70°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485ANZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485ARMZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead MSOP</td>
<td>RM-8</td>
<td>M42</td>
</tr>
<tr>
<td>ADM1485ARMZ-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead MSOP</td>
<td>RM-8</td>
<td>M42</td>
</tr>
<tr>
<td>ADM1485ARMZ-REEL7</td>
<td>−40°C to +85°C</td>
<td>8-Lead MSOP</td>
<td>RM-8</td>
<td>M42</td>
</tr>
<tr>
<td>ADM1485ARZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485ARZ-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485ARZ-REEL7</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
<td></td>
</tr>
<tr>
<td>ADM1485JCHIPS</td>
<td></td>
<td></td>
<td></td>
<td>Die</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.
REVISION HISTORY

8/12—Rev. E to Rev. F

Changed Data Rates of Up to 5 Mbps to Typical Data Rates of 30 Mbps.......................................................... 1
Updated Outline Dimensions .................................................. 9
Changes to Ordering Guide .................................................. 10

9/03—Data Sheet changed from REV. D to REV. E.

Change to SPECIFICATIONS................................................... 2
Changes to ORDERING GUIDE .................................................. 3
Updated OUTLINE DIMENSIONS .............................................. 9

7/03—Data Sheet changed from REV. C to REV. D.

Changes to SPECIFICATIONS .................................................. 2
Changes to ABSOLUTE MAXIMUM RATINGS .......................... 3
Updated ORDERING GUIDE...................................................... 3

1/03—Data Sheet changed from REV. B to REV. C.

Change to SPECIFICATIONS.................................................. 2
Change to ORDERING GUIDE.................................................. 3

12/02—Data Sheet changed from REV. A to REV. B.

Deleted Q-8 Package.......................................................... Universal
Edits to FEATURES .......................................................... 1
Edits to GENERAL DESCRIPTION ......................................... 1
Edits, additions to SPECIFICATIONS ..................................... 2
Edits, additions to ABSOLUTE MAXIMUM RATINGS ............ 3
Additions to ORDERING GUIDE ............................................ 3
TPCs updated and reformatted ............................................... 5
Addition of 8-Lead MSOP Package ........................................ 9
Update to OUTLINE DIMENSIONS ........................................ 9