STF260N4F7



N-channel 40 V, 1.95 mΩ typ., 90 A, STripFET™ F7 Power MOSFET in a TO-220FP package

Datasheet - preliminary data

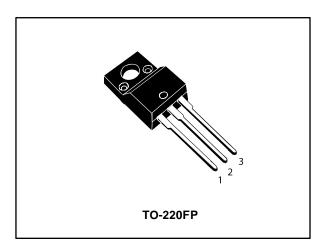
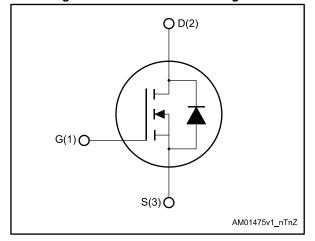


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STF260N4F7	40 V	$2.5~\text{m}\Omega$	35 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low onstate resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF260N4F7	260N4F7	TO-220FP	Tube

Contents STF260N4F7

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STF260N4F7 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T _C = 25 °C	90	Α
I _D	Drain current (continuous) at T _C = 100 °C	64	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	360	Α
P _{TOT}	Total dissipation at $T_C = 25$ °C	35	W
V _{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; T _C = 25 °C)		kV
T _{stg}	Storage temperature	-55 to 175	°C
TJ	Operation junction temperature	-55 10 175	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	4.29	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	°C/W

⁽¹⁾Pulse width limited by safe operating area

Electrical characteristics STF260N4F7

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Uni t
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V
	Zero gate voltage	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}$			1	μΑ
I _{DSS}	I _{DSS} drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 40 \text{ V}$ $T_C = 125 \text{ °C}$			100	μΑ
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = + 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2		4	V
R _{DS(on)}	Static drain-source on- resistance	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$		1.95	2.5	mΩ

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		ı	5640	1	pF
Coss	Output capacitance	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	1	2370	ı	pF
C _{rss}	Reverse transfer capacitance	V63 = 0 V, VB3 = 20 V, 1 = 1 Will 2	-	34	-	pF
Qg	Total gate charge	V _{DD} = 20 V, I _D = 120 A,	-	67	-	nC
Q_gs	Gate-source charge	V _{GS} = 10 V	ı	31	1	nC
Q_{gd}	Gate-drain charge	(see Figure 3: "Test circuit for gate charge behavior")	-	10	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 20 \text{ V}, I_D = 60 \text{ A},$	-	30	-	ns
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	-	21	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 2: "Test circuit for resistive load switching times" and Figure 7: "Switching time waveform"	-	42	-	ns
t _f	Fall time	and wavelenn	-	13		ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 120 A	-	-	1.1	٧
t _{rr}	Reverse recovery time		-	68		ns
Qrr	Reverse recovery charge	I _{SD} = 120 A, di/dt = 100 A/μs V _{DD} = 32 V (see <i>Figure 4: "Test circuit for inductive load switching and diode</i>	-	98		nC
I _{RRM}	Reverse recovery current	recovery times")	-	3		Α

Notes

 $^{^{(1)}\}text{Pulsed:}$ pulse duration = 300 $\mu\text{s,}$ duty cycle 1.5%

Test circuits STF260N4F7

3 **Test circuits**

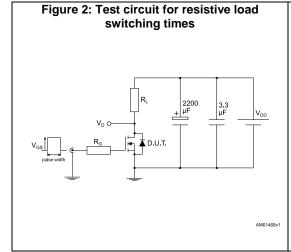


Figure 3: Test circuit for gate charge behavior ⊥ 100 nF I_G= CONST 100 Ω 2.7 kΩ - 1 47 kΩ

Figure 4: Test circuit for inductive load switching and diode recovery times

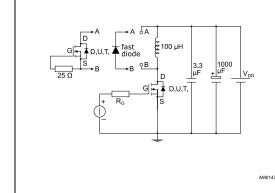


Figure 5: Unclamped inductive load test circuit

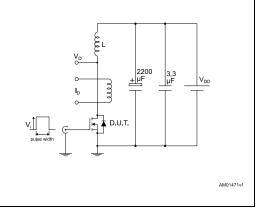


Figure 6: Unclamped inductive waveform

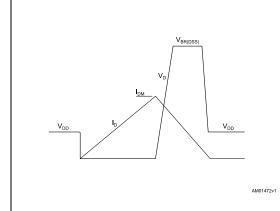
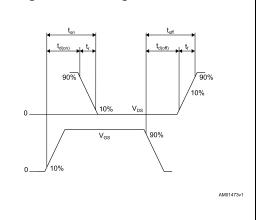


Figure 7: Switching time waveform



STF260N4F7 Package information

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 8: TO-220FP package outline

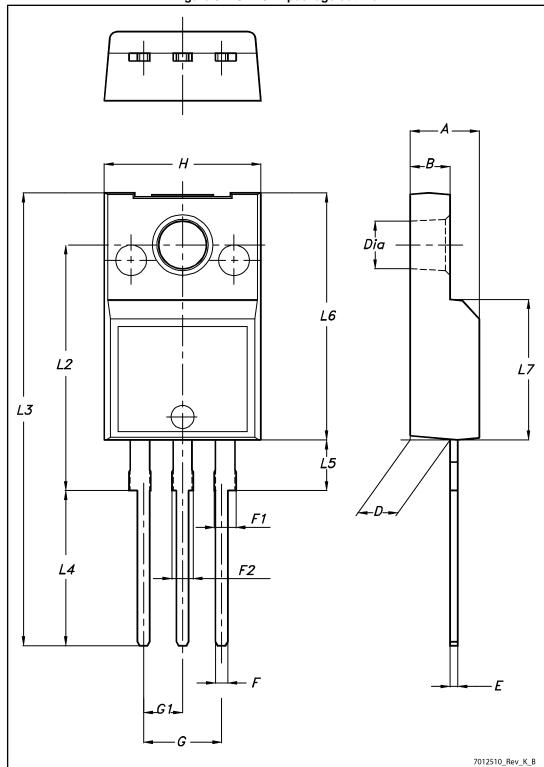


Table 8: TO-220FP package mechanical data

Dim	mm				
Dim.	Min.	Тур.	Max.		
А	4.4		4.6		
В	2.5		2.7		
D	2.5		2.75		
Е	0.45		0.7		
F	0.75		1		
F1	1.15		1.70		
F2	1.15		1.70		
G	4.95		5.2		
G1	2.4		2.7		
Н	10		10.4		
L2		16			
L3	28.6		30.6		
L4	9.8		10.6		
L5	2.9		3.6		
L6	15.9		16.4		
L7	9		9.3		
Dia	3		3.2		

Revision history STF260N4F7

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
13-Oct-2015	1	Initial release.

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