STL80N10WF7

N-channel 100 V, 9.4 mΩ typ., 80 A, STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

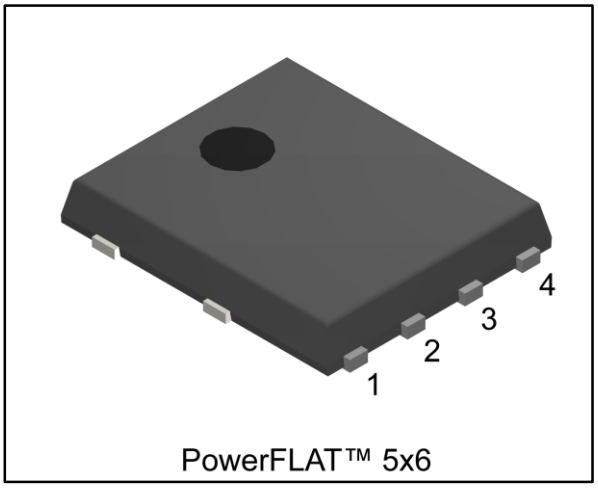
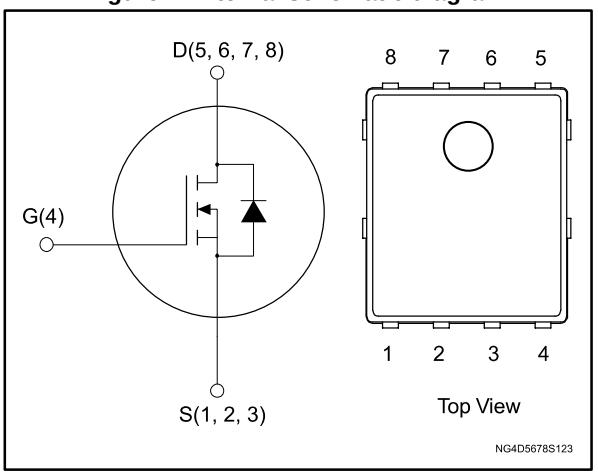


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STL80N10WF7	100 V	11 mΩ	80 A	150 W

- Best in class SOA capability
- High current surge capability
- Extremely low on-resistance

Applications

- Hot-swap
- Electronic fuse
- Load switch

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure able to provide a wider SOA capability in conjunction with a very low on-state resistance. The resulting MOSFET ensures the best trade-off between linear mode operation and switching operation.

Table 1: Device summary

Order code	Marking	Package	Packing
STL80N10WF7	80N10WF7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_c= 25 °C	80	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	59	A
I_{DM} (1)(2)	Drain current (pulsed)	320	A
I_D (3)	Drain current (continuous) at T_{pcb} = 25 °C	15	A
I_D (3)	Drain current (continuous) at T_{pcb} = 100 °C	11	A
I_{DM} (3)(2)	Drain current (pulsed)	60	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	150	W
P_{TOT} (3)	Total dissipation at T_{pcb} = 25 °C	4.8	W
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

Notes:

(1)This value is rated according to $R_{thj\text{-}c}$.

(2)Pulse width limited by safe operating area.

(3)This value is rated according to $R_{thj\text{-}pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.0	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W

Notes:

(1)When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 100 V			1	µA
		V_{GS} = 0 V, V_{DS} = 100 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		9.4	11.0	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	-	2190	-	pF
C_{oss}	Output capacitance		-	1350	-	pF
C_{rss}	Reverse transfer capacitance		-	65	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 15 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	36	-	nC
Q_{gs}	Gate-source charge		-	13	-	nC
Q_{gd}	Gate-drain charge		-	9.4	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 7.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	21.4	-	ns
t_r	Rise time		-	13	-	ns
$t_{d(off)}$	Turn-off delay time		-	35.2	-	ns
t_f	Fall time		-	16.2	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 15 A	-	-	1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 15 A, di/dt = 100 A/µs V_{DD} = 80 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	37		ns
Q_{rr}	Reverse recovery charge		-	125		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

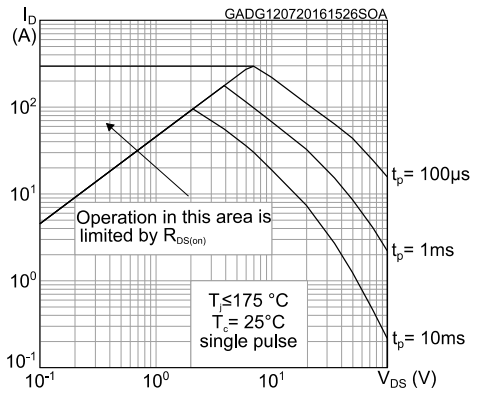


Figure 3: Thermal impedance

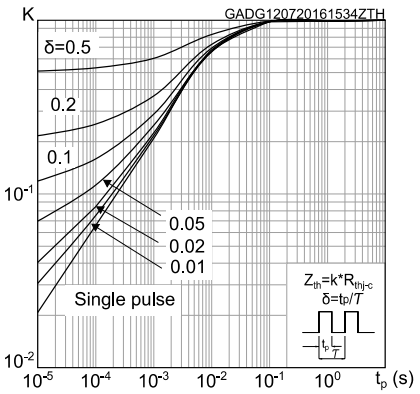


Figure 4: Output characteristics

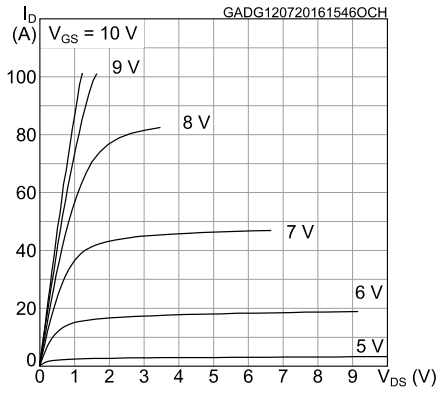


Figure 5: Transfer characteristics

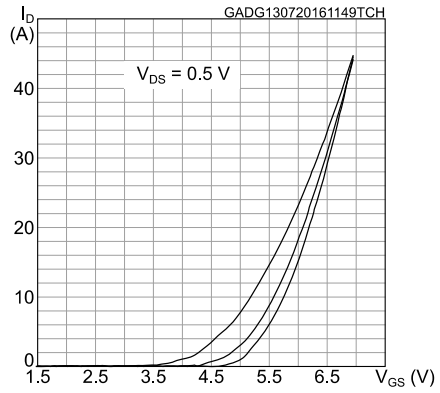


Figure 6: Gate charge vs gate-source voltage

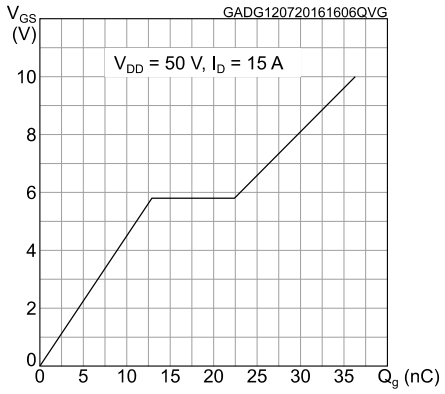


Figure 7: Static drain-source on-resistance

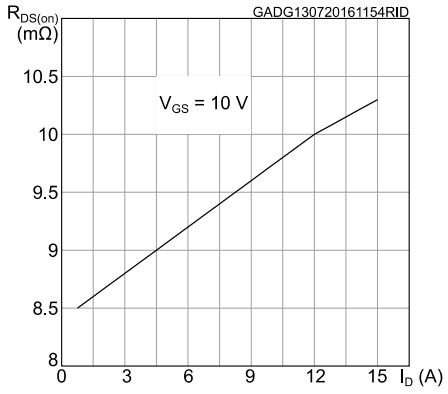


Figure 8: Capacitance variations

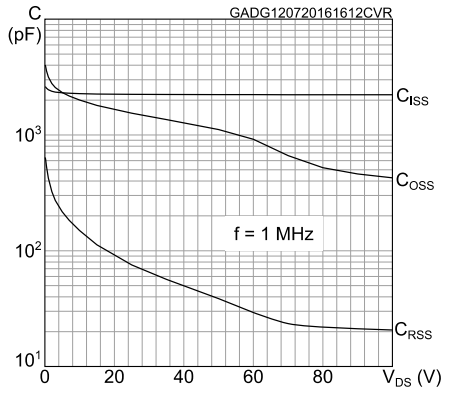


Figure 9: Normalized gate threshold voltage vs temperature

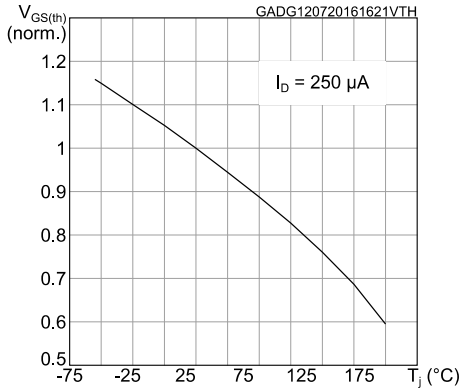


Figure 10: Normalized on-resistance vs temperature

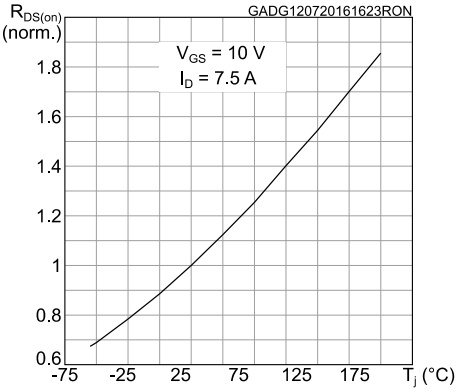


Figure 11: Normalized V(BR)DSS vs temperature

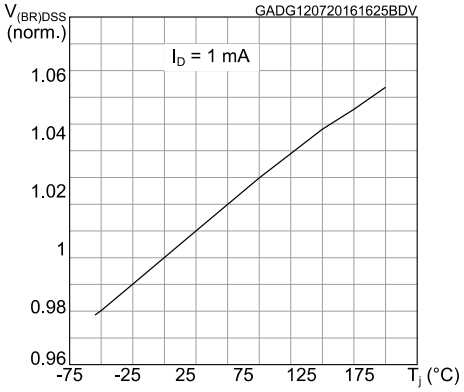
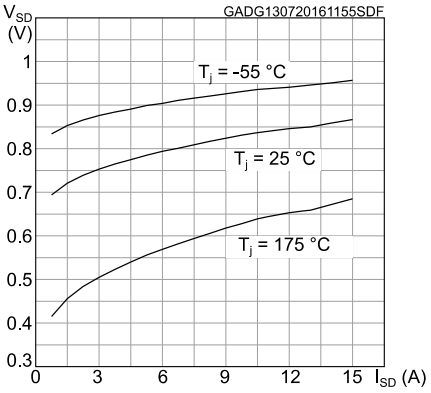


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

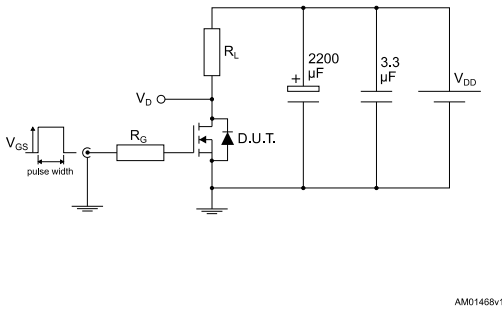


Figure 14: Test circuit for gate charge behavior

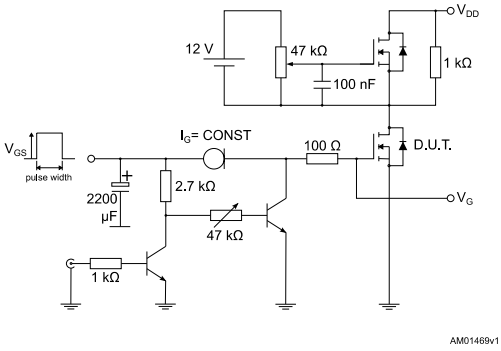


Figure 15: Test circuit for inductive load switching and diode recovery times

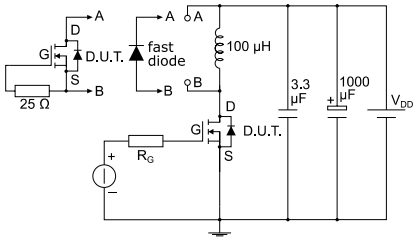


Figure 16: Unclamped inductive load test circuit

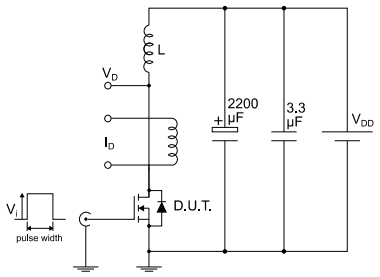


Figure 17: Unclamped inductive waveform

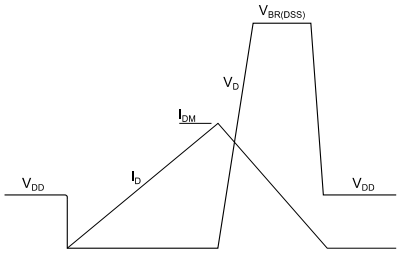
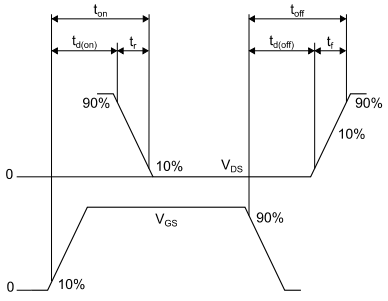


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 19: PowerFLAT™ 5x6 type C package outline

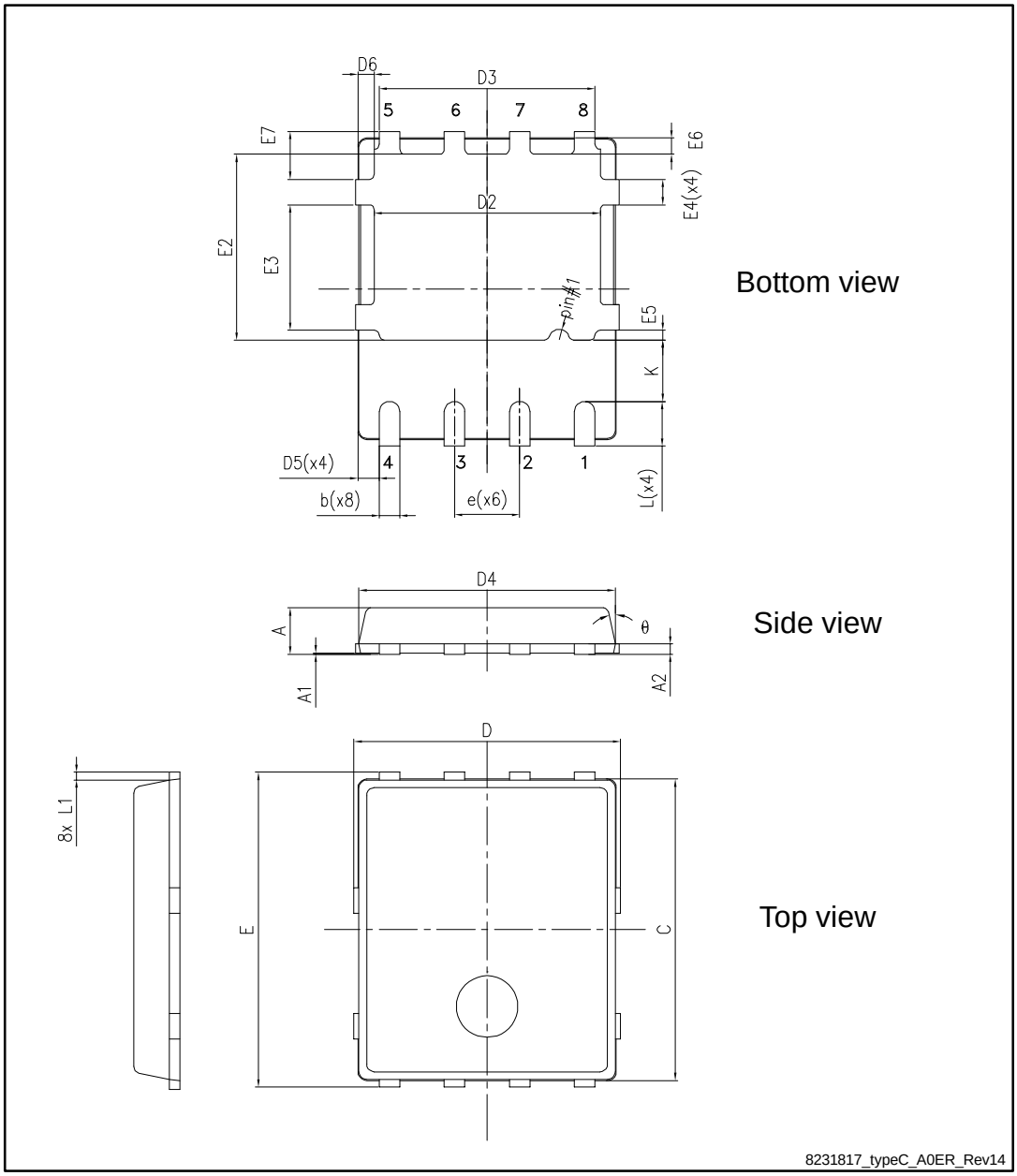
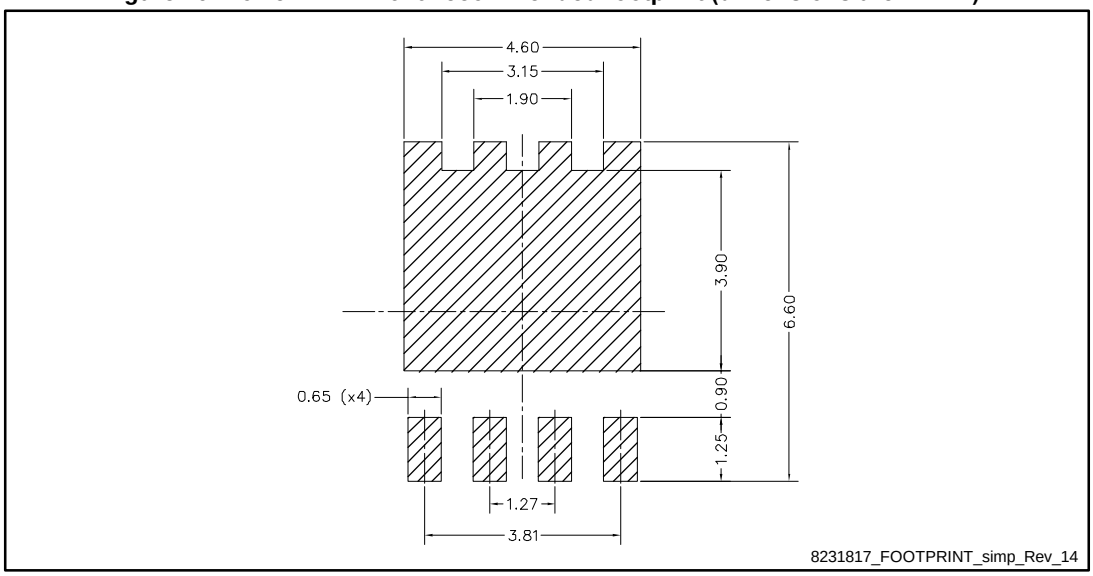


Table 8: PowerFLAT™ 5x6 type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 type C packing information

Figure 21: PowerFLAT™ 5x6 tape (dimensions are in mm)

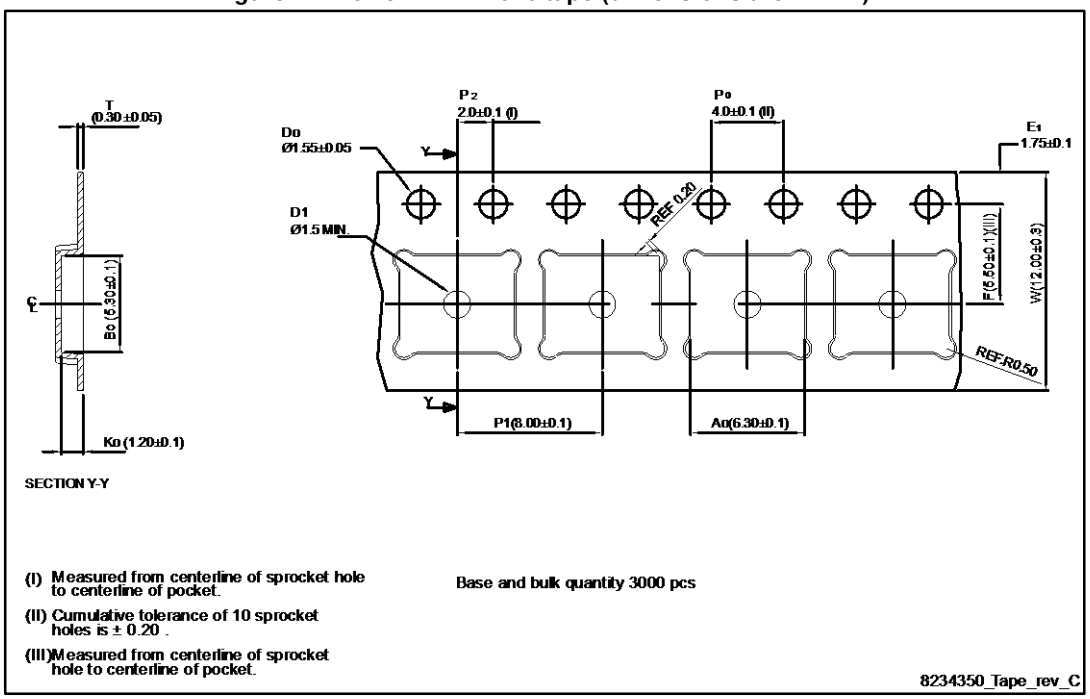


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

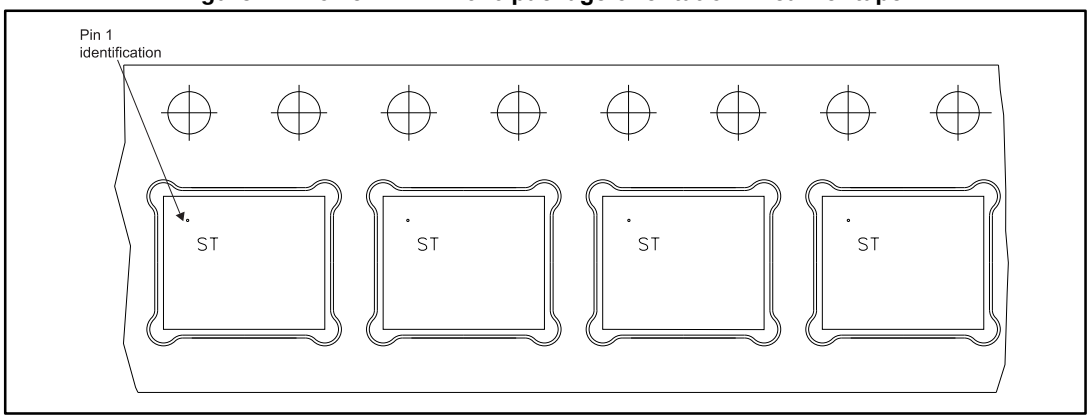
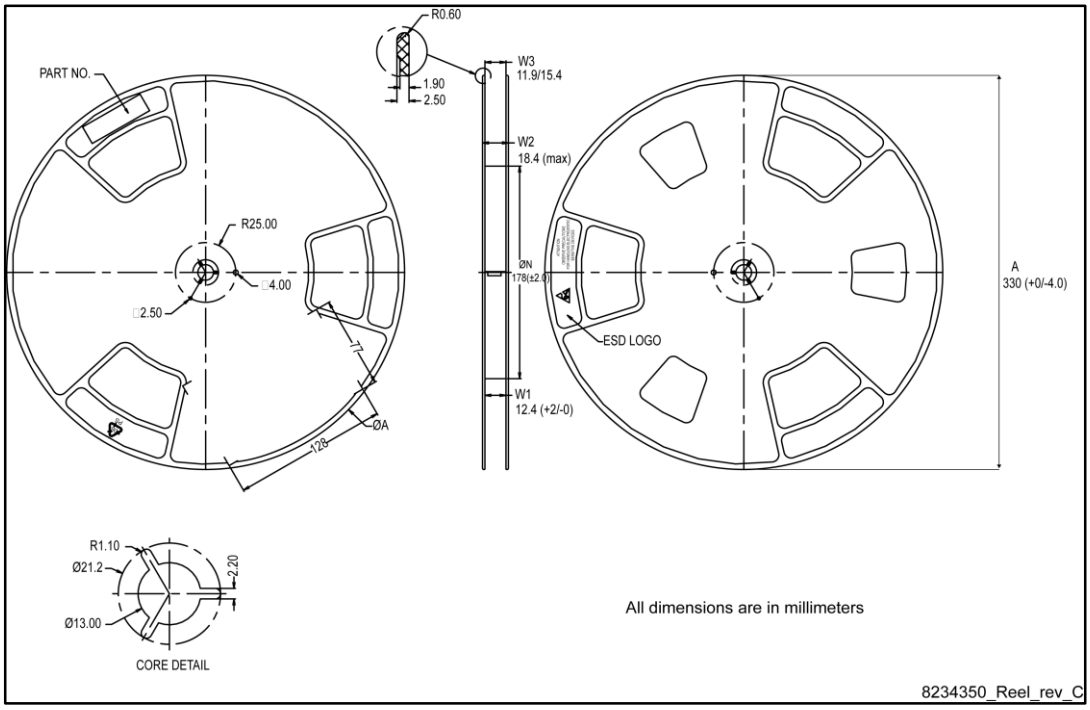


Figure 23: PowerFLAT™ 5x6 reel



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
12-Jul-2016	1	Initial release.

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