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FAIRCHILD SEMICONDUCTOR®

February 2008

# MM74HC14
# Hex Inverting Schmitt Trigger

## Features

- Typical propagation delay: 13ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20µA maximum (74HC Series)
- Low input current: 1µA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}$ = 4.5V

## General Description

The MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

## Ordering Information

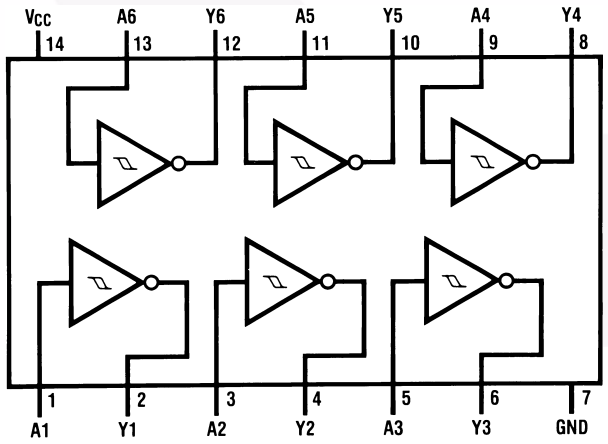
| Order Number | Package Number | Package Description |
|---|---|---|
| MM74HC14M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC14SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC14MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC14N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

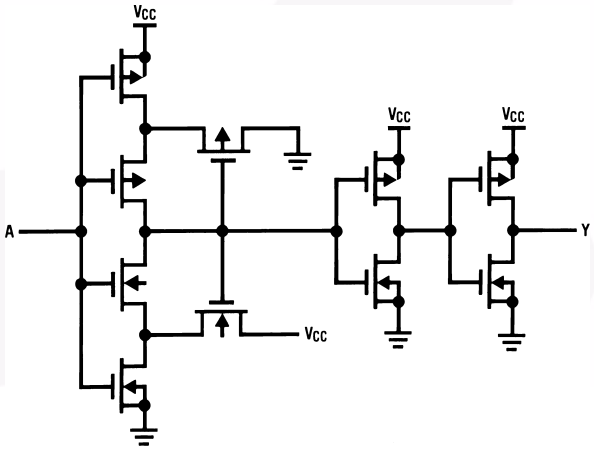
## Connection Diagram

**Pin Assignments for DIP, SOIC, SOP and TSSOP**




**Top View**

## Logic Diagram

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## Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.5 to +7.0V |
| $V_{IN}$ | DC Input Voltage | –1.5 to $V_{CC}$+1.5V |
| $V_{OUT}$ | DC Output Voltage | –0.5 to $V_{CC}$+0.5V |
| $I_{IK}$, $I_{OK}$ | Clamp Diode Current | ±20mA |
| $I_{OUT}$ | DC Output Current, per pin | ±25mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current, per pin | ±50mA |
| $T_{STG}$ | Storage Temperature Range | –65°C to +150°C |
| $P_D$ | Power Dissipation<br>Note 2 | 600mW |
| | S.O. Package only | 500mW |
| $T_L$ | Lead Temperature (Soldering 10 seconds) | 260°C |

**Notes:**

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 | 6 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | –55 | +125 | °C |

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## DC Electrical Characteristics[3]

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = 25°C | $T_A$ = –40°C to 85°C | $T_A$ = –55°C to 125°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | | |
| $V_{T+}$ | Positive Going Threshold Voltage | 2.0 | Minimum | 1.2 | 1.0 | 1.0 | 1.0 | V |
| | | 4.5 | | 2.7 | 2.0 | 2.0 | 2.0 | |
| | | 6.0 | | 3.2 | 3.0 | 3.0 | 3.0 | |
| | | 2.0 | Maximum | 1.2 | 1.5 | 1.5 | 1.5 | |
| | | 4.5 | | 2.7 | 3.15 | 3.15 | 3.15 | |
| | | 6.0 | | 3.2 | 4.2 | 4.2 | 4.2 | |
| $V_{T-}$ | Negative Going Threshold Voltage | 2.0 | Minimum | 0.7 | 0.3 | 0.3 | 0.3 | V |
| | | 4.5 | | 1.8 | 0.9 | 0.9 | 0.9 | |
| | | 6.0 | | 2.2 | 1.2 | 1.2 | 1.2 | |
| | | 2.0 | Maximum | 0.7 | 1.0 | 1.0 | 1.0 | |
| | | 4.5 | | 1.8 | 2.2 | 2.2 | 2.2 | |
| | | 6.0 | | 2.2 | 3.0 | 3.0 | 3.0 | |
| $V_H$ | Hysteresis Voltage | 2.0 | Minimum | 0.5 | 0.2 | 0.2 | 0.2 | V |
| | | 4.5 | | 0.9 | 0.4 | 0.4 | 0.4 | |
| | | 6.0 | | 1.0 | 0.5 | 0.5 | 0.5 | |
| | | 2.0 | Maximum | 0.5 | 1.0 | 1.0 | 1.0 | |
| | | 4.5 | | 0.9 | 1.4 | 1.4 | 1.4 | |
| | | 6.0 | | 1.0 | 1.5 | 1.5 | 1.5 | |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | 2.0 | $V_{IN} = V_{IL}$, $\|I_{OUT}\| = 20\mu A$ | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | 4.5 | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | 6.0 | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | 4.5 | $V_{IN} = V_{IL}$, $\|I_{OUT}\| = 4.0mA$ | 4.2 | 3.98 | 3.84 | 3.7 | |
| | | 6.0 | $V_{IN} = V_{IL}$, $\|I_{OUT}\| = 5.2mA$ | 5.7 | 5.48 | 5.34 | 5.2 | |
| $V_{OL}$ | Maximum LOW Level Output Voltage | 2.0 | $V_{IN} = V_{IH}$, $\|I_{OUT}\| = 20\mu A$ | 0 | 0.1 | 0.1 | 0.1 | V |
| | | 4.5 | | 0 | 0.1 | 0.1 | 0.1 | |
| | | 6.0 | | 0 | 0.1 | 0.1 | 0.1 | |
| | | 4.5 | $V_{IN} = V_{IH}$, $\|I_{OUT}\| = 4.0mA$ | 0.2 | 0.26 | 0.33 | 0.4 | |
| | | 6.0 | $V_{IN} = V_{IH}$, $\|I_{OUT}\| = 5.2mA$ | 0.2 | 0.26 | 0.33 | 0.4 | |
| $I_{IN}$ | Maximum Input Current | 6.0 | $V_{IN} = V_{CC}$ or GND | | ±0.1 | ±1.0 | ±1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current | 6.0 | $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$ | | 2.0 | 20 | 40 | µA |

**Note:**

3. For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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## AC Electrical Characteristics

$V_{CC}$ = 5V, $T_A$ = 25°C, $C_L$ = 15pF, $t_r = t_f$ = 6ns

| Symbol | Parameter | Conditions | Typ. | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | | 12 | 22 | ns |

## AC Electrical Characteristics

$V_{CC}$ = 2.0V to 6.0V, $C_L$ = 50pF, $t_r = t_f$ = 6ns (unless otherwise specified)

| Symbol | Parameter | $V_{CC}$ (V) | Conditions | $T_A$ = 25°C | $T_A$ = –40°C to 85°C | $T_A$ = –55°C to 125°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ. | Guaranteed Limits | | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | 2.0 | | 60 | 125 | 156 | 188 | ns |
| | | 4.5 | | 13 | 25 | 31 | 38 | |
| | | 6.0 | | 11 | 21 | 26 | 32 | |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise and Fall Time | 2.0 | | 30 | 75 | 95 | 110 | ns |
| | | 4.5 | | 8 | 15 | 19 | 22 | |
| | | 6.0 | | 7 | 13 | 16 | 19 | |
| $C_{PD}$ | Power Dissipation Capacitance(4) | | (per gate) | 27 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |

**Note:**

4. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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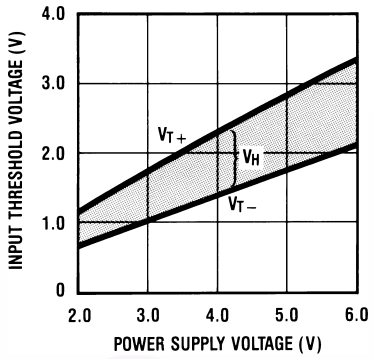
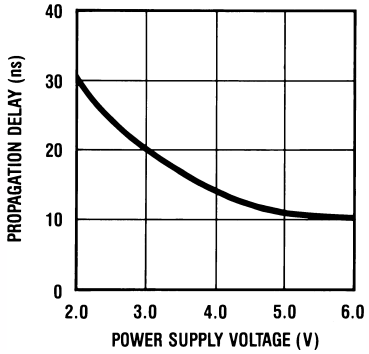
## Typical Performance Characteristics

**Input Threshold, $V_T+$, $V_T-$, vs Power Supply Voltage**

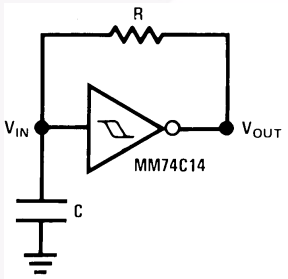



**Propagation Delay vs. Power Supply**



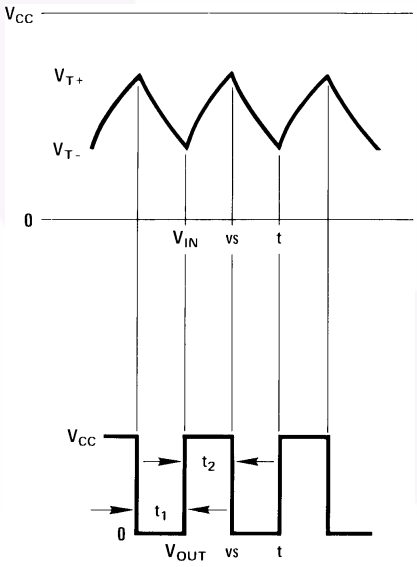

## Typical Applications

**Low Power Oscillator**




$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

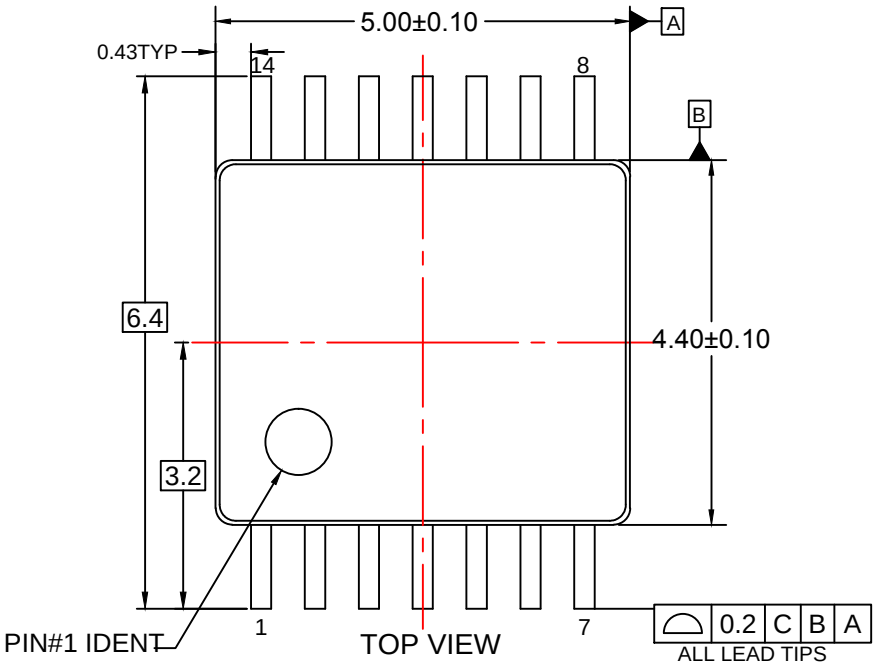
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$



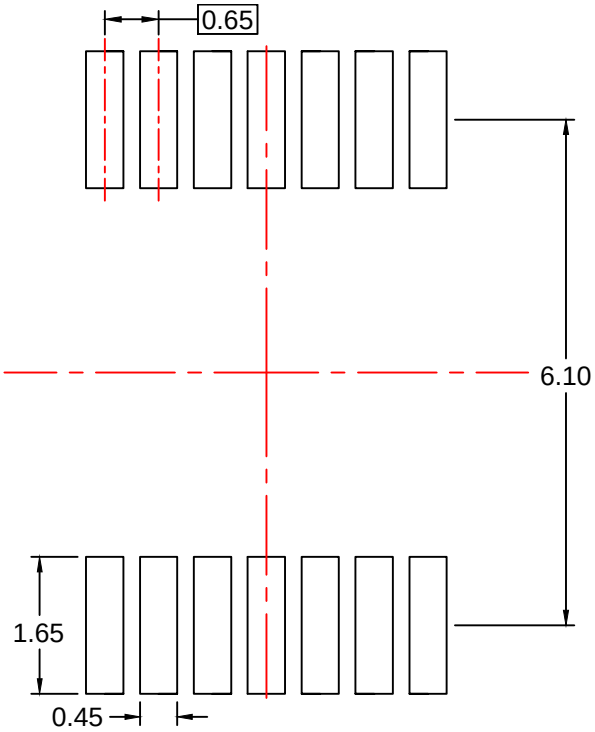

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}}$$

**Note:**

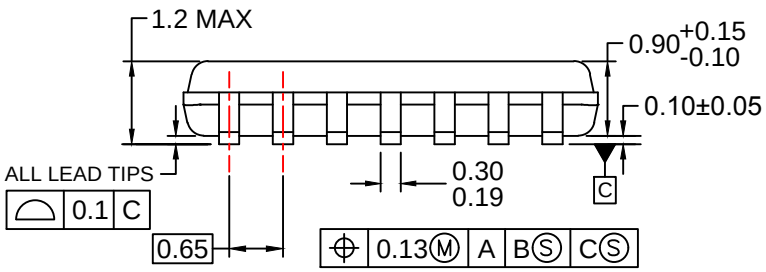
The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$



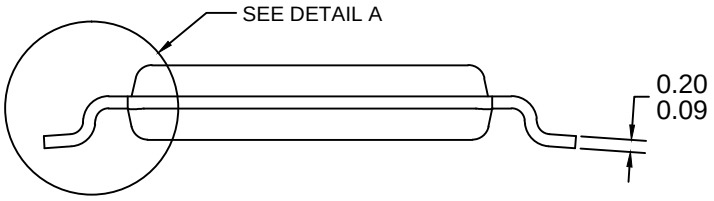

TOP VIEW

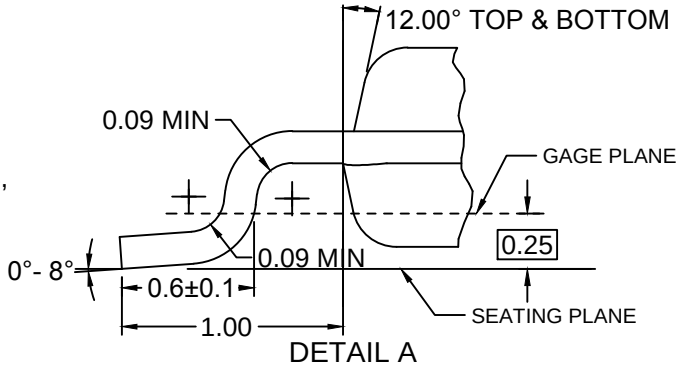



RECOMMENDED LAND PATTERN




FRONT VIEW




DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.

E. LANDPATTERN STANDARD: SOP65P640X110-14M.

F. DRAWING FILE NAME: MKT-MTC14rev7.

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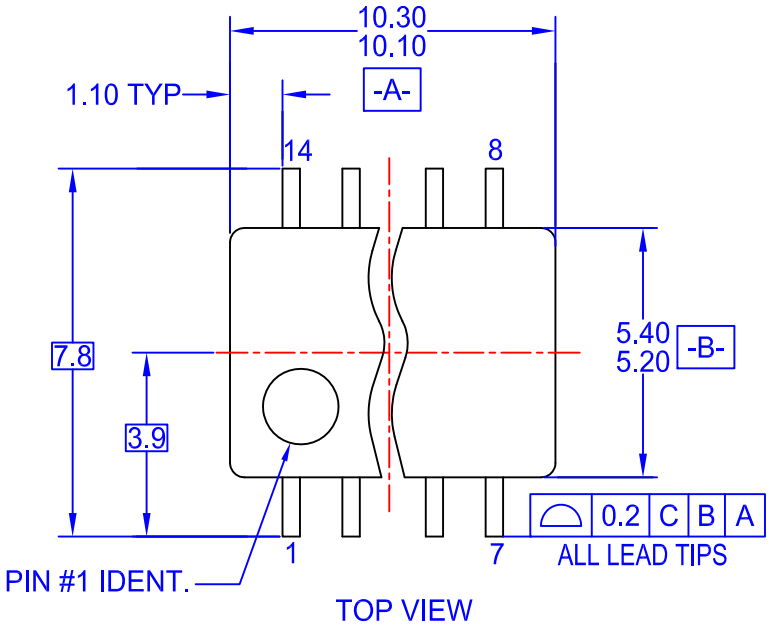
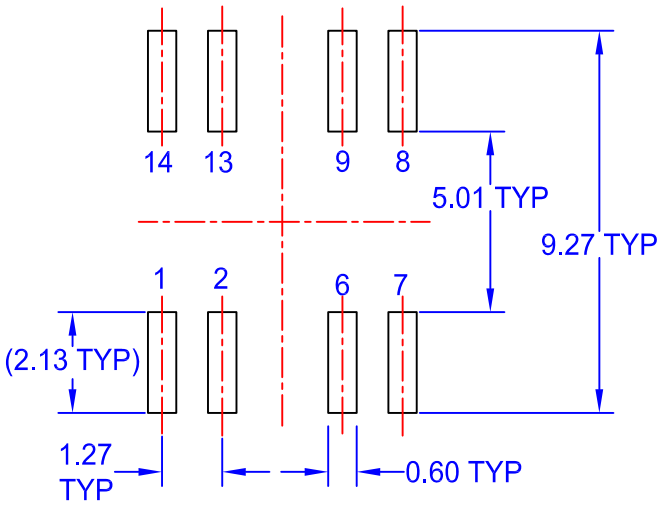
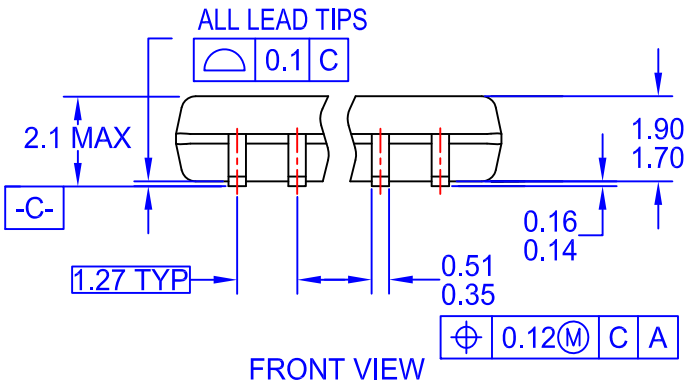


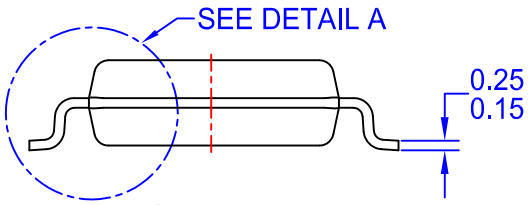

TOP VIEW



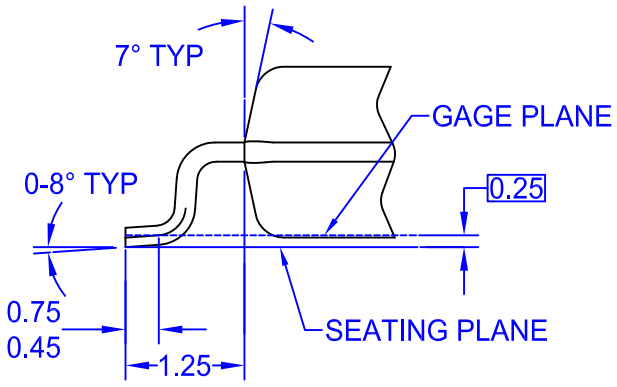

LAND PATTERN RECOMMENDATION




FRONT VIEW




SIDE VIEW




DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DRAWING FILENAME: MKT-M14Drev4.

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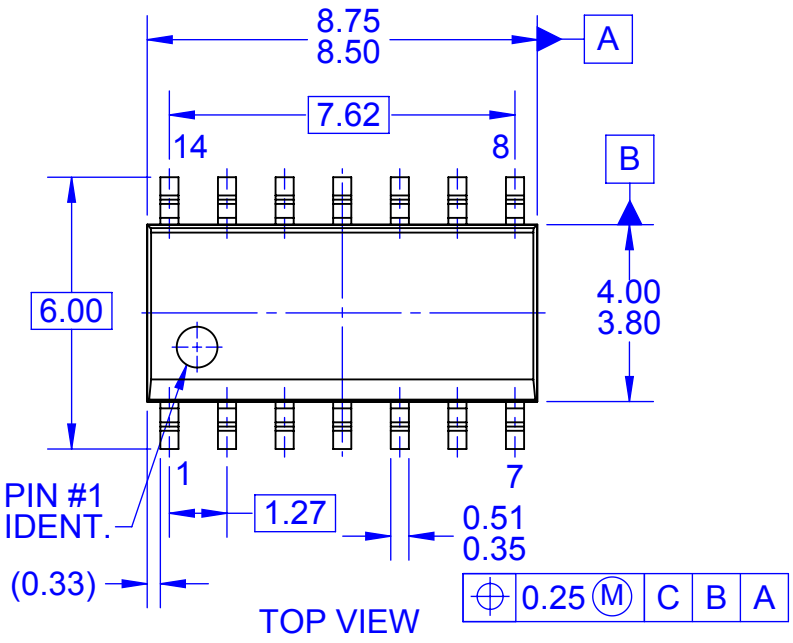
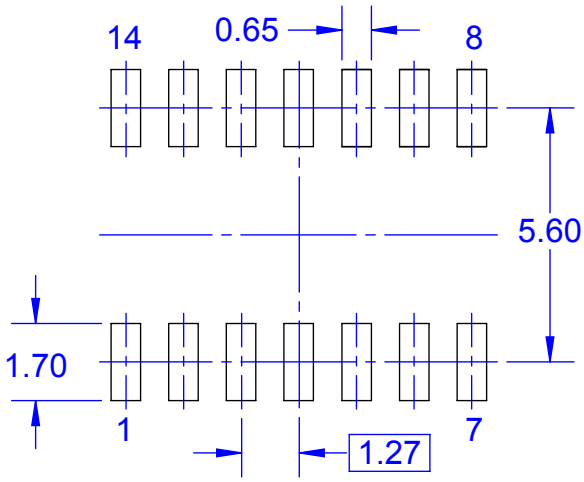
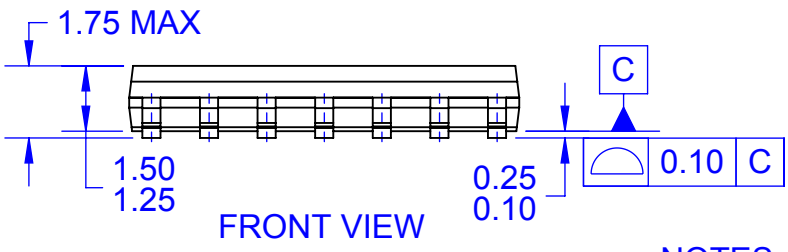


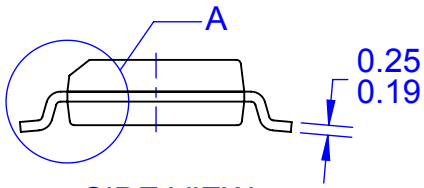

TOP VIEW




LAND PATTERN RECOMMENDATION



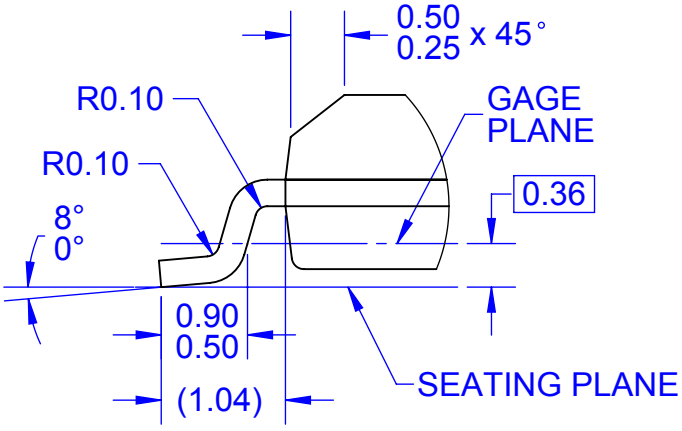

FRONT VIEW




SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145-14M
E. CONFORMS TO ASME Y14.5M, 2009
D. DRAWING FILENAME: MKT-M14Arev14




DETAIL A
SCALE 16 : 1

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