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June 2013

FSBH0F70A _F116, FSBH0170_F116, FSBH0270_F116, FSBH0370_F116 Green Mode Fairchild Power Switch (FPS™)

Features

- Brownout Protection with Hysteresis
- Built-In 5 ms Soft-Start Function
- Internal Avalanche-Rugged 700 V SenseFET
- Low Acoustic Noise During Light-Load Operation
- High-Voltage Startup
- Linearly Decreasing PWM Frequency to 18 KHz
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-Loop Protection
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Internal Auto-Restart Circuit (OVP, OTP)
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis
- VIN Pin for Pull-HIGH Latch Function and Pull-LOW Auto-Recovery Protection

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player, Printer, Facsimile, and Scanner
- Adapter for Camcorder

Description

The highly integrated FSBH-series consists of an integrated current-mode Pulse Width Modulator (PWM) and an avalanche-rugged 700 V SenseFET. It is specifically designed for high-performance offline Switched-Mode Power Supplies (SMPS) with minimal external components.

The integrated PWM controller features include a proprietary green-mode function that provides off-time modulation to linearly decrease the switching frequency at light-load conditions to minimize standby power consumption. To avoid acoustic-noise problems, the minimum PWM frequency is set above 18 kHz. This green-mode function enables the power supply to meet international power conservation requirements. The PWM controller is manufactured using the BiCMOS process to further reduce power consumption. The FSBH-series turns off some internal circuits to improve power saving when $V_{\rm FB}$ is lower than 1.6 V, which allows an operating current of only 2.5 mA.

The FSBH-series has built-in synchronized slope compensation to achieve stable peak-current-mode control. The proprietary external line compensation ensures constant output power limit over a wide AC input voltage range, from $90\ V_{AC}$ to $264\ V_{AC}$.

The FSBH-series provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety when an open-loop or output short occurs. PWM output is disabled until V_{DD} drops below the $V_{\text{TH-OLP}},$ then the controller starts up again. As long as V_{DD} exceeds 28 V, the internal OVP circuit is triggered.

Compared with a discrete MOSFET and controller or RCC switching converter solution, the FSBH-series reduces component count, design size, and weight; while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, such as in PC auxiliary power supplies.

Ordering Information

Part Number	SenseFET	VIN Pin (PIN #4)	Operating Temperature Range	Package	Packing Method
FSBH0F70ANY_F116	0.5 A 700 V	Not Available			
FSBH0170NY_F116	1.0 A 700 V		-40°C to +105°C	8-Pin, Dual In-Line	Tube
FSBH0270NY_F116	2.0 A 700 V	Enabled	-40 C to +105 C	Package (DIP)	Tube
FSBH0370NY_F116	3.0 A 700 V				

Typical Application Diagram

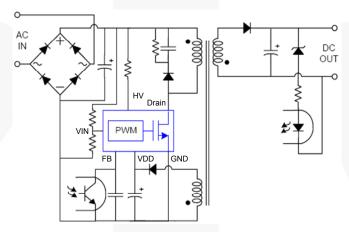


Figure 1. Typical Flyback Application

Output Power Table(1)

Product	230 V _{AC} ±		230 V _{AC} ± 15% ⁽²⁾		85-26	85-265 V _{AC}		
Product	Adapter ⁽³⁾	Open Frame ⁽⁴⁾	Adapter ⁽³⁾	Open Frame ⁽⁴⁾				
FSBH0F70A_F116	7 W	10 W	6 W	8 W				
FSBH0170_F116	10 W	15 W	9 W	13 W				
FSBH0270_F116	14 W	20 W	11 W	16 W				
FSBH0370_F116	17.5 W	25 W	13 W	19 W				

Notes

- 1. The maximum output power can be limited by junction temperature.
- 2. 230 V_{AC} or 100/115 V_{AC} with doublers.
- 3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50°C ambient.
- Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink at 50°C ambient.

Block Diagram

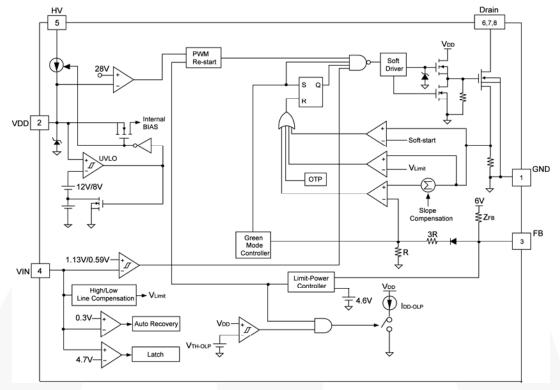


Figure 2. FSBH0170 / 0270 / 0370_F116 Internal Block Diagram

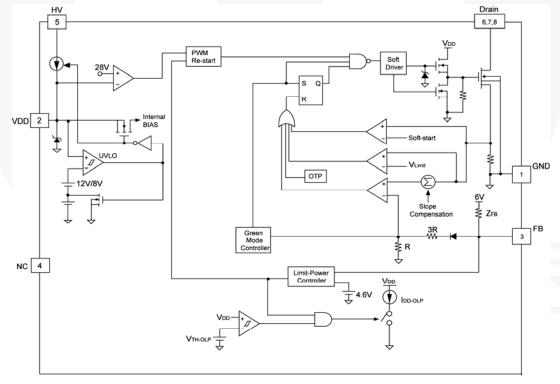
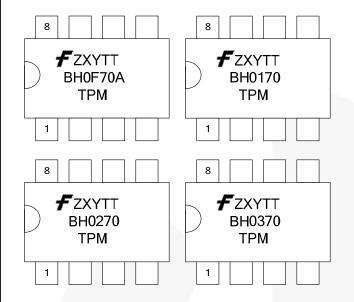


Figure 3. FSBH0F70A_F116 Internal Block Diagram

Pin Configuration



- F Fairchild Logo
- Z Plant Code
- X 1-Digit Year Code
- Y 1-Digit Week Code
- TT 2-Digit Die-Run Code
- T Package Type (N:DIP)
- P Y: Green Package
- M Manufacture Flow Code

Figure 4. Pin Configuration and Top Mark Information

Pin Definitions

Pin#	Name	Description					
1	GND	Ground. SenseFET source terminal on primary side and internal controller ground.					
2	VDD	Power Supply . The internal protection circuit disables PWM output as long as V_{DD} exceeds the OVP trigger point.					
3	FB	Feedback . The signal from the external compensation circuit is fed into this pin. The PWM duty cycle is determined in response to the signal on this pin and the internal current-sense signal.					
4	VIN	Line-Voltage Detection . The line-voltage detection is used for brownout protection with hysteresis and constant output power limit over universal AC input range. This pin has additional protections that are pull-HIGH latch and pull-LOW auto recovery, depending on the application.					
	NC	Connection. FSBH0F70A_F116					
5	HV	Startup. For startup, this pin is pulled HIGH to the line input or bulk capacitor via resistors.					
6	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.					
7	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.					
8	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.					

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit	
V _{DRAIN}	Drain Pin Voltage ^(5,6)	FSBH0x70/A_F116		700	V
		FSBH0F70A_F116		1.5	
	Drain Current Pulsed ⁽⁷⁾	FSBH0170_F116		4.0	^
I _{DM}	Diam Current Fulseu	FSBH0270_F116		8.0	Α
		FSBH0370_F116		12.0	
		FSBH0F70A_F116		10	
E _{AS}	Single Pulsed Avalanche Energy ⁽⁸⁾	FSBH0170_F116		50	mJ
LAS	olligic Fulsed Avaianone Energy	FSBH0270_F116		140	1110
		FSBH0370_F116		230	
V_{DD}	DC Supply Voltage			30	V
V_{FB}	FB Pin Input Voltage		-0.3	7.0	V
V _{IN}	VIN Pin Input Voltage		-0.3	7.0	V
V_{HV}	HV Pin Input Voltage			700	V
P_D	Power Dissipation (T _A < 50°C)			1.5	W
Θ_{JA}	Junction-to-Air Thermal Resistance			80	°C/W
Ψлт	Junction-to-Top Thermal Resistance ⁽⁹⁾			20	°C/W
TJ	Operating Junction Temperature		Internally	limited ⁽¹⁰⁾	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T∟	Lead Temperature (Wave Soldering or IR, 10 Se	econds)		+260	°C
		FSBH0F70A_F116	5.0		
	Human Body Model	FSBH0170_F116	5.0		
	(All Pins Except HV pin): JESD22-A114	FSBH0270_F116	5.0		
ESD		FSBH0370_F116	5.0		kV
LSD		FSBH0F70A_F116	2.0		KV
	Charged Device Model	FSBH0170_F116	2.0		
	(All Pins Except HV pin): JESD22-C101	FSBH0270_F116	2.0	7	
		FSBH0370_F116	1.5		

Notes:

- 5. All voltage values, except differential voltages, are given with respect to the network ground terminal.
- 6. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
- 7. Non-repetitive rating: pulse width is limited by maximum junction temperature.
- 8. L = 51mH, starting $T_J = 25$ °C.
- 9. Measured on the package top surface.
- 10. Internally Limited of T_J refers to T_{OTP}

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Ī	Symbol	Parameter	Min.	Max.	Unit
	T_A	Operating Ambient Temperature		+105	°C

Electrical Characteristics

 $V_{\text{DD}}\text{=}15~V$ and $T_{\text{A}}\text{=}25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition		Min.	Тур.	Max.	Unit
SenseFET	Section				•		
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250 μA, V _{GS} =0 V		700			V
	Zero-Gate-Voltage	V _{DS} =700 V, V _{GS} =0 V				50	
I _{DSS}	Drain Current	V _{DS} =560 V, V _{GS} =0 V, T	_C =125°C			200	μA
			FSBH0F70A_F116		14.00	19.00	
Б	Drain-Source On-	\/ -40\/ L -0.5 A	FSBH0170_F116		8.80	11.00	
$R_{DS(ON)}$	State Resistance ⁽¹²⁾	V _{GS} =10 V, I _D =0.5 A	FSBH0270_F116		6.00	7.20	Ω
			FSBH0370_F116		4.00	4.75	
			FSBH0F70A_F116		162	211	
0	Innut Consoitance	V _{GS} =0 V, V _{DS} =25 V,	FSBH0170_F116		250	325	
C _{ISS}	Input Capacitance	f=1 MHz	FSBH0270_F116		550	715	pF
			FSBH0370_F116		315	410	
/	Coss Output Capacitance		FSBH0F70A_F116		18	24	
		V _{GS} =0 V, V _{DS} =25 V,	FSBH0170_F116		25	33	
Coss		Output Capacitance f=1 MHz		FSBH0270_F116		38	50
			FSBH0370_F116		47	61	1
		FSBH0F70A_F116		3.8	5.7		
0	Reverse Transfer		FSBH0170_F116		10.0	15.0	pF
C_{RSS}	Capacitance		FSBH0270_F116		17.0	26.0	
			FSBH0370_F116		9.0	24.0	
			FSBH0F70A_F116		9.5	29.0	
	T O. D. I.	V 050 V 1 4 0 A	FSBH0170_F116		12.0	34.0	
$t_{D(ON)}$	Turn-On Delay	V _{DS} =350 V, I _D =1.0 A	FSBH0270_F116		20.0	50.0	ns
			FSBH0370_F116		11.2	33.0	
			FSBH0F70A_F116	/	19	48	
	Diag Time	V -250 V I -4.0 A	FSBH0170_F116		4	18	
t _R	Rise Time	V _{DS} =350 V, I _D =1.0 A	FSBH0270_F116		15	40	ns
			FSBH0370_F116		34	78	
			FSBH0F70A_F116		33.0	76.0	
		V 250 V I 40 A	FSBH0170_F116		30.0	70.0	
t _{D(OFF)} Turn-Off Delay	V _{DS} =350 V, I _D =1.0 A	FSBH0270_F116		55.0	120.0	ns	
		FSBH0370_F116		28.2	67.0		
			FSBH0F70A_F116		42	94	
4.	Fall Time	\/=250\/_L=4.0.4	FSBH0170_F116		10	30	no
t⊧	Fall Time	V _{DS} =350 V, I _D =1.0 A	FSBH0270_F116		25	60	ns
			FSBH0370_F116		32	74	

Continued on the following page...

Electrical Characteristics (Continued)

 V_{DD} =15 V and T_A =25°C unless otherwise specified.

Symbol	Pa	rameter	Condition	Min.	Тур.	Max.	Unit
Control Sec	tion	tion				•	·
V _{DD} Section							
$V_{\text{DD-ON}}$	Start Threshold Voltage				12	13	V
$V_{DD\text{-}OFF}$	Minimum Operation	ng Voltage		7	8	9	V
		FSBH0170_F116	6				
	l Otantun Ourmant	FSBH0270_F116	V _{DD-ON} – 0.16 V			30	
I _{DD-ST} S	Startup Current	FSBH0370_F116					μA
		FSBH0F70A_F116	V _{DD-ON} – 0.16 V	240	320	400	
I _{DD-OP}	Operating Supply	Current	V _{DD} =15 V, V _{FB} =3 V	3.0	3.5	4.0	mA
I _{DD-ZDC}	Operating Curren	t for V _{FB} <v<sub>FB-ZDC</v<sub>	V _{DD} =12 V, V _{FB} =1.6 V	1.5	2.5	3.5	mA
I _{DD-OLP}	Internal Sink Curr	ent	V _{TH-OLP} +0.1 V	30	70	90	μA
V _{TH-OLP}	I _{DD-OLP} Off Voltage			5	6	7	V
$V_{DD\text{-}OVP}$	V _{DD} Over-Voltage	Protection		27	28	29	V
t _{D-VDD-OVP}	V _{DD} Over-Voltage	Protection Debounce	Time	75	130	200	μs
HV Section						•	
I _{HV}	Maximum Curren	t Drawn from HV Pin	HV 120 V _{DC} , V _{DD} =0 V with 10 μF	1.5	3.5	5.0	mA
I _{HV-LC}	Leakage Current after Startup		HV=700 V, V _{DD} =V _{DD-OFF} +1 V		1	20	μΑ
Oscillator S	ection			•		•	
fosc	Frequency in Non	ninal Mode	Center Frequency	94	100	106	kHz
f _{OSC-G}	Green-Mode Fred	luency		14	18	22	kHz
D _{MAX}	Maximum Duty C	ycle			85		%
f_{DV}	Frequency Variati	on vs. V _{DD} Deviation	V _{DD} =11 V to 22 V			5	%
f _{DT}	Frequency Variation Deviation (11)	on vs. Temperature	T _A =-25 to 85°C			5	%
V _{IN} Section			-		•		
V _{IN-ON}	PWM Turn-On Th	reshold Voltage		1.08	1.13	1.18	V
V _{IN-OFF}	PWM Turn-Off Th	reshold Voltage		0.50	0.55	0.60	V
t _{IN-OFF}	PWM Turn-Off Debounce Time				500		ms
V _{IN-H}	Pull-HIGH Latch Trigger Level				4.7	5.0	V
t _{IN-H}	Pull-HIGH Latch Debounce Time				100		μs
V _{IN-L}	Pull-LOW Auto-Recovery Trigger Level				0.3	0.4	V
	put Section						
A _V	FB Voltage to Cur	rent-Sense Attenuation	1	1/4.5	1/4.0	1/3.5	V/V
Z _{FB}	Input Impedance			4		7	kΩ
V _{FB-OPEN}	Output High Volta	ge	FB Pin Open	5.5		İ	V

Continued on the following page...

Electrical Characteristics (Continued)

V_{DD}=15 V and T_A=25°C unless otherwise specified.

Par	rameter	Condition	Min.	Тур.	Max.	Unit
Green-Mode Entry	Green-Mode Entry FB Voltage			2.5	2.7	V
Green-Mode Endi	ng FB Voltage		1.9	2.0	2.1	V
Zero Duty Cycle F	B Voltage			1.6		V
FB Open-Loop	FSBH0F70A_F116		5.2	5.4	5.6	V
V _{FB-OLP} Trigger Level	FSBH0x70_F116		4.4	4.6	4.8	\ \ \
FB Open-Loop Pro	otection Delay		50	56	59	ms
se Section ⁽¹⁵⁾						
	FSBH0F70A_F116	V _{IN} Open	0.63	0.73	0.83	Α
I _{LIM} Peak Current Limit	FSBH0170_F116	V _{IN} =1.2 V	0.70	0.80	0.90	
	FSBH0270_F116	V _{IN} =1.2 V	0.90	1.00	1.10	
	FSBH0370_F116	V _{IN} =1.2 V	1.10	1.20	1.30	
Period During Soft-Start Time ⁽¹¹⁾			4.5	5.0	5.5	ms
wer Limit (FSBH0	170, FSBH0270, FSBH	0370)				
Threshold Voltage	e 1 for Current Limit	V _{IN} =1.2 V	0.73	0.80	0.87	V
Threshold Voltage	e 2 for Current Limit	V _{IN} =3.6 V	0.56	0.63	0.70	V
wer Limit (FSBH0	F70A)		•			
Threshold Voltage	e for Current Limit		0.97	1.00	1.03	V
rature Protection	Section (OTP)		ų.			
Protection Junctio	n Temperature ^(11,13)		+135	+142	+150	°C
				T _{OTP} -25		°C
	Green-Mode Entry Green-Mode Entry Green-Mode Endi Zero Duty Cycle F FB Open-Loop Trigger Level FB Open-Loop Propose Section (15) Peak Current Limit Period During Soft Diver Limit (FSBH0) Threshold Voltage Diversity Threshold Voltage Diver	Green-Mode Ending FB Voltage Zero Duty Cycle FB Voltage FB Open-Loop Trigger Level FSBH0F70A_F116 FSBH0x70_F116 FB Open-Loop Protection Delay SE Section (15) Peak Current Limit FSBH0F70A_F116 FSBH0170_F116 FSBH0270_F116 FSBH0370_F116 Period During Soft-Start Time (11)	Green-Mode Entry FB Voltage Green-Mode Ending FB Voltage Zero Duty Cycle FB Voltage FB Open-Loop Trigger Level FSBH0F70A_F116 FSBH0x70_F116 FB Open-Loop Protection Delay se Section FSBH0F70A_F116 FSBH0F70A_F116 FSBH0F70A_F116 FSBH0170_F116 FSBH0270_F116 FSBH0370_F116 VIN=1.2 V FSBH0370_F116 VIN=1.2 V Period During Soft-Start Time Time VIN=1.2 V Threshold Voltage 1 for Current Limit Threshold Voltage 2 for Current Limit FSBH0F70A) Threshold Voltage for Current Limit Frature Protection Section (OTP) Protection Junction Temperature (11,13)	Green-Mode Entry FB Voltage 2.3 Green-Mode Ending FB Voltage 1.9 Zero Duty Cycle FB Voltage 5.2 FB Open-Loop Trigger Level FSBH0F70A_F116 4.4 FB Open-Loop Protection Delay 50 see Section(15) FSBH0F70A_F116 V _{IN} Open 0.63 FSBH0170_F116 V _{IN} =1.2 V 0.70 FSBH0270_F116 V _{IN} =1.2 V 0.90 FSBH0370_F116 V _{IN} =1.2 V 1.10 Period During Soft-Start Time(11) 4.5 Ower Limit (FSBH0170, FSBH0270, FSBH0370) Threshold Voltage 1 for Current Limit V _{IN} =1.2 V 0.73 Threshold Voltage 2 for Current Limit V _{IN} =3.6 V 0.56 Ower Limit (FSBH0F70A) Threshold Voltage for Current Limit 0.97 Protection Junction Temperature(11,13) Protection Junction Temperature(11,13)	Green-Mode Entry FB Voltage 2.3 2.5	Green-Mode Entry FB Voltage 2.3 2.5 2.7

Notes:

- 11. These parameters, although guaranteed, are not 100% tested in production.
- 12. Pulse test: pulse width $\leq 300 \,\mu\text{s}$, duty $\leq 2\%$.
- 13. When activated, the output is disabled and the latch is turned off.
- 14. The threshold temperature for enabling the output again and resetting the latch after over-temperature protection has been activated.
- 15. These parameters, although guaranteed, are tested in wafer process.

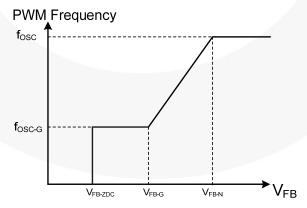


Figure 5. V_{FB} vs. PWM Frequency

Typical Characteristics

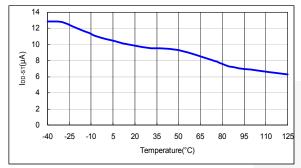


Figure 6. I_{DD-ST} vs. Temperature

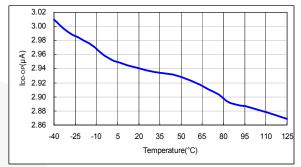


Figure 7. I_{DD-OP} vs. Temperature

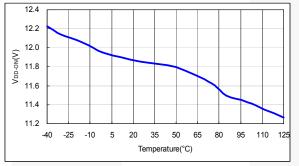


Figure 8. V_{DD-ON} vs. Temperature

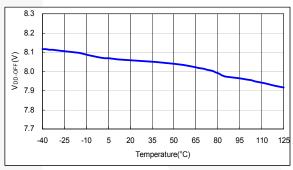


Figure 9. V_{DD-OFF} vs. Temperature

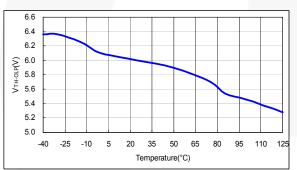


Figure 10. V_{TH-OLP} vs. Temperature

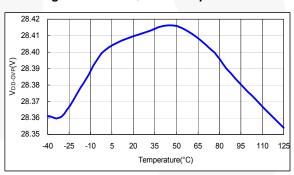


Figure 11. V_{DD-OVP} vs. Temperature

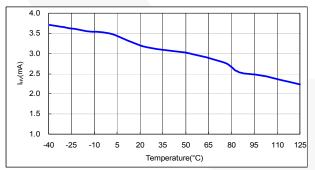


Figure 12. I_{HV} vs. Temperature

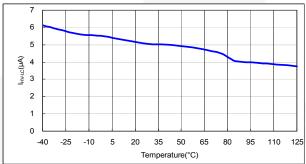


Figure 13. I_{HV-LC} vs. Temperature

Typical Characteristics

0.64

0.63

0.62

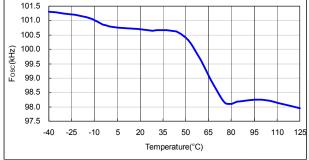
0.60

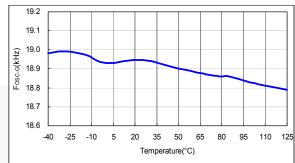
0.59

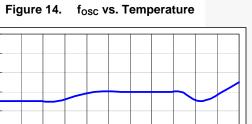
0.58

-25 -10

VIN-OFF(V) 0.61







95

Figure 15. fosc-g vs. Temperature

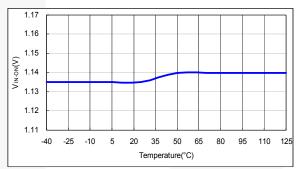


Figure 16. V_{IN-OFF} vs. Temperature

35 50 65

Temperature(°C)

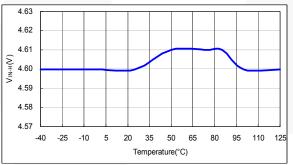


Figure 17. V_{IN-ON} vs. Temperature

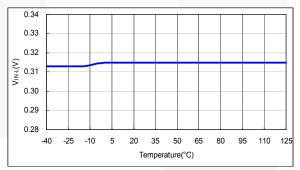
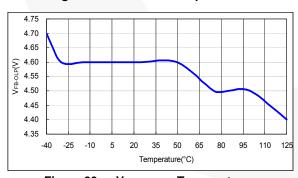


Figure 18. V_{IN-H} vs. Temperature



V_{IN-L} vs. Temperature Figure 19.

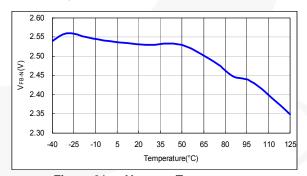


Figure 20. V_{FB-OLP} vs. Temperature

Figure 21. V_{FB-N} vs. Temperature

Typical Characteristics

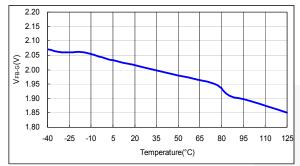


Figure 22. $V_{\text{FB-G}}$ vs. Temperature

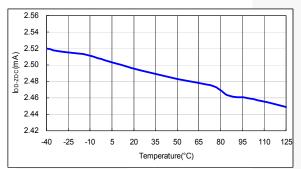


Figure 24. I_{DD-ZDC} vs. Temperature

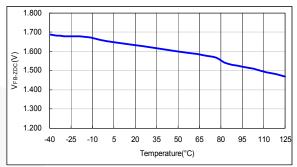


Figure 23. V_{FB-ZDC} vs. Temperature

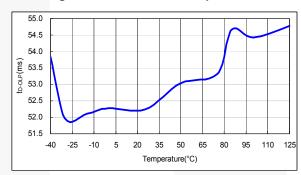


Figure 25. t_{D-OLP} vs. Temperature

Functional Description

Startup Operation

The HV pin is connected to bulk voltage through an external resistor, R_{HV} , as shown in Figure 26. When AC voltage is applied to the power system, an internal HV startup circuit provides a high current (around 3.5 mA) to charge an external V_{DD} capacitor until V_{DD} voltage exceeds the turn-on threshold voltage ($V_{DD\text{-}ON}$). For lower power consumption, the HV startup circuit shuts down during normal operation. The external V_{DD} capacitor and auxiliary winding maintain the V_{DD} voltage and provide operating current to controller.

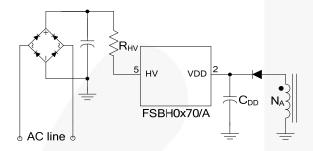


Figure 26. Startup Circuit

Slope Compensation

The FSBH-series is designed for flyback power converters. The peak-current-mode control is used to optimize system performance. Slope compensation is added to reduce current loop gain and improve power system stability. The FSBH-series has a built-in, synchronized, positive slope for each switching cycle.

Soft-Start

The FSBH-series has an internal soft-start circuit that reduces the SenseFET switching current during power system startup. The characteristic curve of soft-start time versus V_{LMT} level is shown in Figure 27. The V_{LMT} level rises in six steps. By doing so, the power system can smoothly build up the rated output voltage and effectively reduce voltage stress on the PWM switch and output diode.

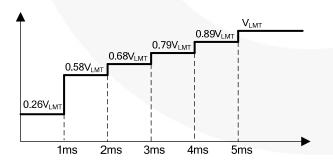


Figure 27. Soft-Start Function

Brown-In/Out Function

FSBH0x70 has a built-in internal brown-in/out protection comparator monitoring voltage of VIN pin. Figure 28 shows a resistive divider with low-pass filtering for line-voltage detection on the VIN pin.

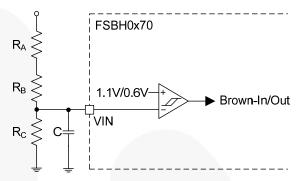


Figure 28. Brown-In/Out Function on VIN Pin

Once the VIN pin voltage is lower than 0.6 V and lasts for 500 ms, the PWM gate is disabled to protect the system from over current. FSBH0x70 starts up as V_{IN} increases above 1.1 V. Because the divider resistors of the VIN pin are connected behind the bridge, the ratio calculations for brownout in PFC and non-PFC system are different, as shown in Figure 29. The formulas are provided in the following equations:

Brownout with PFC:

$$\frac{R_C}{R_A + R_B + R_C} \cdot \sqrt{2} V_{AC_OUT} \cdot \frac{2}{\pi} = 0.6 \tag{1}$$

Brownout with non-PFC:

$$\frac{R_{\rm C}}{R_A + R_B + R_{\rm C}} \cdot \sqrt{2} V_{AC_{-}OUT} = 0.6$$
 (2)

Brown-in level is determined by:

$$V_{AC_IN} = \frac{1.1}{\sqrt{2}} \cdot \frac{R_A + R_B + R_C}{R_C}$$
 (3)

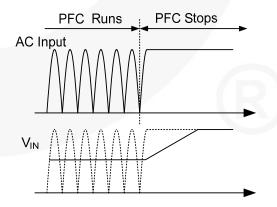


Figure 29. V_{IN} Level According to PFC Operation

Brown-In Function of FSBH0F70A

The VIN pin functions are disabled in FSBH0F70A, but FSBH0F70A has brown-in protection in the VDD pin. There is a discharge current internal from V_{DD} to ground during startup. The HV source current must be larger than $I_{\text{DD-ST}}$ to charge the capacitor of V_{DD} . Therefore, the brown-in level can be determined by R_{HV} according to the equation:

$$R_{HV} = \frac{\sqrt{2}V_{AC} - 12}{I_{DD-ST}} \tag{4}$$

Green-Mode Operation

The FSBH-series uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 30, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 100 kHz. Once V_{FB} decreases below V_{FB-N} (2.5 V), the PWM frequency starts to linearly decrease from 100 kHz to 18kHz to reduce switching losses. As V_{FB} decreases below V_{FB-G} (2.0 V), the switching frequency is fixed at 18 kHz and the FSBH-series enters "deep" green mode to reduce the standby power consumption.

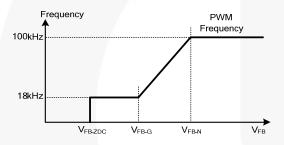


Figure 30. PWM Frequency

As V_{FB} decreases below V_{FB-ZDC} (1.6 V), the FSBH-series enters burst-mode operation. When V_{FB} drops below V_{FB-ZDC} , FSBH-series stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above V_{FB-ZDC} , switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss to improve power saving, as shown in Figure 31.

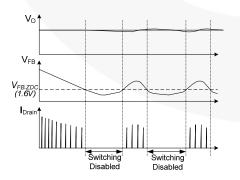


Figure 31. Burst-Mode Operation

H/L Line Over-Power Compensation

To limit the output power of the converter constantly, high/low line over-power compensation is included. Sensing the converter input voltage through the VIN pin, the high/low line compensation function generates a relative peak-current-limit threshold voltage for constant power control, as shown in Figure 32.

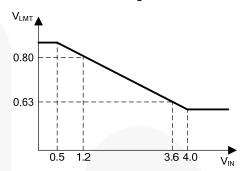


Figure 32. Constant Power Control

Protections

The FSBH-series provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

Latch/Auto-Recovery Function

Besides the brownout protection and high/low line overpower compensation, the FSBH0X70_F116 has additional protections via the VIN pin, such as pull-HIGH latch and pull-LOW auto-recovery that depends on the application. As shown in Figure 33, when V_{IN} level is higher than 4.7 V, FSBH-series is latched until the V_{DD} is discharged. FSBH-series is auto-recovery when the V_{IN} level is lower than 0.3 V.

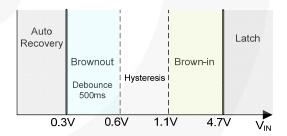
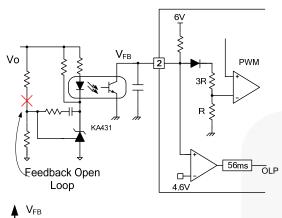


Figure 33. VIN Pin Function

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown) is broken, as shown in Figure 34, or over current or output short occurs, there is no current flowing through the opto-coupler transistor, which pulls the feedback voltage up to 6 V.

When feedback voltage is above 4.6 V for longer than 56 ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value longer than 56 ms due to the overload condition.



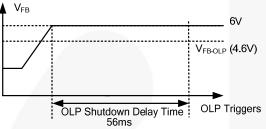


Figure 34. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

 V_{DD} over-voltage protection prevents IC damage caused by over voltage on the VDD pin. The OVP is triggered when V_{DD} voltage reaches 28 V. Debounce time (typically 130 μ s) prevents false trigger by switching noise.

Over-Temperature Protection (OTP)

The SenseFET and the control IC are integrated, making it easier to detect the temperature of the SenseFET. As the temperature exceeds approximately 142°C, thermal shutdown is activated.

Physical Dimensions 0.400 10.160 0.355 9.017 5 **PIN 1 INDICATOR** 0.280 **7**.112 6.096 0.015 [0.389] GAGE PLANE HALF LEAD 4X **FULL LEAD 4X** 0.325 **8**.263 7.628 0.005 [0.126] MIN 0.005 [0.126] MAX 0,210 [5,334] **SEATING PLANE** 0.150 **3**.811 0.115 2.922 MIN 0.015 [0.381] 0.100 [2.540] 0.300 [7.618] 0.430 [10.922] 0.022 0.562 0.014 0.358 MAX 0.070 [1.778] 0.045 [1.143] ⊕ 0.10M C NOTES: A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA B) CONTROLING DIMS ARE IN INCHES C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1982 E) DRAWING FILENAME AND REVSION: MKT-N08MREV1.

Figure 35. 8-Pin Dual In-Line Package (DIP)

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