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June 2014

# FQA70N10

## N-Channel QFET<sup>®</sup> MOSFET

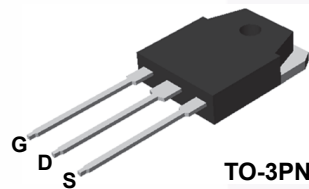
100 V, 70 A, 23 mΩ

### Description

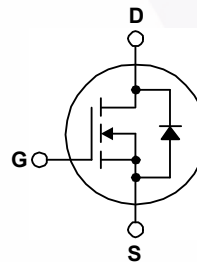
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 70 A, 100 V,  $R_{DS(on)} = 23 \text{ m}\Omega$  (Max) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 35 \text{ A}$
- Low Gate Charge (Typ. 85 nC)
- Low Crss (Typ. 150 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



TO-3PN



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQA70N10	Unit
$V_{DSS}$	Drain-Source Voltage	100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	70	A
		49.5	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	280	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1300	mJ
$I_{AR}$	Avalanche Current (Note 1)	70	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	21.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	214	W
		1.43	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQA70N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

FQA70N10 — N-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQA70N10	FQA70N10	TO-3PN	-	-	30

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.1	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	--	0.019	0.023	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 35\text{ A}$	--	48	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2500	3300	pF
$C_{oss}$	Output Capacitance		--	720	940	pF
$C_{rss}$	Reverse Transfer Capacitance		--	150	200	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 70\text{ A},$ $R_G = 25\ \Omega$  (Note 4)	--	30	70	ns
$t_r$	Turn-On Rise Time		--	470	950	ns
$t_{d(off)}$	Turn-Off Delay Time		--	130	270	ns
$t_f$	Turn-Off Fall Time		--	160	330	ns
$Q_g$	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 70\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4)	--	85	110	nC
$Q_{gs}$	Gate-Source Charge		--	16	--	nC
$Q_{gd}$	Gate-Drain Charge		--	42	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	70	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	280	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 70\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 70\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	110	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	430	--	nC

#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 0.4\text{ mH}, I_{AS} = 70\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 70\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

## Typical Characteristics

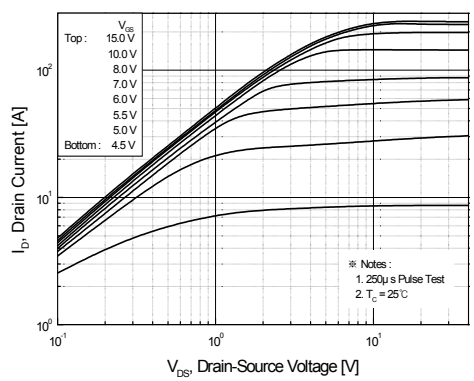


Figure 1. On-Region Characteristics

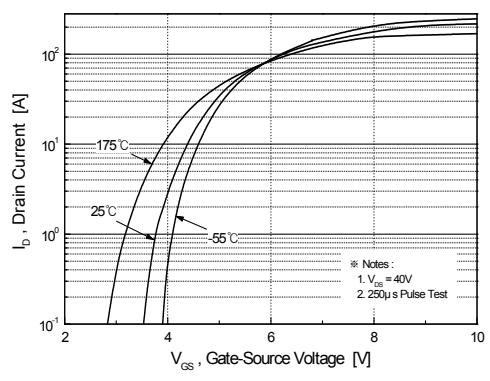


Figure 2. Transfer Characteristics

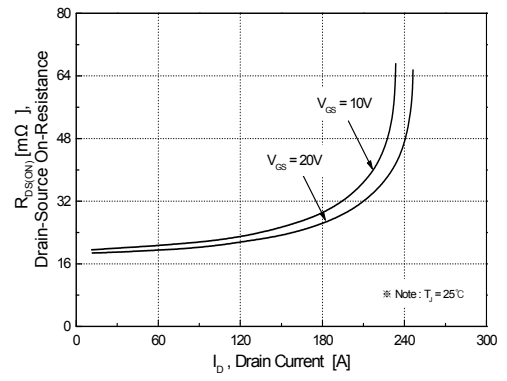


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

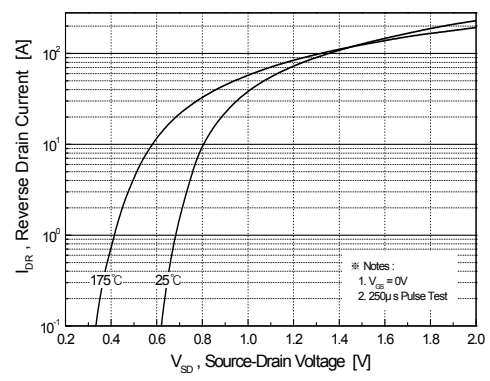


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

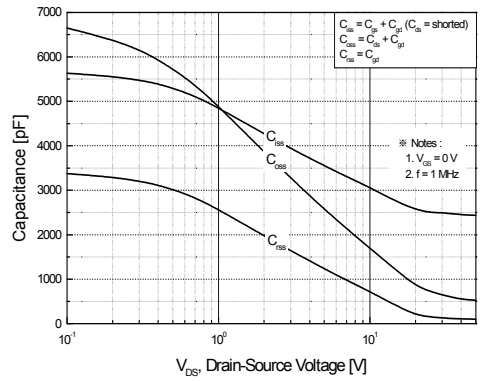


Figure 5. Capacitance Characteristics

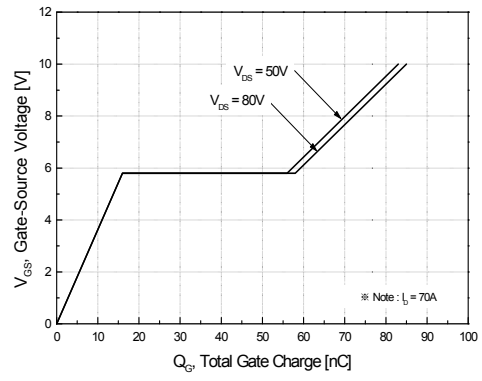
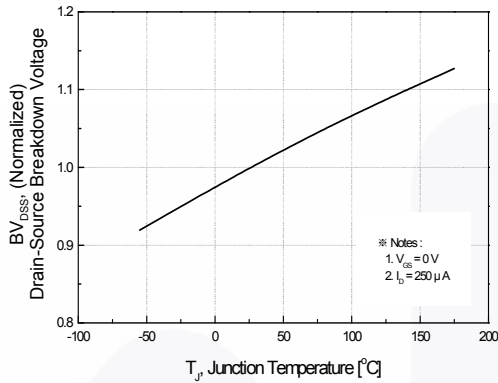
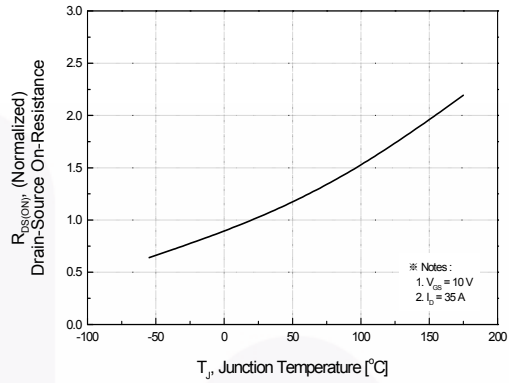


Figure 6. Gate Charge Characteristics

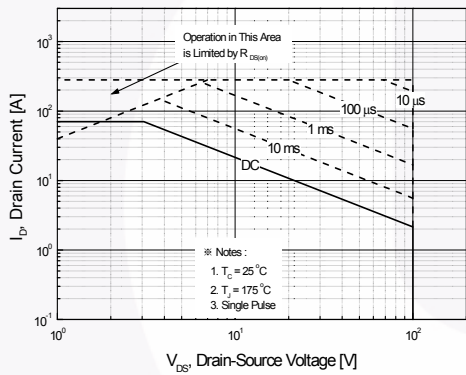
**Typical Characteristics** (Continued)



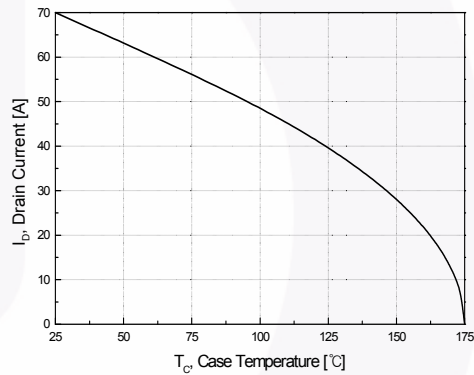
**Figure 7. Breakdown Voltage Variation vs. Temperature**



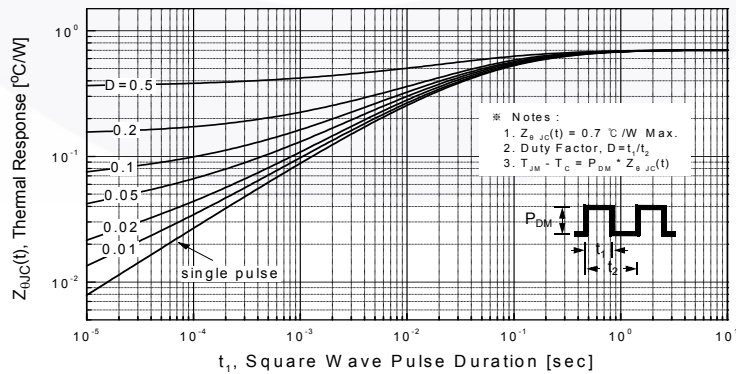
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

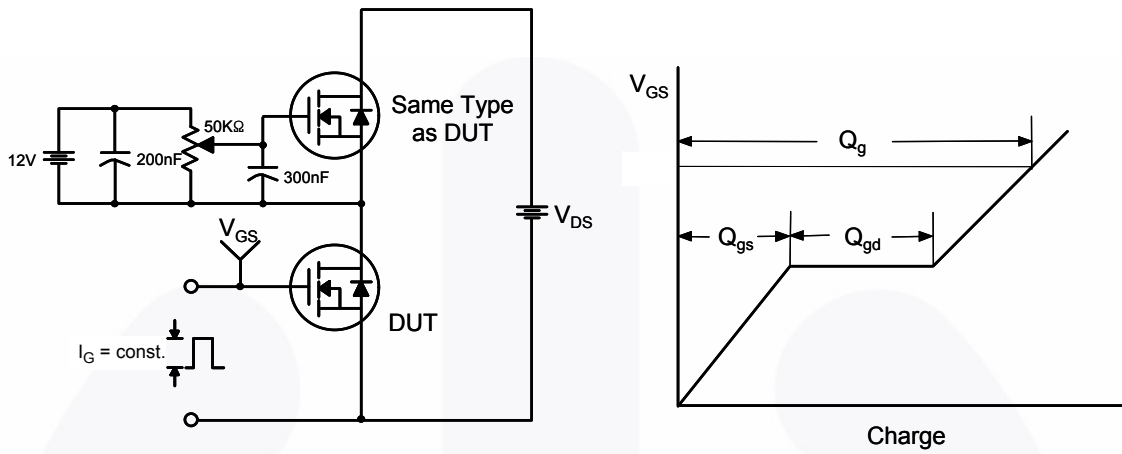


**Figure 10. Maximum Drain Current vs. Case Temperature**

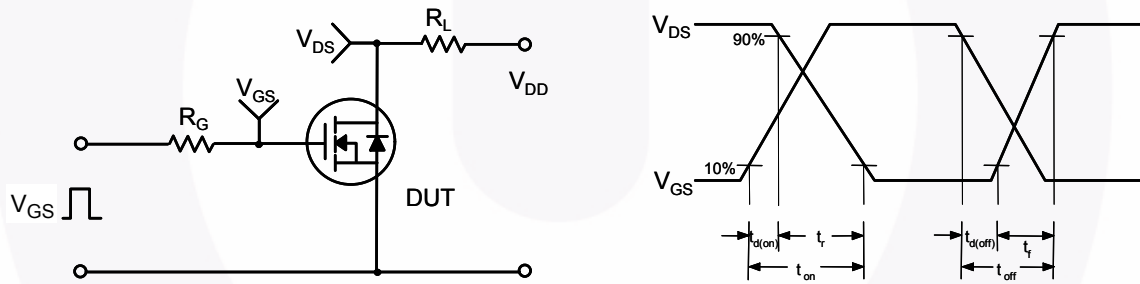


**Figure 11. Transient Thermal Response Curve**

**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

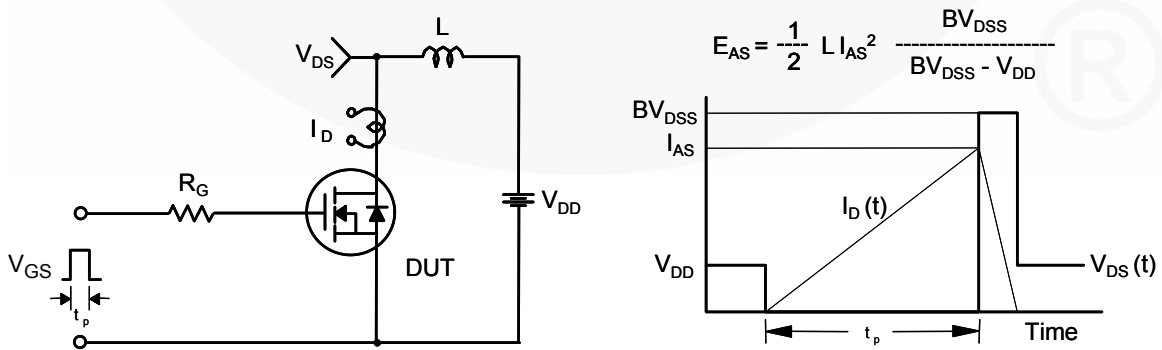
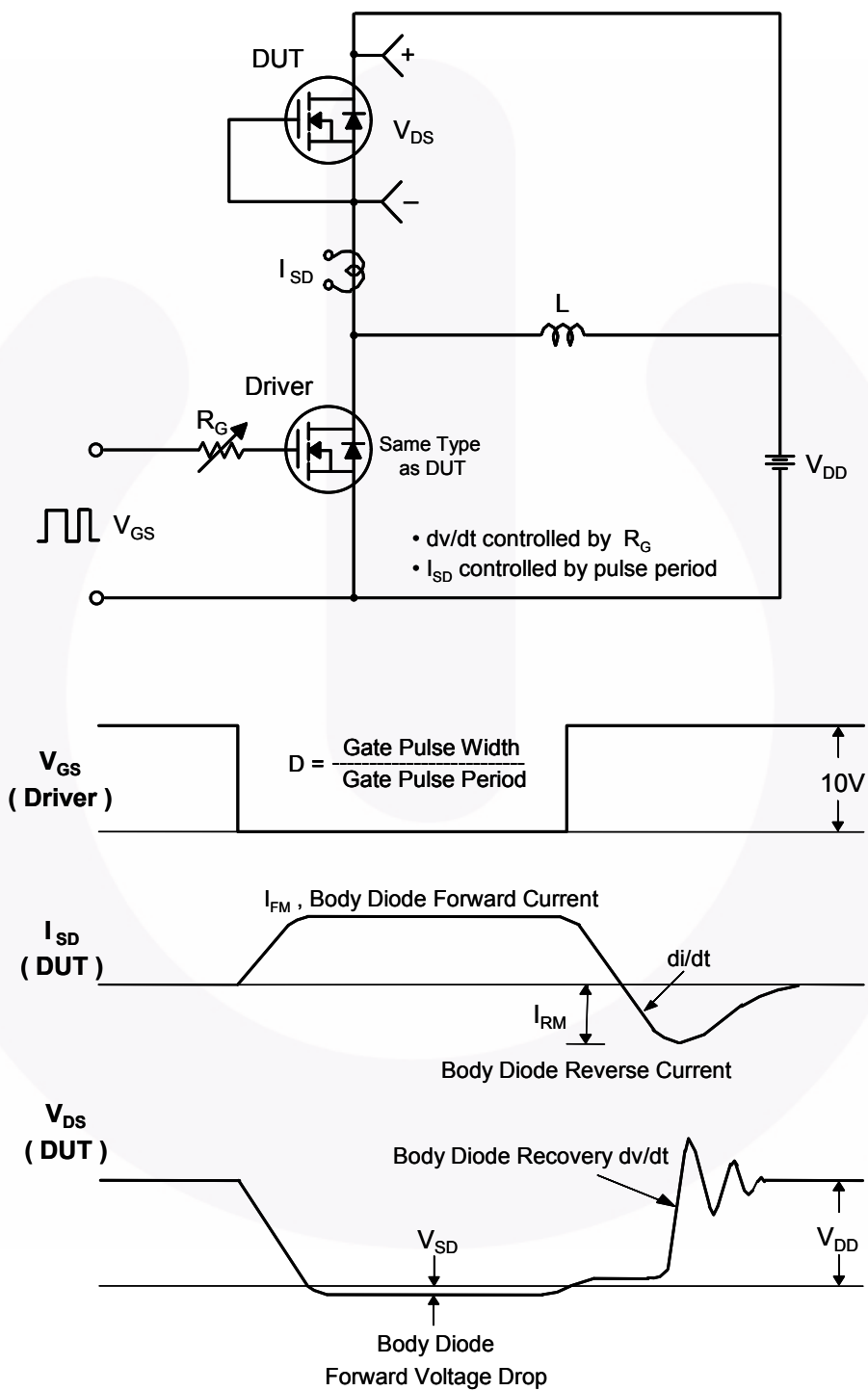
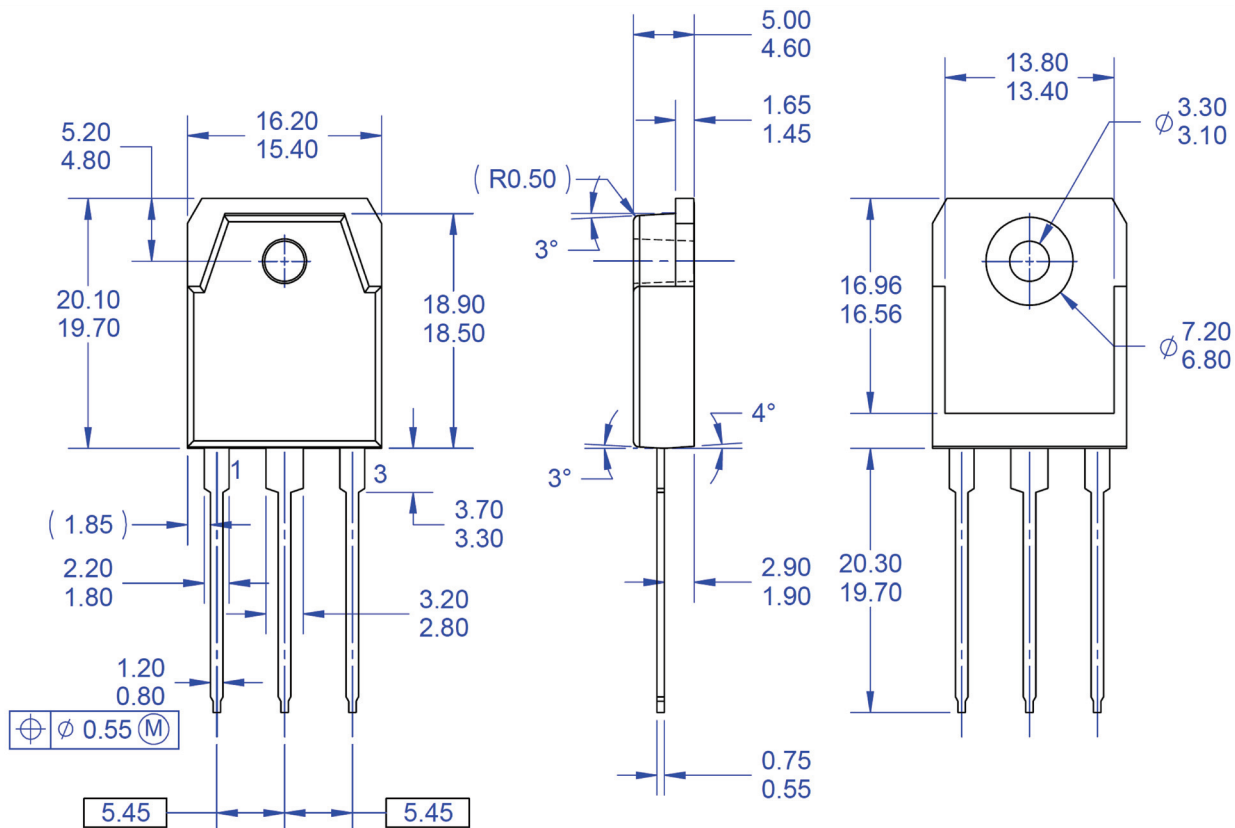


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

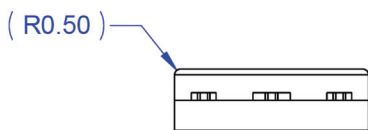


### Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.



**Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65**

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