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FQPF9N50C

N-Channel QFET® MOSFET

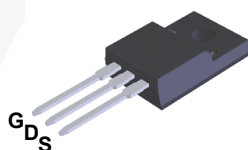
500 V, 9 A, 800 mΩ

Description

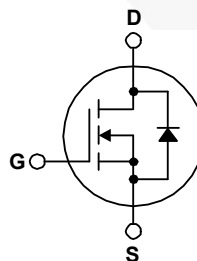
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

Features

- 9 A, 500 V, $R_{DS(on)} = 800 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 4.5 \text{ A}$
- Low Gate Charge (Typ. 28 nC)
- Low C_{rss} (Typ. 24 pF)
- 100% Avalanche Tested



TO-220F



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQPF9N50C	Units
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	9 *	A
	- Continuous ($T_C = 100^\circ\text{C}$)	5.4 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	36 *	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	360	mJ
I_{AR}	Avalanche Current (Note 1)	9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	13.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	44	W
	- Derate above 25°C	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FQPF9N50C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.86	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF9N50C	FQPF9N50C	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.57	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$	--	0.65	0.8	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 4.5\text{ A}$	--	6.5	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	790	1030	pF
C_{oss}	Output Capacitance		--	130	170	pF
C_{rss}	Reverse Transfer Capacitance		--	24	30	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 9\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	18	45	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	93	195	ns
t_f	Turn-Off Fall Time		--	64	125	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 9\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	--	28	35	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge		--	15	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 9 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 9 A,	--	335	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	2.95	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 8\text{ mH}, I_{AS} = 9\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 9\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

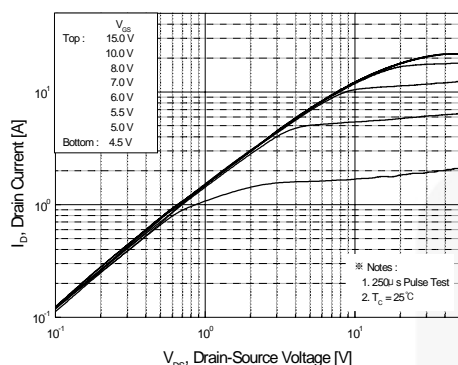


Figure 1. On-Region Characteristics

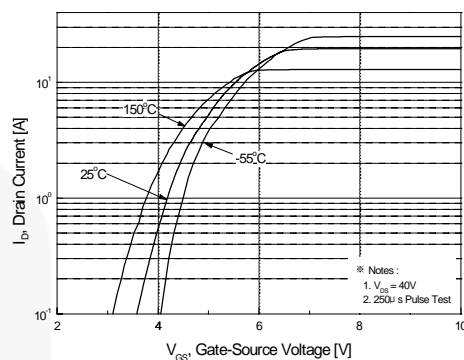


Figure 2. Transfer Characteristics

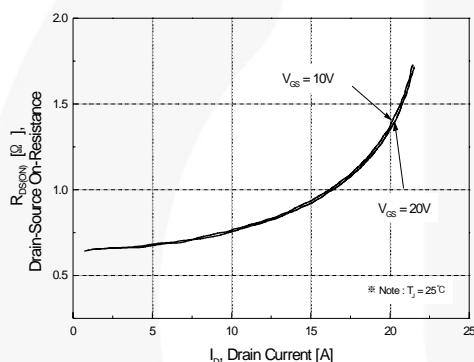


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

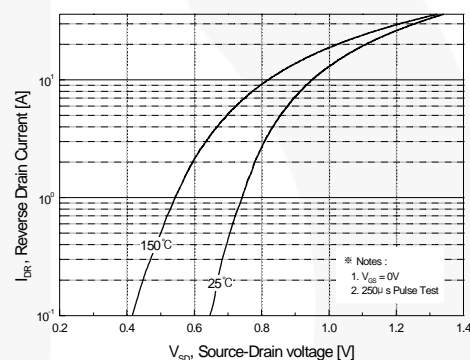


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

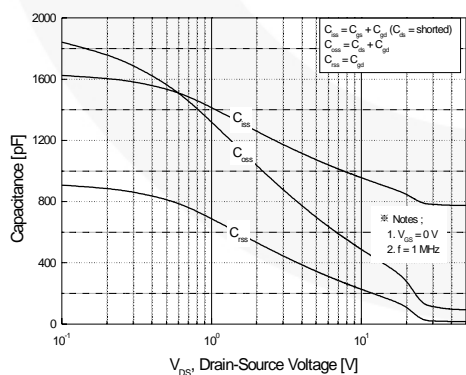


Figure 5. Capacitance Characteristics

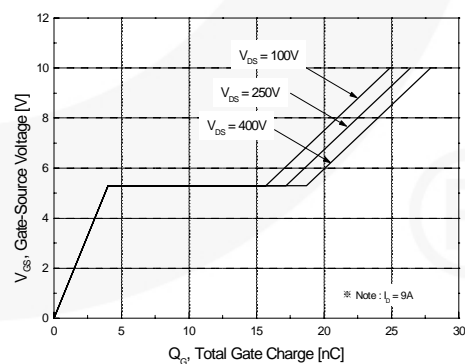


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

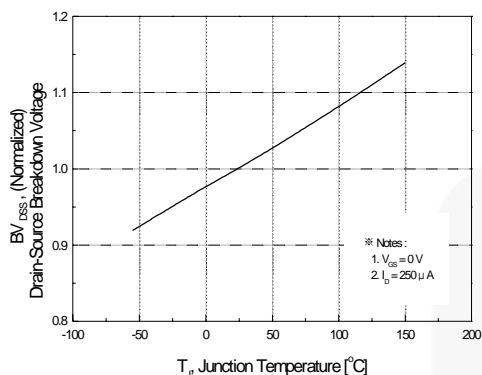


Figure 7. Breakdown Voltage Variation vs Temperature

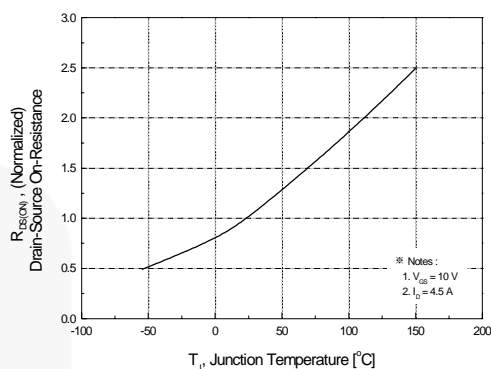


Figure 8. On-Resistance Variation vs Temperature

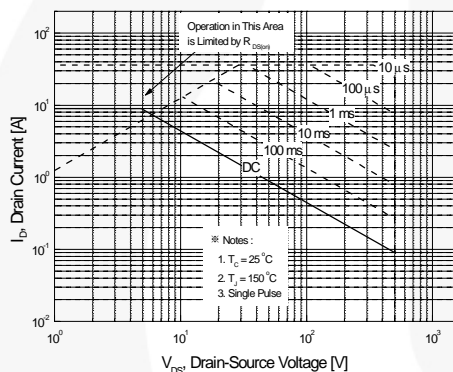


Figure 9. Maximum Safe Operating Area

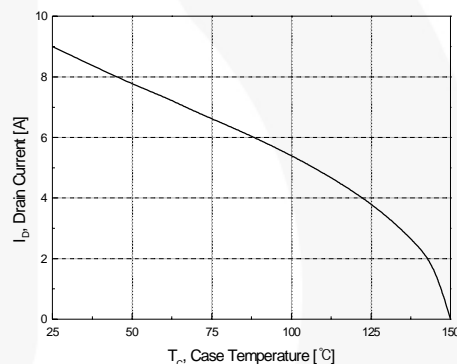


Figure 10. Maximum Drain Current vs Case Temperature

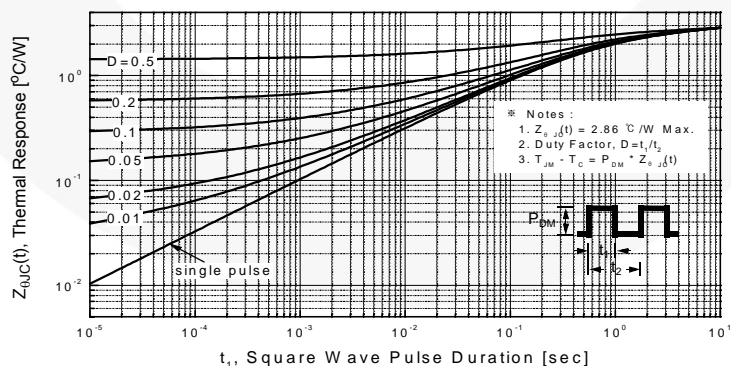


Figure 11. Transient Thermal Response Curve

The figure consists of two parts. The left part is a schematic diagram of a common-source MOSFET amplifier. A MOSFET, labeled 'DUT', has its gate connected to a pulse input V_{GS} through a resistor R_G . The drain is connected to a load resistor R_L and a supply voltage V_{DS} . The source is connected to ground. The right part is a timing diagram showing the gate voltage V_{GS} and drain voltage V_{DS} waveforms. V_{GS} is a square wave switching between 10% and 90% of its peak. V_{DS} is a trapezoidal wave. Key timing parameters are marked: $t_{d(on)}$ (delay to turn-on), t_r (rise time), t_{on} (total on-time), $t_{d(off)}$ (delay to turn-off), t_f (fall time), and t_{off} (total off-time).

Figure 1: Schematic diagram and waveforms of the test setup. The schematic shows a MOSFET switching an inductive load (L) connected to a DC source (V_{DD}). The MOSFET gate is driven by a pulse generator (V_{GS}) through a gate resistor (R_G). The drain voltage (V_{DS}) is measured across the load. The Device Under Test (DUT) is connected in parallel with the load. The waveforms show the gate voltage V_{GS} as a pulse with width t_p, the drain current I_D(t) as a trapezoidal pulse, and the drain voltage V_{DS}(t) as a voltage that ramps up during the current rise and falls during the current fall, with a peak value BV_{DSS}.

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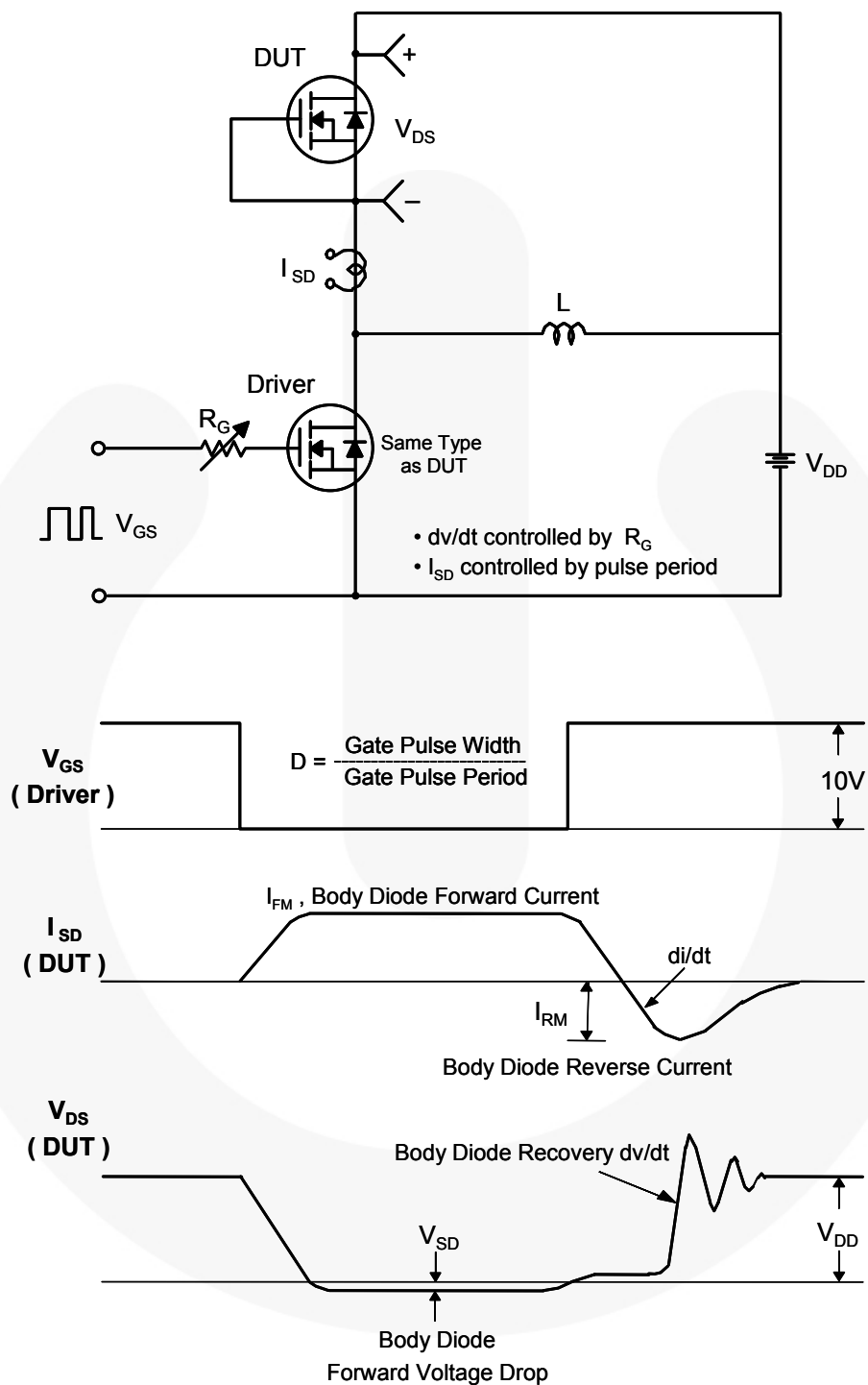


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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