

CC195**Specification**

English extract

CC195

Knock Sensor IC

Specification

Version 6.9a

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Automotive Equipment Division 8
Development of Integrated Circuits (MOS)

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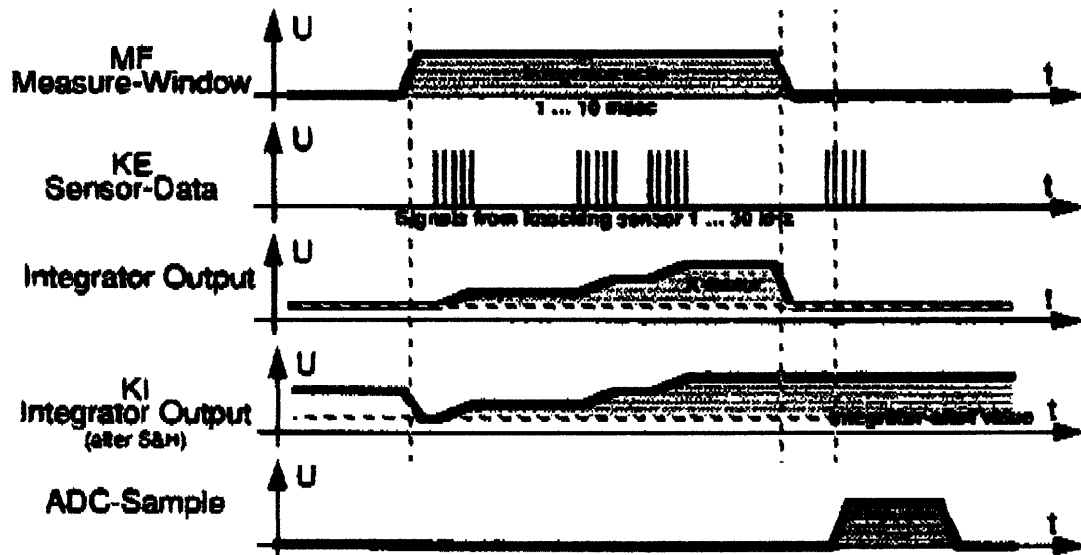
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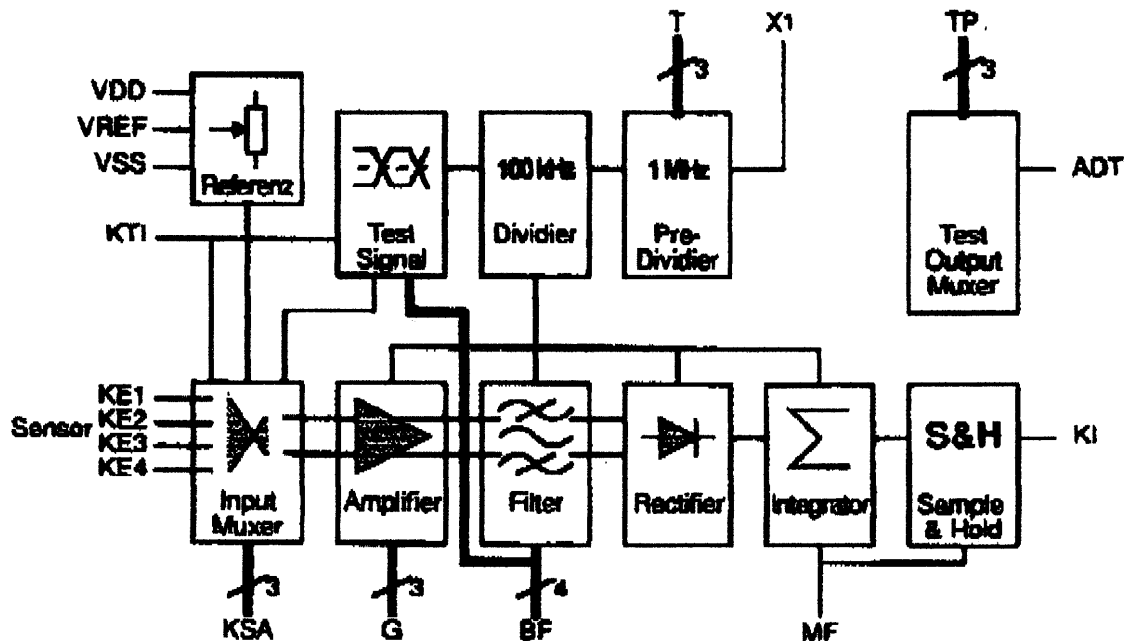
1 Introduction

1.1 Short Description of the IC

The CC195 is an application specific integrated circuit for the evaluation of analog signals from piezoelectric sound detectors (knock sensors) in gasoline engines.



It consists of a programmable amplifier, bandpass filter, rectifier, integrator and control logic.



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The CC195 was designed as a robust and trimless filter device in a switch-capacitor technology.

The circuit is fully programmable and can easily be adapted to a broad range of motor management systems and automotive engines.

- Features:**
- * 4 selectable inputs for knock sensors
 - * Alternate 2 selectable fully differential inputs for knock sensors
 - * Programmable gain (7 factors from 2 to 128)
 - * Programmable bandpass filter (9 centre frequencies from 5 to 16 kHz)
 - * No external trimming required
 - * Programmable external clock (8 steps from 1 to 18/27 MHz)
 - * Built-in facility for diagnostics
 - * Adaptable to many different microcontroller types
 - * PLCC 28 Package

The CC195 is available as packaged part and can be delivered as tested die on wafer for hybrid assembly.

1.1.1 Handling Instructions

Handle with extreme care. Pins should not be touched.

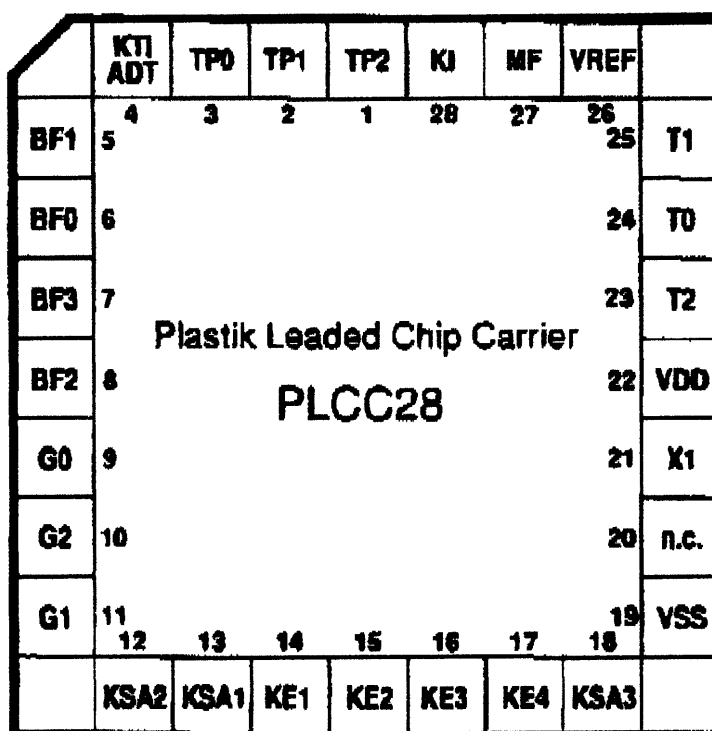
Follow ESD (Electrostatic Discharge) protection procedure.

Minimum slew - rate of Supply-Voltage: 1 V/us.

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2 Connections - Pin Configuration



VDD	Power supply 5V
VSS	Ground
VREF	VDD/2 reference voltage output
X1	External clock input X1, 1 ... 18 MHz
T0, T1, T2	Clock frequency select inputs (1 ... 18 MHz)
KE1, KE2, KE3, KE4	Knock sensor inputs 1,2,3,4
KSA1, KSA2, KSA3	Knock sensor select inputs
G0, G1, G2	Gain select inputs (2^n , $n = 1 \dots 7$)
BF0, BF1, BF2, BF3	Bandpass centre and testpulse frequency select inputs (5 ... 16 kHz)
MF	Measurement enable
KI	Knock integral output
TP0, TP1, TP2	Test mode inputs with pulldown resistors. (must be connected to VSS in normal mode) The combination TP0=TP2=VSS and TP1=VDD activates the differential input mode
KT1/ADT	Mode control input KT1 (normal mode) Test output ADT (test mode)

3 Electrical Specification

3.1 Absolute Maximum Ratings

Functional operation under any of these conditions is not implied. Operation beyond the limits in this table may impair the lifetime of the device.

Maximum rise-time of Supply-Voltage: 1 V/ μ s

Maximum Supply-Voltage: VDD-VSS: - 0.5 V ... +5.5 V

Maximum current at all inputs/outputs: +/- 25 mA

Protection of inputs/outputs against ESD: +/- 2kV
(1.5 k Ω , 100 pF)

Storage temperature: -55 ... 135° Celsius

Ambient temperature: -40 ... +125 ° Celsius

Note: For the conditions listed above the IC is protected against latch up effects.

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3.2 Characteristics

Parameter	Condition	Symbol	Min.	Max.	Unit
Supply voltage		VDD	4.75	5.25	V
Logic input level					
Low		VIL		0.8	V
High		VIH	2.0		V
External clock level					
Low		VIL1		VDD/2-1	V
High		VIH1	VDD/2+1		V
Input current LOW ②	VI = VSS.	IXL		-1	µA
X1	VDD = VDDmax	IIL	-15	-180	µA
remaining TTL inputs					
Input current HIGH ②	VI = VDDmax,	IXH		1	µA
X1	VDD = VDDmax	IHH		10	µA
remaining TTL inputs					
Voltage at the inputs TP0,1,2	VDD = VDDmax	VOBL		VSS + 0.3	V
without load ②					
Voltage at all inputs except for	VDD = VDDmax	VOBH		VDD - 0.3	V
X1, TP0,1,2, KE1,2,3,4 without					
load ②					
Supply current	VDD = VDDmax	IDD	8	30	mA
Reference voltage	IREF = ±0.5mA	VREF	VDD/2-15	VDD/2+15	V
Usable integrator shift		ΔVKI	3.5	4.7	V
Integrator offset	MF = 10msec	VKloffset			
	Temp. > 0 °C		-300	+300	mV
	Temp. < 0 °C		-400	+400	mV
Integrator output impedance		ZKI		5	kΩ
Integrator start voltage	after Reset	VKlstart	VDD/7-0.2	VDD/7+0.2	V
Integrator start voltage drift over	VDD = const.	ΔVKlstart		45	mV
temperature	(not testable)				
Input current KE1-4	VKE = 2.0 V	IKE1/2/3/4	-10	10	µA
Input voltage range KE1-4		VKE1/2/3/4	0	VDD/2±1	V

Note: All voltage values are referred to VSS.

Note ②: The TP0, TP1 und TP2 inputs have 50 kΩ nominal internal pulldown resistors.
All other logical inputs have 50 kΩ nominal internal pullup resistors.

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AC-Parameter:

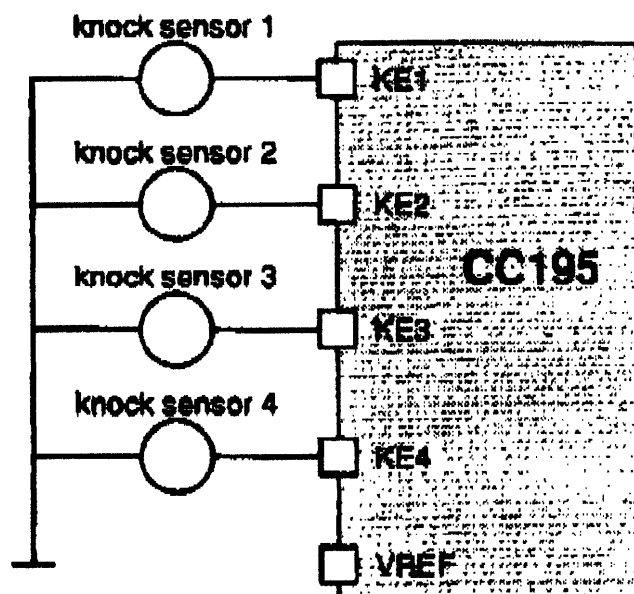
Parameter	Condition	Symbol	Min.	Max.	Unit
Input capacity at KE1-4	$f = 1\text{MHz}$, $G2 = 0$ $f = 1\text{MHz}$, $G2 = 1$	CIN	10 -10%	10 +10%	pF pF
Input frequency at KE1-4		FKE	0	30	kHz
Input clock frequency		FX1	1	18	MHz
Input capacity at X1		CXIN		5	pF
Input signal gain		V	2	128	
Gain factor tolerance		ΔV	-3	+3	%
Filter centre frequencies		FM	5	16	kHz
Filter frequency tolerance		ΔFM	-3	+3	%
Filter performance		Q	3		
Filter performance tolerance		ΔQ	-0.5	+0.3	
Integration time		T1	148	152	μs
Integrator output voltage drift during hold time	Thold = 2msec MF = 0	ΔV_{hold}		20	mV
Bandpass filter gain tolerances	FM = 5 kHz	dB5kHz	0	+0.25	dB
	FM = 6 kHz	dB6kHz	0	+0.25	dB
	FM = 7 kHz	dB7kHz	0	+0.25	dB
	FM = 8 kHz	dB8kHz	0	+0.25	dB
	FM = 9 kHz	dB9kHz	0	+0.25	dB
	FM = 10 kHz	dB10kHz	0	+0.5	dB
	FM = 12 kHz	dB12kHz	+0.25	+0.75	dB
	FM = 14 kHz	dB14kHz	+0.5	+1.0	dB
Sample & Hold gain tolerance	FM = 16 kHz	dB16kHz	+0.5	+1.0	dB
		ΔV_{SH}	-5	+5	%

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3.3 Function Tables

Asymmetric mode



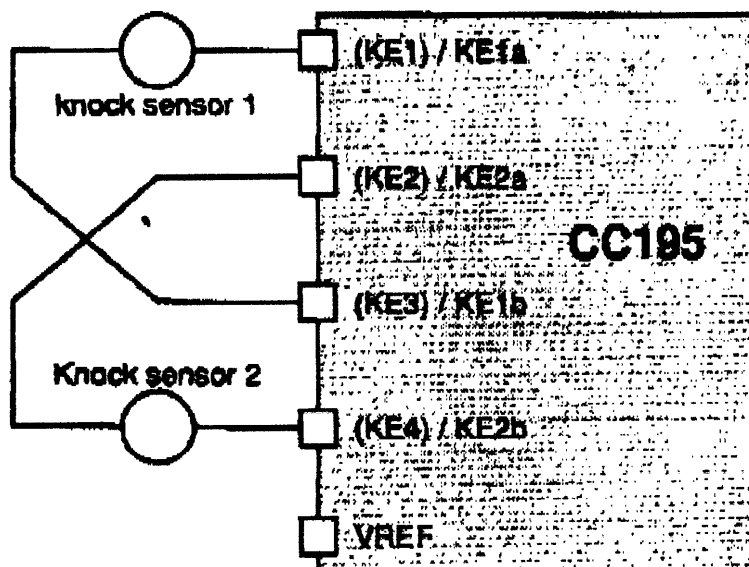
TP0 = TP1 = TP2 = low

KSA1	KSA2	KSA3	KT/VADT	Status	Testpulse
0	0	0	0	KE1 on	off
1	0	0	0	KE2 on	off
0	1	0	0	KE3 on	off
1	1	0	0	KE4 on	off
X	X	1	0	KE1/2/3/4 off	off
0	0	0	1	KE1 on	on
1	0	0	1	KE2 on	on
0	1	0	1	KE3 on	on
1	1	0	1	KE4 on	on
0	0	1	1	KE1/2/3/4 off	on
1	0	1	1	KE1/2/3/4 off	on
0	1	1	1	KE1/2/3/4 off	on
1	1	1	1	Reset	

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Differential mode



TP0 = TP2 = low und TP1 = high

KSA1	KSA2	KSA3	KT/VADT	Status	Testpulse
0	X	0	0	KE1a/b on	of
1	X	0	0	KE2a/b on	off
X	X	1	0	KE1/2 off	off
0	X	0	1	KE1a/b on	on
1	X	0	1	KE2a/b on	on
X	0	1	1	KE1/2 off	on
0	1	1	1	KE1/2 off	on
1	1	1	1	Reset	

Input gain select:

G2	G1	G0	Gain
0	0	0	2
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

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Select bandpass centre frequencies (FM) and knock testpulse frequency (FTEST):

BF3	BF2	BF1	BF0	FM	FTEST (in kHz)
0	0	0	0	10	10
0	0	0	1	(16)	---
0	0	1	0	12	12.5
0	0	1	1	14	14.29
0	1	0	0	16	16.6
0	1	0	1	(16)	---
0	1	1	0	9	9.09
0	1	1	1	(16)	---
1	0	0	0	5	5
1	0	0	1	(16)	---
1	0	1	0	6	6.25
1	0	1	1	7	7.145
1	1	0	0	8	8.3
1	1	0	1	(16)	---
1	1	1	0	(16)	---
1	1	1	1	(16)	---

Note: The bandwidth ΔF refers to the -3 dB points and is defined as:

$$\Delta F = f_{3db_{upper}} - f_{3db_{lower}}$$

The decay is -20 dB/decade at the edge of the bandpass.

The minimal attenuation above 30 kHz is 10 dB.

Extern clock frequency:

T2	T1	T0	X1 (in MHz)
0	0	0	8
0	0	1	18
0	1	0	4
0	1	1	10
1	0	0	16
1	0	1	12
1	1	0	14
1	1	1	1

MF measurement window and integration start:

MF	Measurement	Integrator (intern)	K1
0	inactive	reset	hold
1	active	active	active
	---	start	reset

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3.4 Note

All electrical parameters are referred to the internal clock frequency of 100 kHz.

With an appropriate clock frequency and the clock frequency selection (T0, T1, T2) the IC can operate at maximum 1.5 or minimum 0.5 times the 100 kHz internal frequency.

Linear changing of external clock frequency effects a linear changing of the internal clock frequency. Let F_n be the internal normal (typical) clock frequency of 100 kHz and let F be the increased/decreased internal clock frequency.

The bandpass frequencies FM can be calculated as:

$$FM_{new} = FM_{old} * (F / F_n)$$

The same equation can be applied to the test frequencies.

The increased/decreased integration time constants can be calculated as:

$$TI = 15 / F$$

(For $F = F_n$ follows $TI = 150 \mu s$)

Parameter	Condition	Symbol	Min.	Max.	Unit
Integrator offset	MF = 10msec F = 150 kHz Temp. > 0 °C	VKloffset	-600	+600	mV
	Temp. < 0 °C		-800	+800	mV
Input frequency at KE1-4	F = 50 kHz	FKE	0	15	kHz
	F = 100 kHz		0	30	kHz
	F = 150 kHz		0	45	kHz
Input clock frequency	F = 50 kHz	FX1	0.5	9	MHz
	F = 100 kHz		1	18	MHz
	F = 150 kHz		1.5	27	MHz
Filter centre frequencies	F = 50 kHz	FM	2.5	8	kHz
	F = 100 kHz		5	16	kHz
	F = 150 kHz		7.5	24	kHz
Integration time	F = 50 kHz	TI	98	102	μs
	F = 100 kHz		148	152	μs
	F = 150 kHz		198	202	μs
Bandpass filter gain tolerances	FM = 4.5 kHz	dB4.5kHz	0	+0.25	dB
	FM = 5 kHz	dB5kHz	0	+0.25	dB
	FM = 6 kHz	dB6kHz	0	+0.25	dB
	FM = 7 kHz	dB7kHz	0	+0.25	dB
	FM = 8 kHz	dB8kHz	0	+0.25	dB
	FM = 9 kHz	dB9kHz	0	+0.25	dB
	FM = 10 kHz	dB10kHz	0	+0.5	dB
	FM = 13.5 kHz	dB13.5kHz	0	+0.5	dB
	FM = 15 kHz	dB15kHz	+0.25	+0.75	dB
	FM = 12 kHz	dB12kHz	+0.25	+0.75	dB
	FM = 14 kHz	dB14kHz	+0.5	+1.0	dB
	FM = 16 kHz	dB16kHz	+0.5	+1.0	dB
	FM = 24 kHz	dB24kHz	+0.75	+1.5	dB