



Is Now Part of



ON Semiconductor®

**To learn more about ON Semiconductor, please visit our website at
www.onsemi.com**

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

MM74HCT373 • MM74HCT374

3-STATE Octal D-Type Latch •

3-STATE Octal D-Type Flip-Flop

General Description

The MM74HCT373 octal D-type latches and MM74HCT374 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The 3-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM74HCT373 LATCH ENABLE input is HIGH, the Q outputs will follow the D inputs. When the LATCH ENABLE goes LOW, data at the D inputs will be retained at the outputs until LATCH ENABLE returns HIGH again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

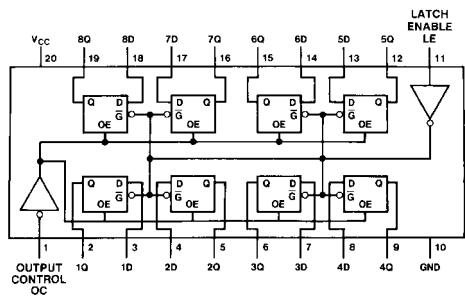
Ordering Code:

Order Number	Package Number	Package Descriptions
MM74HCT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT373N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HCT374WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT374N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

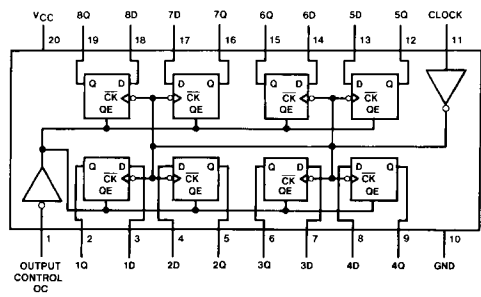
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

MM74HCT373 • MM74HCT374 3-STATE Octal D-Type Latch • 3-STATE Octal D-Type Flip-Flop

Connection Diagrams



Top View
MM74HCT373



Top View
MM74HCT374

Truth Tables

MM74HCT373

Output Control	LE	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

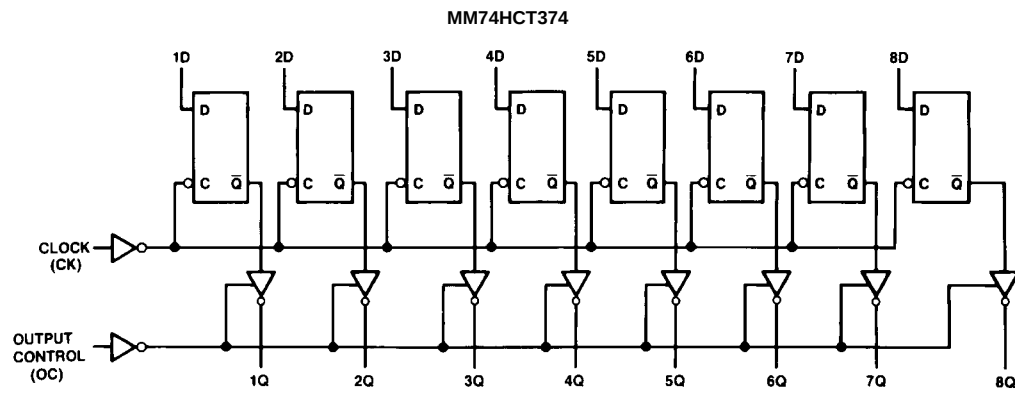
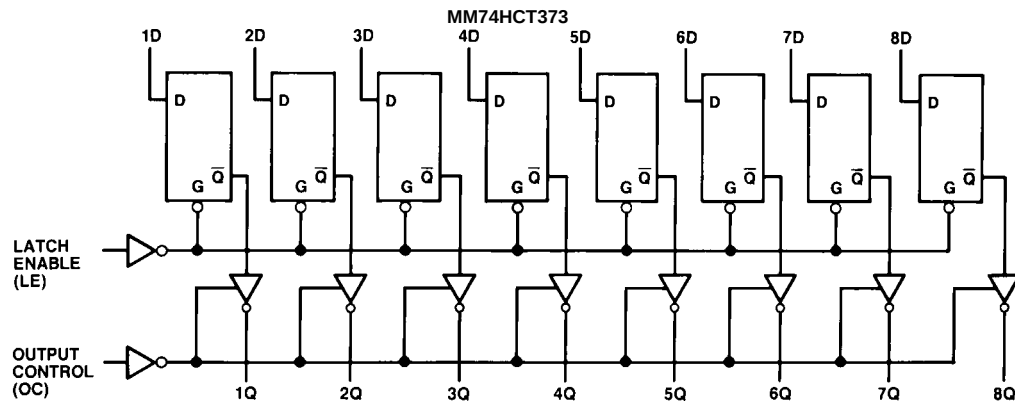
H = HIGH Level
L = LOW Level
Q₀ = Level of output before steady-state input conditions were established.
Z = High Impedance

MM74HCT374

Output Control	Clock	Data	Output (374)
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

H = HIGH Level
L = LOW Level
X = Don't Care
↑ = Transition from LOW-to-HIGH
Z = High Impedance State
Q₀ = The level of the output before steady state input conditions were established.

Logic Diagrams



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	–0.5 to +7.0V
DC Input Voltage (V_{IN})	–1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	–0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.**Note 2:** Unless otherwise specified all voltages are referenced to ground.**Note 3:** Power Dissipation temperature derating — plastic "N" package: –12 mW/°C from 65°C to 85°C.**DC Electrical Characteristics** $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
			Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V _{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL}					
		I _{OUT} = 20 μA	V _{CC}	V _{CC} - 0.1	V _{CC} - 0.1	V _{CC} - 0.1	V
		I _{OUT} = 6.0 mA, V _{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		I _{OUT} = 7.2 mA, V _{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V _{OL}	Maximum LOW Level Voltage	V _{IN} = V _{IH} or V _{IL}					
		I _{OUT} = 20 μA	0	0.1	0.1	0.1	V
		I _{OUT} = 6.0 mA, V _{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		I _{OUT} = 7.2 mA, V _{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}		±0.1	±1.0	±1.0	μA
I _{OZ}	Maximum 3-STATE Output Leakage Current	V _{OUT} = V _{CC} or GND Enable = V _{IH} or V _{IL}		±0.5	±5.0	±10	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA		8.0	80	160	μA
		V _{IN} = 2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical CharacteristicsMM74HCT373: $V_{CC} = 5.0V$, $t_r = t_f = 6 \text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay Data to Output	$C_L = 45 \text{ pF}$	18	25	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L = 45 \text{ pF}$	21	30	ns
t_{PZH} , t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L = 45 \text{ pF}$ $R_L = 1 \text{ k}\Omega$	20	28	ns
t_{PHZ} , t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L = 5 \text{ pF}$ $R_L = 1 \text{ k}\Omega$	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical CharacteristicsMM74HCT373: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A =25°C		T _A =−40 to 85°C	T _A =−55 to 125°C	Units
			Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay Data to Output	C _L = 50 pF	22	30	37	45	ns
		C _L = 150 pF	30	40	50	60	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay	C _L = 50 pF	25	35	44	53	ns
	Latch Enable to Output	C _L = 150 pF	32	45	56	68	ns
t _{PZH} , t _{PZL}	Maximum Enable Propagation Delay Control to Output	C _L = 50 pF	21	30	37	45	ns
		C _L = 150 pF R _L = 1 kΩ	30	40	50	60	ns
t _{PHZ} , t _{PLZ}	Maximum Disable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	21	30	37	45	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L = 50 pF	8	12	15	18	ns
t _W	Minimum Clock Pulse Width			16	20	24	ns
t _S	Minimum Setup Time Data to Clock			5	6	8	ns
t _H	Minimum Hold Time Clock to Data			10	13	20	ns
C _{IN}	Maximum Input Capacitance			10	10	10	pF
C _{OUT}	Maximum Output Capacitance			20	20	20	pF
C _{PD}	Power Dissipation Capacitance (Note 5)	OC = V _{CC}		5			pF
		OC = GND		52			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Electrical Characteristics

MM74HCT374: $V_{CC} = 5.0V$, $t_r = t_f = 6\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL} , t_{PLH}	Maximum Propagation Delay to Output	$C_L = 45\text{ pF}$	20	32	ns
t_{PZH} , t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L = 45\text{ pF}$ $R_L = 1\text{ k}\Omega$	19	28	ns
t_{PHZ} , t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L = 5\text{ pF}$ $R_L = 1\text{ k}\Omega$	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

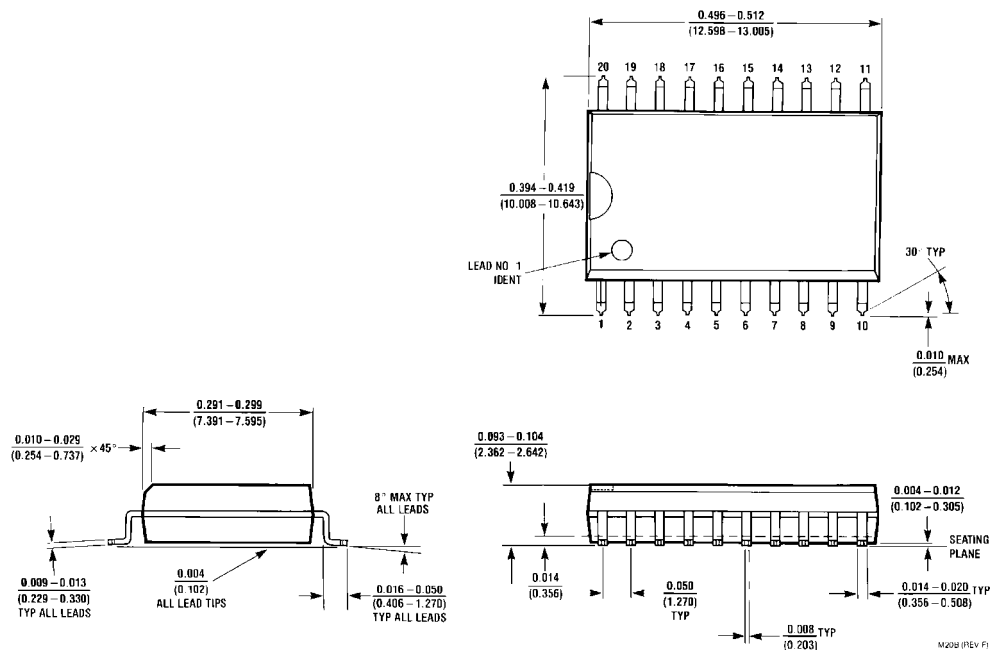
AC Electrical Characteristics

MM74HCT374: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		T _A = −40 to 85°C	T _A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
f _{MAX}	Maximum Clock Frequency			30	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay to Output	C _L = 50 pF	22	36	45	48	ns
		C _L = 150 pF	30	46	57	69	ns
t _{PZH} , t _{PZL}	Maximum Enable Propagation Delay Control to Output	C _L = 50 pF	21	30	37	45	ns
		C _L = 150 pF R _L = 1 kΩ	30	40	50	60	ns
t _{PHZ} , t _{PLZ}	Maximum Disable Propagation Delay Control to Output	C _L = 50 pF R _L = 1 kΩ	21	30	37	45	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time	C _L = 50 pF	8	12	15	18	ns
t _W	Minimum Clock Pulse Width			16	20	24	ns
t _S	Minimum Setup Time Data to Clock			20	25	30	ns
t _H	Minimum Hold Time Clock to Data			5	5	5	ns
C _{IN}	Maximum Input Capacitance			10	10	10	pF
C _{OUT}	Maximum Output Capacitance			20	20	20	pF
C _{PD}	Power Dissipation Capacitance (Note 6)	OC = V _{CC}		5			pF
		OC = GND		58			pF

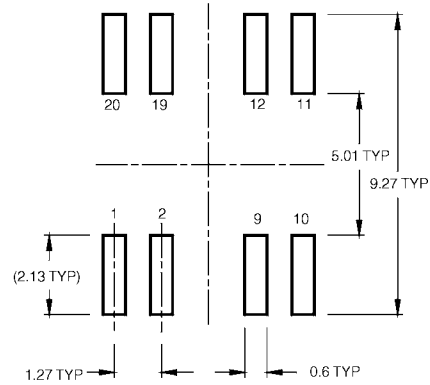
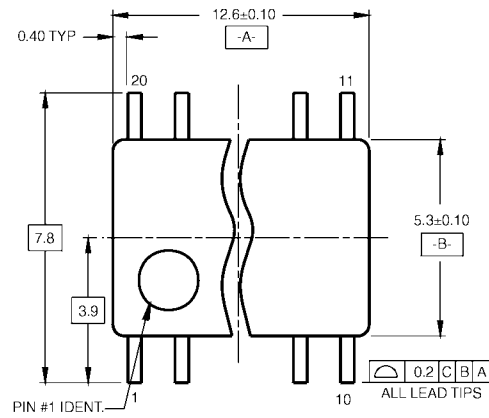
Note 6: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

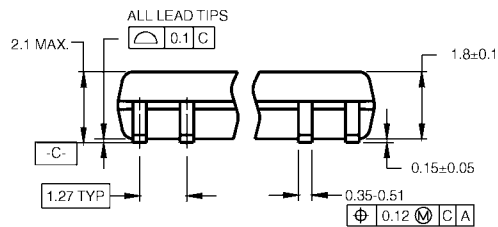


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

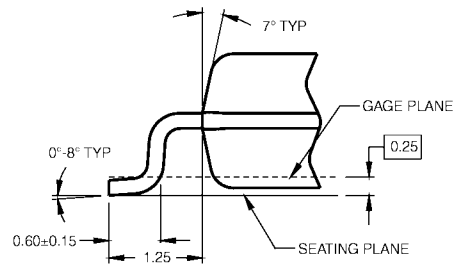
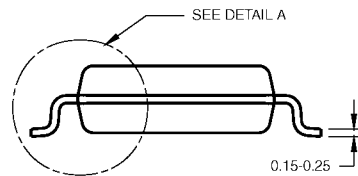
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

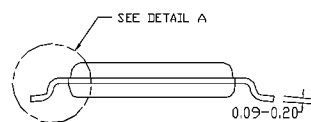
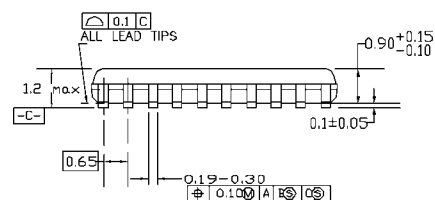
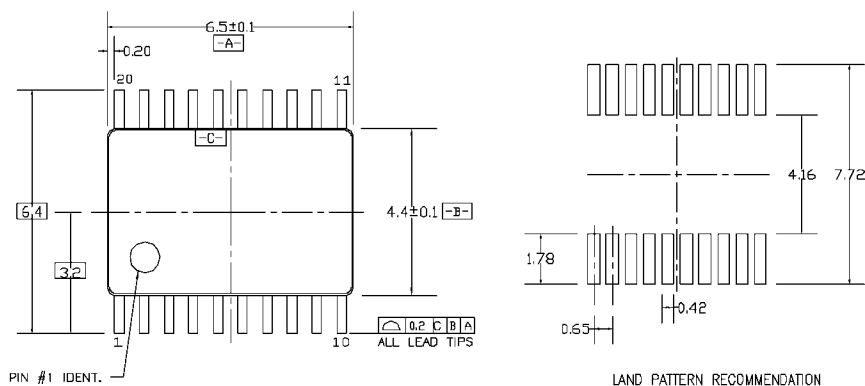
NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

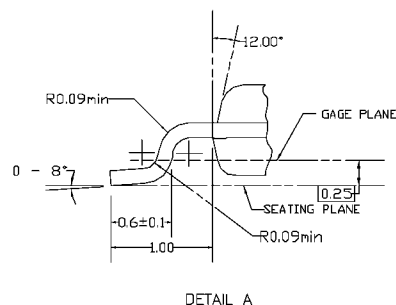
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

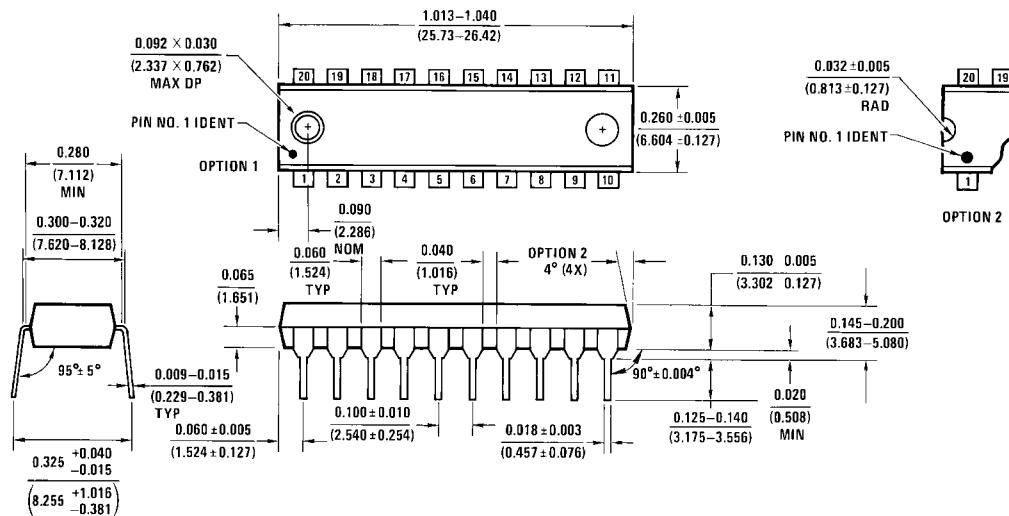
- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



DETAIL A

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative