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# FDJ1027P

## P-Channel 1.8V Specified PowerTrench® MOSFET

### Features

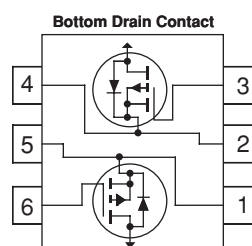
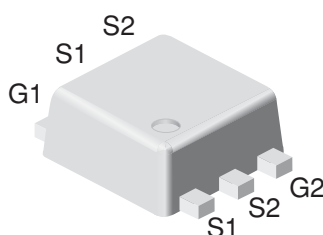
- -2.8 A, -20 V  $R_{DS(ON)} = 160 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 230 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$   
 $R_{DS(ON)} = 390 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- Low gate charge, High Power and Current handling capability
- High performance trench technology for extremely low  $R_{DS(ON)}$
- FLMP SC75 package: Enhanced thermal performance in industry-standard package size

### General Description

This dual P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. Packaged in FLMP SC75, the  $R_{DS(ON)}$  and thermal properties of the device are optimized for battery power management applications.

### Applications

- Battery management/Charger Application
- Load switch



### MOSFET Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current – Continuous (Note 1a)	-2.8	A
	– Pulsed	-12	
$P_D$	Power Dissipation for Single Operation (Note 1a)	1.5	W
	(Note 1b)	0.9	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
<b>Thermal Characteristics</b>			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	5	

### Package Marking and Ordering Information

.G	FDJ1027P	7"	8mm	3000 units
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**Electrical Characteristics**  $T_A = 25^\circ\text{C}$  unless otherwise noted

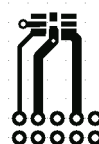
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = −250 μA	−20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = −250 μA, Referenced to 25°C		−13		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = −16 V, V <sub>GS</sub> = 0 V			−1	μA
I <sub>GSS</sub>	Gate–Body Leakage	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V			±100	nA
On Characteristics (Note 2)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = −250 μA	−0.4	−0.8	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = −250 μA, Referenced to 25°C		3		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −2.8 A V <sub>GS</sub> = −2.5 V, I <sub>D</sub> = −2.2 A V <sub>GS</sub> = −1.8 V, I <sub>D</sub> = −1.7 A V <sub>GS</sub> = −4.5 V, I <sub>D</sub> = −2.8 A, T <sub>J</sub> = 125°C		108 163 283 150	160 230 390 238	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = −5 V, I <sub>D</sub> = −2.8 A		5		S
Dynamic Characteristics						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = −10 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		290		pF
C <sub>oss</sub>	Output Capacitance			55		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			29		pF
R <sub>g</sub>	Gate Resistance	f = 1.0 MHz		13		Ω
Switching Characteristics (Note 2)						
t <sub>d(on)</sub>	Turn–On Delay Time	V <sub>DD</sub> = −10 V, I <sub>D</sub> = −1 A, V <sub>GS</sub> = −4.5 V, R <sub>GEN</sub> = 6 Ω		8	16	ns
t <sub>r</sub>	Turn–On Rise Time			13	23	ns
t <sub>d(off)</sub>	Turn–Off Delay Time			13	23	ns
t <sub>f</sub>	Turn–Off Fall Time			18	32	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = −10 V, I <sub>D</sub> = −2.8 A, V <sub>GS</sub> = −4.5 V		3	4	nC
Q <sub>gs</sub>	Gate–Source Charge			0.65		nC
Q <sub>gd</sub>	Gate–Drain Charge			0.75		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current				−1.25	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = −1.25 A (Note 2)		−0.8	−1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = −2.8 A, dI <sub>F</sub> /dI <sub>t</sub> = 100 A/μs		14		ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge			4		nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $80^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper (Single Operation).



b)  $140^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics

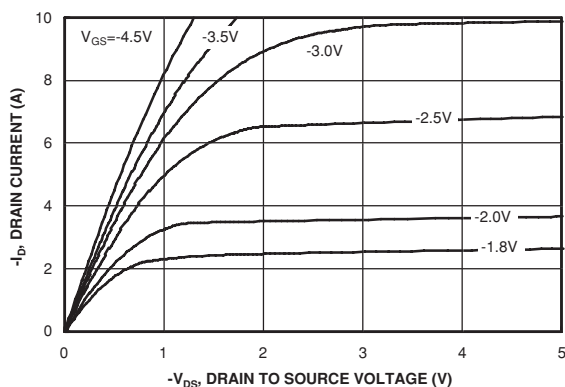


Figure 1. On-Region Characteristics.

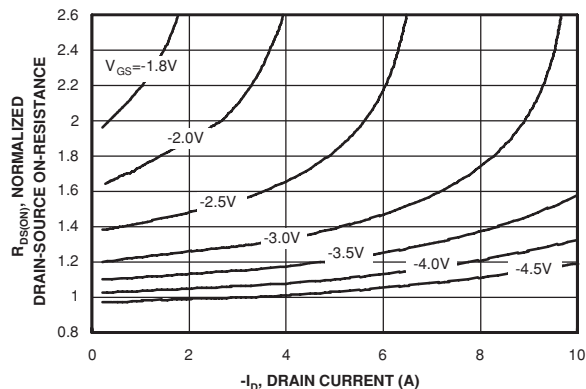


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

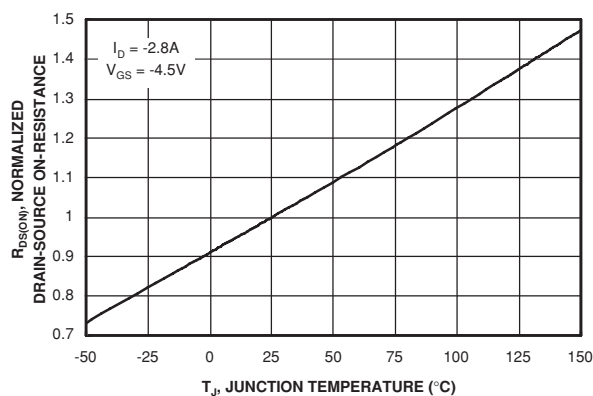


Figure 3. On-Resistance Variation with Temperature.

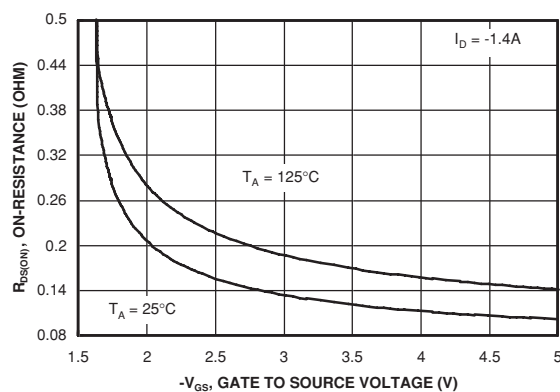


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

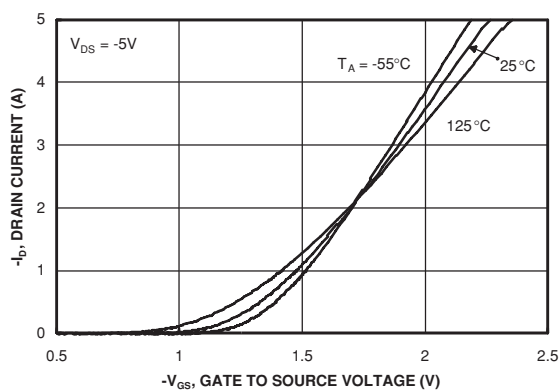


Figure 5. Transfer Characteristics.

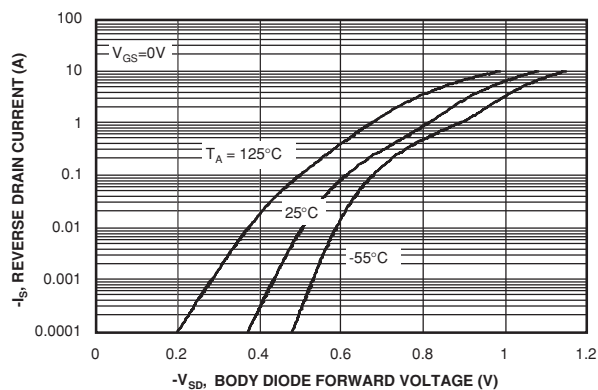


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

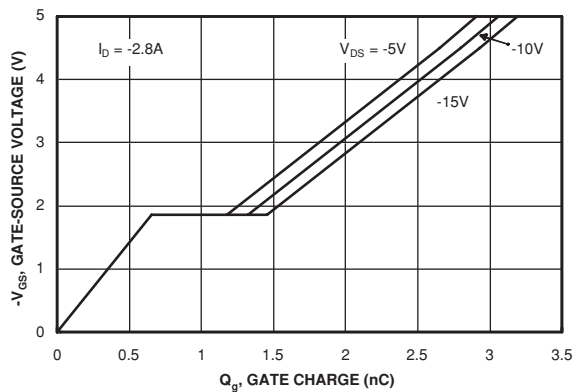


Figure 7. Gate Charge Characteristics.

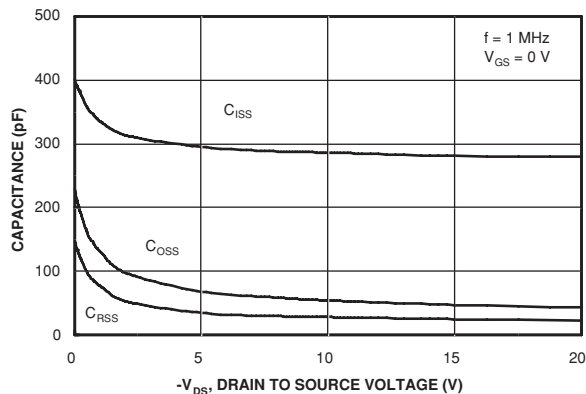


Figure 8. Capacitance Characteristics.

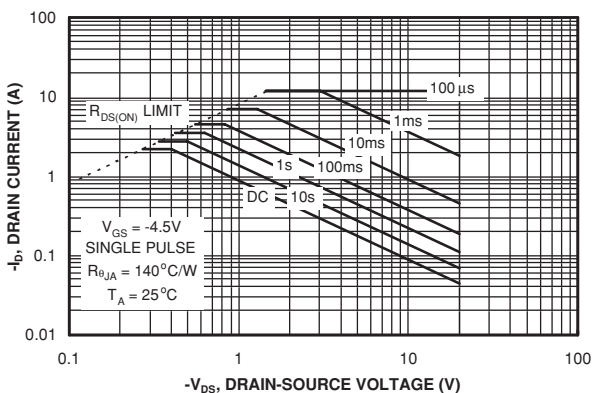


Figure 9. Maximum Safe Operating Area.

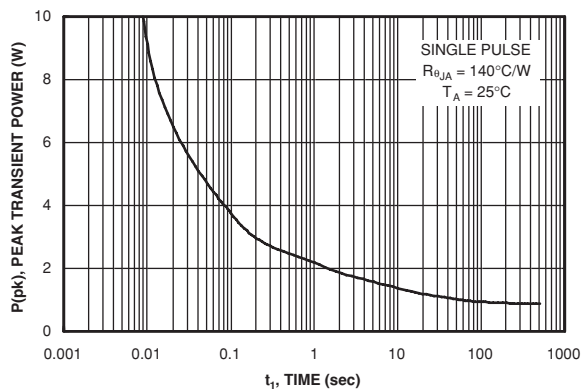


Figure 10. Single Pulse Maximum Power Dissipation.

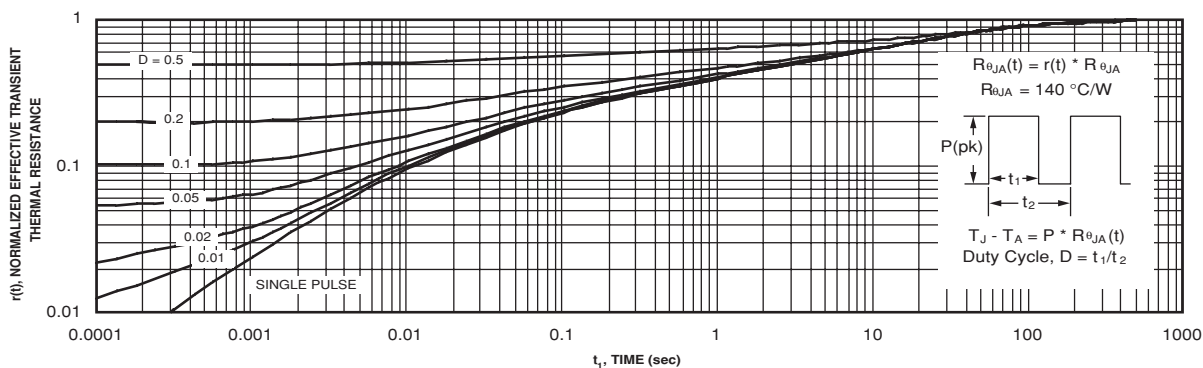
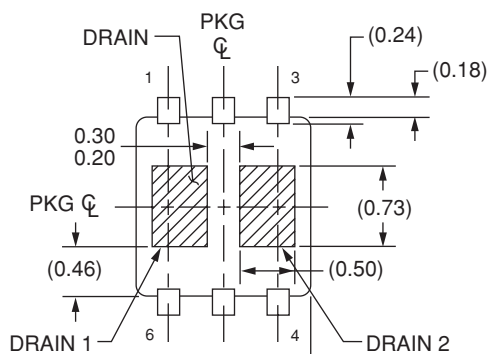


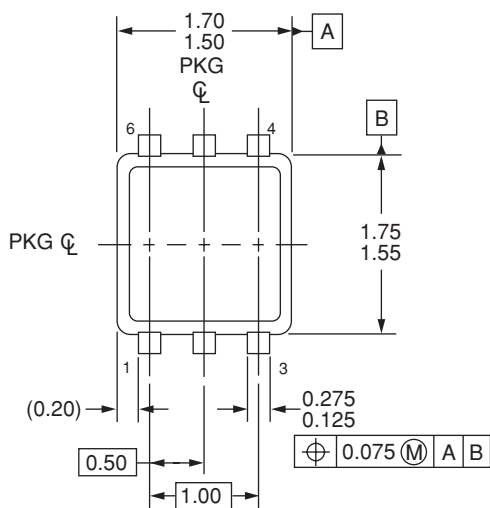
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

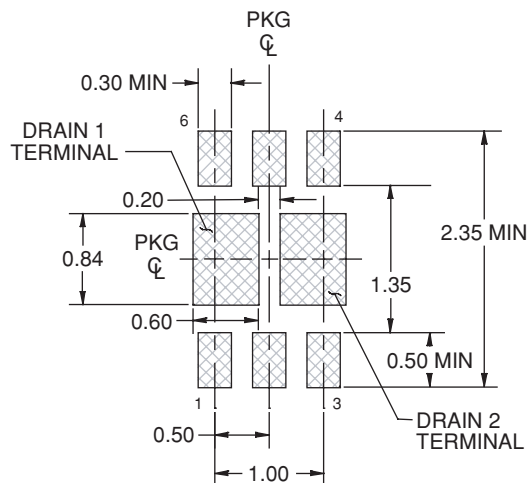
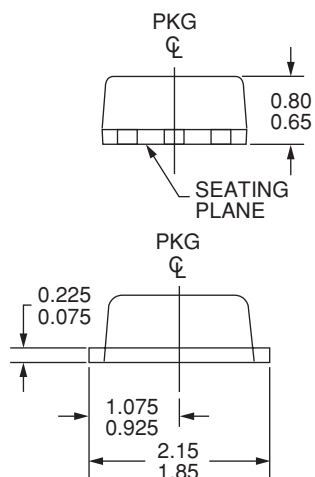
## Dimensional Outline and Pad Layout



**Bottom View**



**Top View**



**Recommended Landing Pattern**

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