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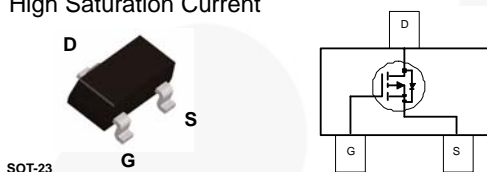


# BSS84

## P-Channel Enhancement Mode Field-Effect Transistor

### Features

- -0.13 A, -50 V,  $R_{DS(ON)} = 10 \Omega$  at  $V_{GS} = -5$  V
- Voltage-Controlled P-Channel Small-Signal Switch
- High-Density Cell Design for Low  $R_{DS(ON)}$
- High Saturation Current



### Description

This P-channel enhancement-mode field-effect transistor is produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process minimizes on-state resistance and to provide rugged and reliable performance and fast switching. The BSS84 can be used, with a minimum of effort, in most applications requiring up to 0.13 A DC and can deliver current up to 0.52 A. This product is particularly suited to low-voltage applications requiring a low-current high-side switch.

### Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-Source Voltage	-50	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current <sup>(1)</sup>	Continuous	-0.13
		Pulsed	-0.52
$P_D$	Maximum Power Dissipation <sup>(1)</sup>	0.36	W
	Derate Above $25^\circ\text{C}$	2.9	mW / $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient <sup>(1)</sup>	350	$^\circ\text{C}/\text{W}$
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**Note:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the user's board design.



a)  $350^\circ\text{C}/\text{W}$  when mounted on a minimum pad

Scale 1: 1 on letter-size paper.

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
SP	BSS84	7"	8mm	3000

Electrical Characteristics<sup>(2)</sup>

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to 25°C		-48		mV / °C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}$			-15	$\mu\text{A}$
		$V_{DS} = -50\text{ V}, V_{GS} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$			-60	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage.	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	nA
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-50			V
<b>On Characteristics<sup>(2)</sup></b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -1\text{ mA}$	-0.8	-1.7	-2	V
$\frac{V_{GS(TH)}}{T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -1\text{ mA}$ , Referenced to 25°C		3		mV / °C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -5\text{ V}, I_D = -0.10\text{ A}$		1.2	10.0	$\Omega$
		$V_{GS} = -5\text{ V}, I_D = -0.10\text{ A}$ , $T_J = 125^\circ\text{C}$		1.9	17.0	$\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -5\text{ V}, V_{DS} = -10\text{ V}$	-0.6			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -25\text{ V}, I_D = -0.10\text{ A}$	0.05	0.60		S
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{DS} = -25\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$		73		pF
$C_{OSS}$	Output Capacitance			10		pF
$C_{RSS}$	Reverse Transfer Capacitance			5		pF
$R_G$	Gate Resistance	$V_{GS} = -15\text{ mV}, f = 1.0\text{ MHz}$		9		$\Omega$
<b>Switching Characteristics<sup>(2)</sup></b>						
$t_{d(on)}$	Turn–On Delay	$V_{DD} = -30\text{ V}, I_D = -0.27\text{ A}$ , $V_{GS} = -10\text{ V}, R_{GEN} = 6$		2.5	5.0	ns
$t_r$	Turn–On Rise Time			6.3	13.0	ns
$t_{d(off)}$	Turn–Off Delay			10	20	ns
$t_f$	Turn–Off Fall Time			4.8	9.6	ns
$Q_g$	Total Gate Charge			0.9	1.3	nC
$Q_{gs}$	Gate–Source Charge	$V_{DS} = -25\text{ V}, I_D = -0.10\text{ A}$ , $V_{GS} = -5\text{ V}$		0.2		nC
$Q_{gd}$	Gate–Drain Charge			0.3		nC
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-0.13	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.26\text{ A}^{(2)}$		-0.8	-1.2	V
$t_{RR}$	Diode Reverse–Recovery Time	$I_F = -0.1\text{ A}$ , $dI_F / dt = 100\text{ A} / \mu\text{s}^{(2)}$		10		ns
$Q_{RR}$	Diode Reverse–Recovery Charge			3		nC

**Note:**

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

### Typical Characteristics

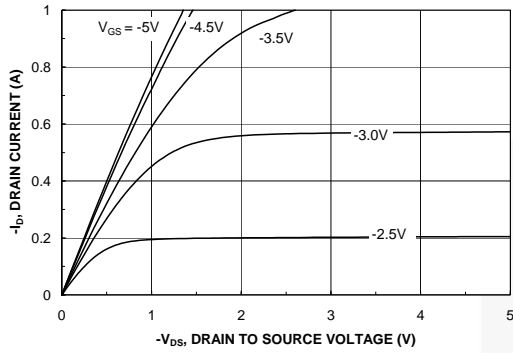


Figure 1. On-Region Characteristics

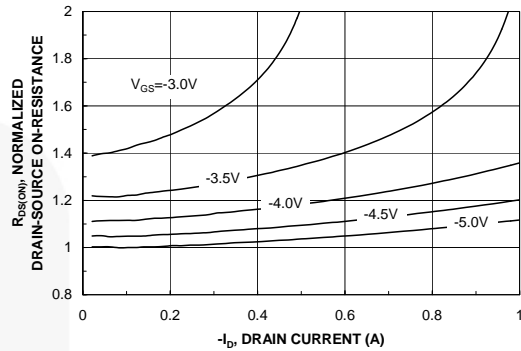


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

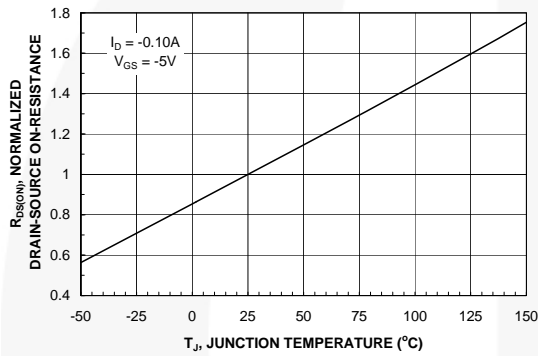


Figure 3. On-Resistance Variation with Temperature

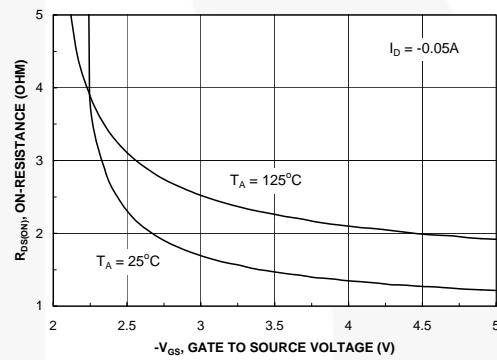


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

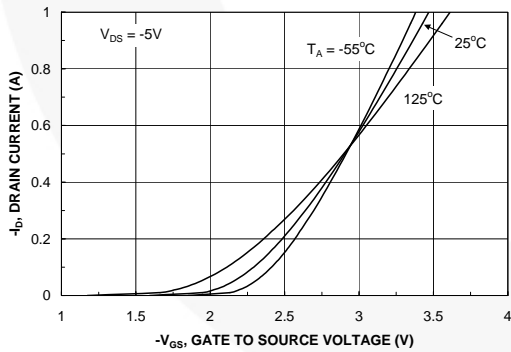


Figure 5. Transfer Characteristics

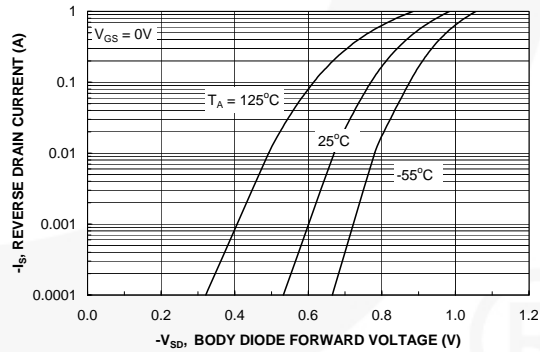
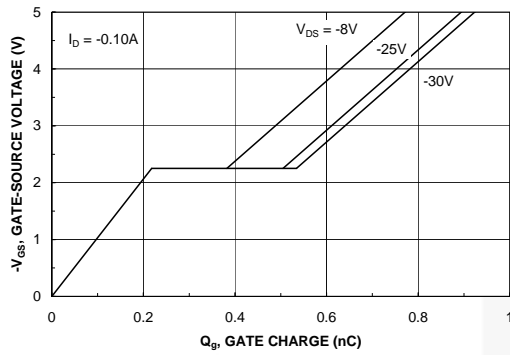
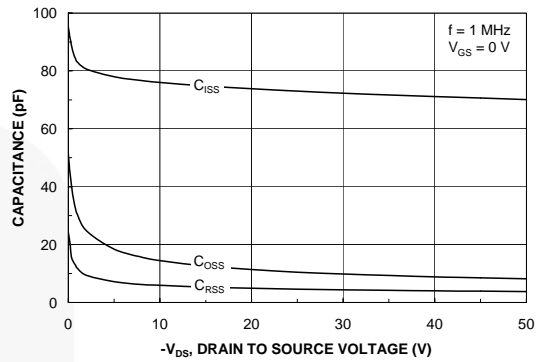


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

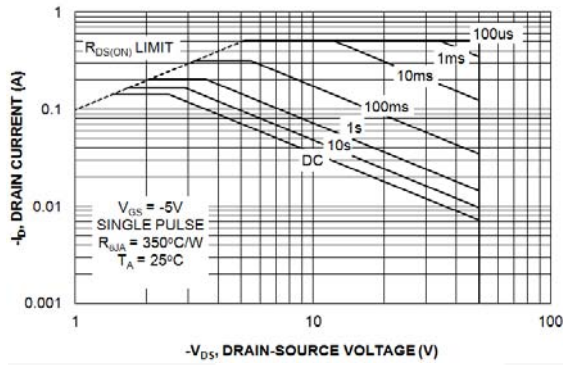
**Typical Characteristics (Continued)**



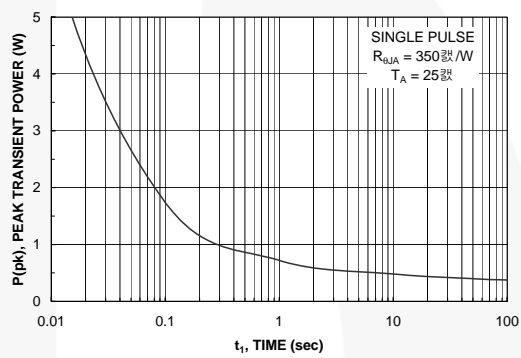
**Figure 7. Gate Charge Characteristics**



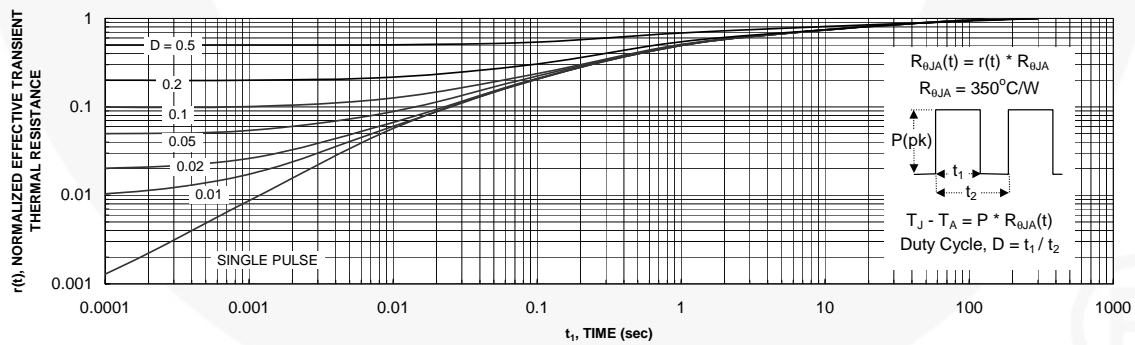
**Figure 8. Capacitance Characteristics**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Single-Pulse Maximum Power Dissipation**



**Figure 11. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described on page 1. Transient thermal response will change depending on the circuit board design.

Physical Dimension

SOT-23 3L

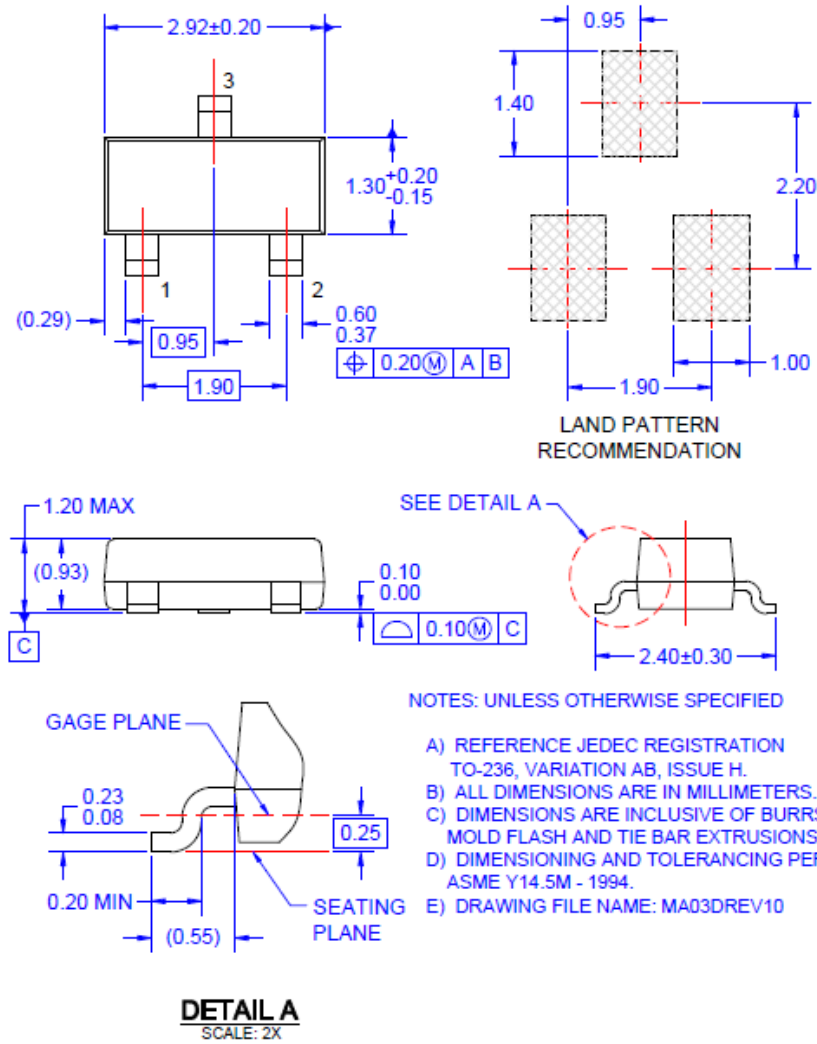


Figure 12. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE

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