



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at

www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

FSSD06 — SD/SDIO and MMC Two-Port Multiplexer

Features

- On Resistance Typically 4Ω, $V_{DDH}=2.7V$
- $f_{toggle} > 120MHz$
- Low On Capacitance: 9pF Typical
- Low Power Consumption: 1μA Maximum
- Conforms to Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) Specifications
- Supports 1-Bit / 4-Bit Host Controllers ($V_{DDH}=1.65V$ to 3.6V) Communicating with High-Voltage (2.7-3.6V) and Dual-Voltage Cards (1.65-1.95V, 2.7-3.6V)
 - $V_{DDH}=1.65$ to 3.6V, $V_{DDC1/C2}=V_{DDH}$ to 3.6V
- 24-Lead MLP (3.5 x 4.5mm) and UMLP Packages

Applications

- Cell Phone, PDA, Digital Camera, Portable GPS
- LCD Monitor, Home Theater PC/TV, All-in-One Printer

Description

The FSSD06 is a two-port multiplexer that allows Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) host controllers to be expanded out to multiple cards or peripherals. This configuration enables the CMD, CLK, and D[3:0] signals to be multiplexed to dual-card peripherals. It is optimized for 1-bit / 4-bit SD / MMC applications.

The architecture includes the necessary bi-directional data and command transfer capability for single high-voltage cards or dual-voltage supply cards. The clock path for the FSSD06 is a uni-directional buffer with an integrated pull-up for high-impedance mode.

Typical applications involve switching in portables and consumer applications: cell phones, digital cameras, home theater monitors, portable GPS units, and printers.

Analog Symbol Diagram

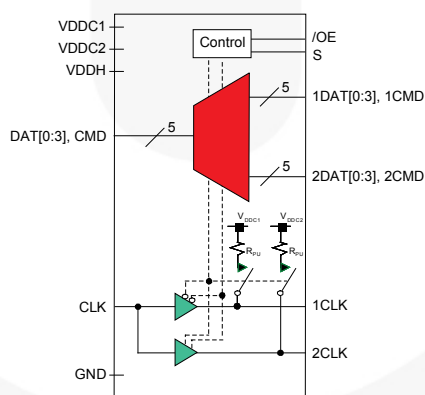


Figure 1. Analog Symbol Diagram

Ordering Information

Part Number	Operating Temperature Range	Package Description	Packing Method
FSSD06BQX	-40°C to +85°C	24-Lead Molded Leadless Package (MLP), JEDEC MO-220, 3.5 x 4.5mm	Tape & Reel
FSSD06UMX	-40°C to +85°C	24-Lead Ultrathin Molded Leadless Package (UMLP)	Tape & Reel

Pin Configuration

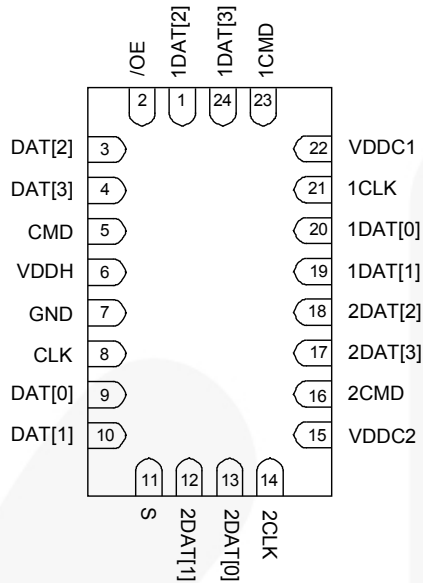


Figure 2. MLP Pin Assignments

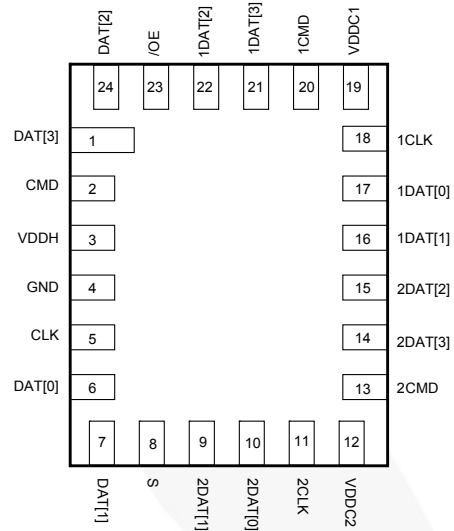


Figure 3. UMLP Pin Assignments

Pin Definitions

Name	Description
VDDH	Power Supply (Host ASIC)
VDDC1, VDDC2	Power Supply (SDIO Peripheral Card Ports)
/OE	Output Enable (Active Low)
S	Select Pin
1DAT[3:0], 2DAT[3:0], 1CMD, 2CMD	SDIO Card Ports
DAT[3:0], CMD	SDIO Common Ports
CLK, 1CLK, 2CLK	Clock Path Ports

Truth Table

/OE	S	Function
LOW	LOW	CMD, CLK, DAT[3:0] connected to 1CMD, 1CLK, 1DAT[3:0]; 2CLK pulled HIGH via R _{PU}
LOW	HIGH	CMD, CLK, DAT[3:0] connected to 2CMD, 2CLK, 2DAT[3:0]; 1CLK pulled HIGH via R _{PU}
HIGH	X	All Ports High Impedance; 1CLK, 2CLK pulled HIGH via R _{PU}

Typical Application Diagram

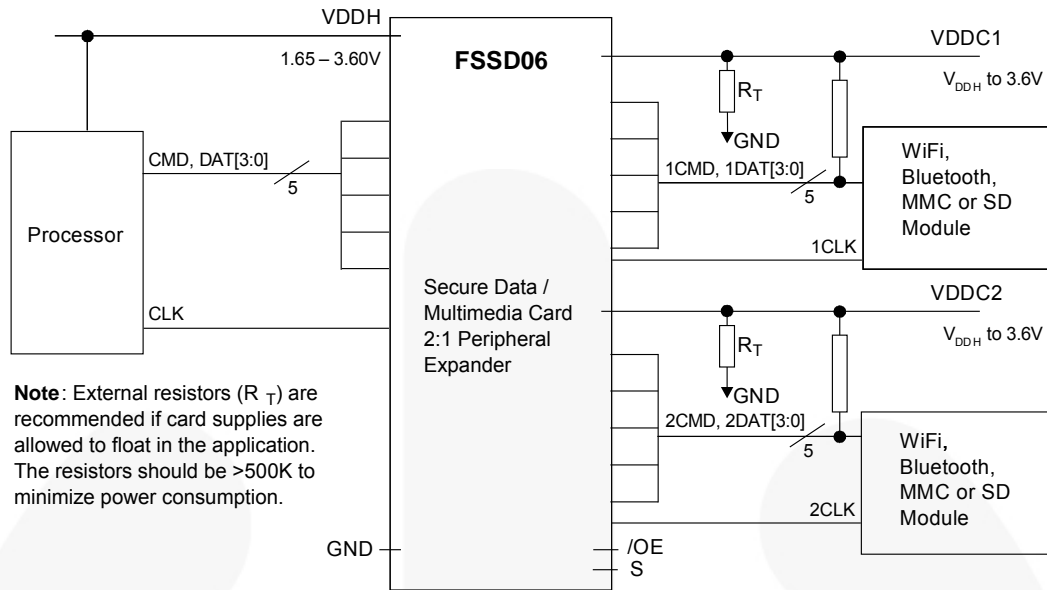


Figure 4. Typical Application Diagram

Functional Description

The FSSD06 enables sharing the ASIC/baseband processor SDIO port(s) to two peripheral cards, providing bi-directional support for dual-voltage SD/SDIO or MMC cards available in the marketplace. Each SDIO port of the FSSD06 has its own supply rail, allowing peripheral cards with different supplies to be interfaced to the host. The peripheral card supplies must be equal or greater than the host to minimize power consumption. The independent V_{DDH} , V_{DDC1} , and V_{DDC2} are defined by the supplies connected from the application Power Management ICs (PMICs) to the FSSD06. The clock path is a uni-directional buffered path rather than a bi-directional switch port.

CMD, DAT Bus Pull-ups

The 1CMD, 2CMD, 1DAT[3:0], and 2DAT[3:0] ports do not have, internally, the system pull-up resistors as defined in the MMC or SD card system bus specifications. The system bus pull-up must be added external to the FSSD06. The value, within the specific specification limits, is a function of the individual application and type of card or peripheral connected. For SD card applications, the R_{CMD} and R_{DAT} pull-ups should be between 10k Ω and 100k Ω . For MMC applications, the R_{CMD} pull-ups should be between 4.7k Ω and 100k Ω and the R_{DAT} pull-ups between 50k Ω and 100k Ω . The card-side 1CMD, 2CMD, 1DAT[3:0], and 2DAT[3:0] outputs have a circuit that facilitates incident wave switching, so the external pull-up resistors ensure retention of the output high level.

The /OE pin can be used to place the 1CMD, 2CMD, 1DAT[3:0] and 2DAT[3:0] into high-impedance mode when the system enters IDLE state (see *IDLE State CMD/DAT Bus "Parking"*).

CLK Bus

The 1CLK and 2CLK outputs are bi-state buffer architectures, rather than a switch I/O, to ensure 52MHz incident wave switching. When there is no communication on the bus (IDLE), the FSSD06 can be disabled with the /OE pin. When this pin is pulled HIGH, the nCLK outputs are also pulled HIGH. Along with nCMD, nDAT[3:0] goes high-impedance to ensure that the CLK path between the FSSD06 and the peripheral does not float.

IDLE State CMD/DAT Bus "Parking"

The SD and MMC card specifications were written for a direct point-to-point communication between host controller and card. The introduction of the FSSD06 in that path, as an expander, requires that the functional operation and system latency not be impacted by the FSSD06 switch characteristics. Since there are various card formats, protocols, and configurable controllers, a /OE pin is available to facilitate a fast IDLE transition for the nCMD/nDAT[3:0] outputs. Some controllers, rather than simply placing CMD/DAT into high-impedance mode, may pull their outputs HIGH for a clock cycle prior to going into high-impedance mode (referred to as "parking" the output). Some legacy controllers pull their outputs HIGH versus high impedance.

If the /OE pin is left LOW and the controller places the CMD/DAT[3:0] outputs into high impedance, the nCMD/nDAT[3:0] output rise time is a function of the RC time constant through the switch path. It is recommended that the host controller pull CMD and DAT[3:0] HIGH for one cycle before pulling /OE HIGH. This facilitates parking all nCMD/nDAT[3:0] outputs HIGH before putting the switch I/Os in high impedance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DDH}	Supply Voltage		-0.5	4.6	V
V_{DDC1}, V_{DDC2}	Supply Voltage		-0.5	4.6	V
$V_{SW}^{(1)}$	Switch I/O Voltage	1DAT[3:0], 2DAT[3:0], 1CMD, 2CMD Pins	-0.5	$V_{DDX}^{(2)} + 0.3V$ (4.6V maximum)	V
		DAT[3:0], CMD Pins	-0.5	$V_{DDX}^{(2)} + 0.3V$ (4.6V maximum)	V
$V_{CNTRL}^{(1)}$	Control Input Voltage	S, /OE	-0.5	4.6	V
$V_{CLKI}^{(1)}$	CLK Input Voltage	CLK	-0.5	4.6	V
$V_{CLKO}^{(1)}$	CLK Output Voltage	1CLK, 2CLK	-0.5	$V_{DDX}^{(2)} + 0.3V$ (4.6V maximum)	V
I_{INDC}	Input Clamp Diode Current			-50	mA
I_{SW}	Switch I/O Current	SDIO Continuous		50	mA
I_{SWPEAK}	Peak Switch Current	SDIO Pulsed at 1ms Duration, <10% Duty Cycle		100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Max Junction Temperature			+150	°C
T_L	Lead Temperature	Soldering, 10 Seconds		+260C	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	I/O to GND		8	kV
		Supply to GND		9	
		All Other Pins		5	
	Charged Device Model (JEDEC: JESD22-C101)			2	kV

Notes:

- The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
- V_{DDX} references the specific SDIO port V_{DD} rail (i.e. V_{DDC1} , V_{DDC2} , V_{DDH}).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DDH}	Supply Voltage - Host Side	1.65	3.6V	V
V_{DDC1}, V_{DDC2}	Supply Voltage - SDIO Cards	V_{DDH}	3.6V	V
V_{CNTRL}	Control Input Voltage - $V_S, V_{/OE}$	0	V_{DDH}	V
V_{CLKI}	Clock Input Voltage - V_{CLKI}	0	V_{DDH}	V
V_{SW}	Switch I/O Voltage - CMD, DAT[3:0]	0	V_{DDH}	V
	Switch I/O Voltage - 1CMD, 1DAT[3:0]	0	V_{DDC1}	V
	Switch I/O Voltage - 2CMD, 2DAT[3:0]	0	V_{DDC2}	V
°C	Operating Temperature	-40	+85	°C
θ_{JA}	Thermal Resistance (free air), MLP24		50	°C/W

DC Electrical Characteristics at 1.8V V_{DDH}

All typical values are for V_{DDH}=1.8V at 25°C unless otherwise specified.

Symbol	Parameter	V _{VDDC1} / V _{VDDC2} (V)	Conditions	T _A =- 40°C to +85°C			Unit
				Min.	Typ.	Max.	
Common Pins							
V _{IK}	Clamp Diode Voltage	2.7	I _{IK} =-18mA			-1.2	V
V _{IH}	Control Input Voltage High	2.7	V _{DDH} =1.65V	1.3			
V _{IL}	Control Input Voltage Low	2.7				0.5	
I _{IN}	S, /OE Input High Current	3.6	V _{DDH} =1.95V, V _{CNTRL} =0V to V _{DDH}	-1		1	μA
I _{OZ}	Off Leakage, Current of all ports	3.6	V _{DDH} =1.95V, V _{SW} =0V to V _{DDX}	-1.0	0.5	1.0	μA
I _{PU}	CLK Pull-up Current	3.6	V _{CLKI} =V _{DDH} , V _{CLKO} =0V, /OE=V _{DDH}			35	μA
V _{OHC}	CLK Output Voltage High	2.7	I _{OH} =-2mA	2.4			V
V _{OLC}	CLK Output Voltage Low	3.6	I _{OL} =-2mA			90	mV
R _{PU}	CLK Pull-up Resistance ⁽³⁾			50	100		kΩ
R _{ON}	Switch On Resistance ⁽⁴⁾	2.7	V _{CMD, DAT[3:0]} =0V, I _{ON} =-2mA, See Figure 5		4	6	Ω
ΔR _{ON}	Delta On Resistance ^(4, 5)	2.7	V _{CMD, DAT[3:0]} =0V, I _{ON} =- 2mA		0.8		Ω
Power Supply							
I _{CC(VDDH)}	Quiescent Supply Current (Host)	0	V _{DDH} =1.95V, V _{SW} =0 or V _{DDH} , I _{OUT} =0			1	μA
I _{CC(VDDC1, VDDC2)}	Quiescent Supply Current (SDIO Cards)	3.6	V _{SW} =0 or V _{DDX} , I _{OUT} =0, V _{CLKI} =V _{DDH} , V _{CLKO} =Open, /OE=0V			1	μA
ΔI _{CARD}	Delta I _{CC(VDDC1, VDDC2)} for One Card Powered Off	3.6V / 0V	V _{SW} =0 or V _{DDX} , I _{OUT} =0, V _{CLKI} =V _{DDH} , V _{CLKO} =Open, /OE=0V			1	μA

Notes:

3. Guaranteed by characterization, not production tested.
4. On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.
5. Δ R_{ON}=R_{ON max} – R_{ON min} measured at identical V_{CC}, temperature, and voltage.

DC Electrical Characteristics at 2.7V V_{DDH}

All typical values are for $V_{DDH}=2.7V$ at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC1} / V_{DDC2} (V)	Conditions	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
Common Pins							
V_{IK}	Clamp Diode Voltage	2.7	$I_{IK}=-18mA$			-1.2	V
V_{IH}	Control Input Voltage High	2.7	$V_{DDH}=2.7V$	1.8			
V_{IL}	Control Input Voltage Low	2.7				0.8	
I_{IN}	S, /OE Input High Current	3.6	$V_{DDH}=3.6V, V_{CNTRL}=0V$ to V_{DDH}	-1		1	μA
I_{OZ}	Off Leakage Current of all ports	3.6	$V_{DDH}=3.6V, V_{SW}=0V$ to V_{DDX}	-1.0	0.5	1.0	μA
I_{PU}	CLK Pull-up Current	3.6	$V_{CLKI}=V_{DDH}, V_{CLKO}=0V, /OE=V_{DDH}$			50	μA
V_{OHC}	CLK Output Voltage High	2.7	$I_{OH}=-2mA$	2.4			V
V_{OLC}	CLK Output Voltage Low	3.6	$I_{OL}=-2mA$			90	mV
R_{PU}	CLK Pull-up Resistance ⁽⁶⁾			50	100		k Ω
R_{ON}	Switch On Resistance ⁽⁷⁾	2.7	$V_{CMD, DAT[3:0]}=0V, I_{ON}=-2mA$ See Figure 5		2.5	6.0	Ω
ΔR_{ON}	Delta On Resistance ^(7,8)	2.7	$V_{CMD, DAT[3:0]}=0V, I_{ON}=-2mA$		0.8		Ω
Power Supply							
$I_{CC(VDDH)}$	Quiescent Supply Current (Host)	0	$V_{DDH}=3.6V, V_{SW}=0$ or $V_{DDH}, I_{OUT}=0$			1	μA
$I_{CC(VDDC1, VDDC2)}$	Quiescent Supply Current (SDIO Cards)	3.6	$V_{SW}=0$ or $V_{DDX}, I_{OUT}=0, V_{CLKI}=V_{DDH}, V_{CLKO}=Open, /OE=0V$			1	μA
ΔI_{CARD}	Delta $I_{CC(VDDC1, VDDC2)}$ for One Card Powered Off	3.6V/0V 0V/3.6V	$V_{SW}=0$ or $V_{DDX}, I_{OUT}=0, V_{CLKI}=V_{DDH}, V_{CLKO}=Open, /OE=0V$			1	μA

Notes:

- Guaranteed by characterization, not production tested.
- On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.
- $\Delta R_{ON}=R_{ON\ max}-R_{ON\ min}$ measured at identical V_{CC} , temperature, and voltage.

AC Electrical Characteristics at 1.8V V_{DDH}

All typical values are for $V_{DDH}=1.8V$ at 25°C unless otherwise specified.

Symbol	Parameter	$V_{DDC1}/$ V_{DDC2} (V)	Conditions	$T_A=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
				Min.	Typ.	Max.	
t_{ON1}	Turn-On Time, S, /OE to CMD, DAT[3:0]	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		10	24	ns
t_{OFF1}	Turn-Off Time, S, /OE to CMD, DAT[3:0]	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		7	22	ns
t_{PD}	Switch Propagation Delay ⁽⁹⁾	2.7 to 3.6	See Figure 9		1		ns
t_{SKEW}	Switch Skew ^(9, 10) CMD, DAT[3:0]	2.7 to 3.6	$R_L=1k\Omega$, $C_L=30pF$		2		ns
t_{ON2}	Turn-On Time, S, /OE to 1CLK, 2CLK	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		17	35	ns
t_{OFF2}	Turn-Off Time S, /OE to 1CLK, 2CLK	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		10	28	ns
t_{PDCLK}	Clock Propagation Delay	2.7 to 3.6	$R_L=1k\Omega$, $C_L=30pF$ See Figure 11		3.0	5.5	ns
O_{IRR}	Off Isolation ⁽⁹⁾	2.7 to 3.6	$f=10MHz$, $R_T=50\Omega$, $C_L=30pF$, See Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk ⁽⁹⁾	2.7 to 3.6	$f=10MHz$, $R_T=50\Omega$, $C_L=30pF$, See Figure 13		-60		dB
f_{toggle}	Clock Frequency ⁽⁹⁾	2.7 to 3.6	$C_L=30pF$		120		MHz

Notes:

9. Guaranteed by characterization, not production tested.
 10. Skew is determined by $|T_{PLH} - T_{PHL}|$ for worst-case temperature and V_{DDX} .

AC Electrical Characteristics at 2.7V V_{DDH}

All typical values are for $V_{DDH}=2.7V$ at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC1}/V_{DDC2} (V)	Conditions	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
				Min.	Typ.	Max.	
t_{ON1}	Turn-On Time S, /OE to CMD, DAT[3:0]	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		8	17	ns
t_{OFF1}	Turn-Off Time S, /OE to CMD, DAT[3:0]	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		6	13	ns
t_{PD}	Switch Propagation Delay ⁽¹¹⁾	2.7 to 3.6	See Figure 9		1		ns
t_{SKEW}	Switch Skew ⁽¹²⁾ CMD, DAT[3:0]	2.7 to 3.6	$R_L=1k\Omega$, $C_L=30pF$		1.5		ns
t_{ON2}	Turn-On Time S, /OE to 1CLK, 2CLK	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		15	25	ns
t_{OFF2}	Turn-Off Time S, /OE to 1CLK, 2CLK	2.7 to 3.6	$V_{SW}=0V$, $R_L=1k\Omega$, $C_L=30pF$ See Figure 7, Figure 8		10	25	ns
t_{PDCLK}	Clock Propagation Delay	2.7 to 3.6	$R_L=1k\Omega$, $C_L=30pF$ See Figure 11		1.5	3.0	ns
O_{IRR}	Off Isolation ⁽¹¹⁾	2.7 to 3.6	$f=10MHz$, $R_T=50\Omega$, $C_L=30pF$ See Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk ⁽¹¹⁾	2.7 to 3.6	$f=10MHz$, $R_T=50\Omega$, $C_L=30pF$ See Figure 13		-60		dB
f_{toggle}	Clock Frequency ⁽¹¹⁾	2.7 to 3.6	$C_L=30pF$		120		MHz

Notes:

11. Guaranteed by characterization, not production tested.
12. Skew is determined by $|T_{PLH} - T_{PHL}|$ for worst-case temperature and V_{DDX} .

Capacitance

Symbol	Parameter	Conditions	$T_A=-40^{\circ}C$ to $+85^{\circ}C$			Unit
			Min.	Typ.	Max.	
$C_{IN(S, /OE, CLK)}$	Control and CLK Pin Input Capacitance	$V_{DDH}=0V$		2.5		pF
C_{ON}	Common Port On Capacitance ($C_{DAT[3:0], CMD}$)	$V_{DDH}=1.8V$, $V_{DDC1}=V_{DDC2}=2.7V$, $V_{/OE}=0V$, $V_{bias}=0V$, $f=1MHz$ See Figure 15		9.0		
C_{OFF}	Input Source Off Capacitance	$V_{DDH}=1.8V$, $V_{DDC1}=V_{DDLH2}=2.7V$, $V_{/OE}=3.3V$, $V_{bias}=0V$, $f=1MHz$ See Figure 14		4.0		

Test Diagrams

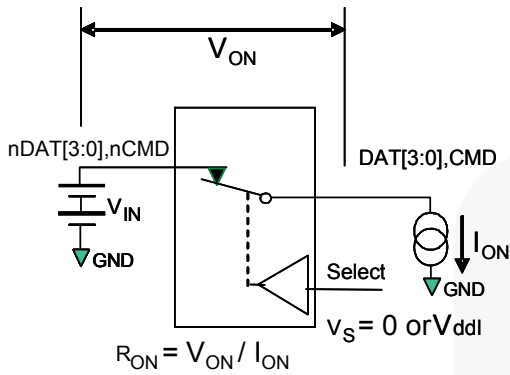


Figure 5. On Resistance

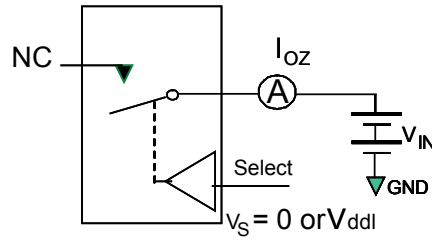
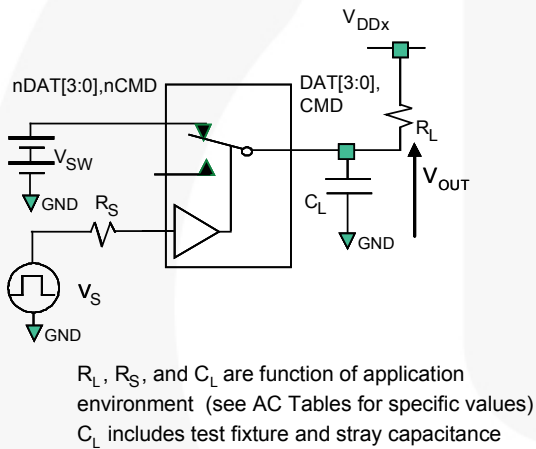


Figure 6. Off Leakage (Each Switch Port is Tested Separately)



R_L , R_S , and C_L are function of application environment (see AC Tables for specific values)
 C_L includes test fixture and stray capacitance

Figure 7. AC Test Circuit Load

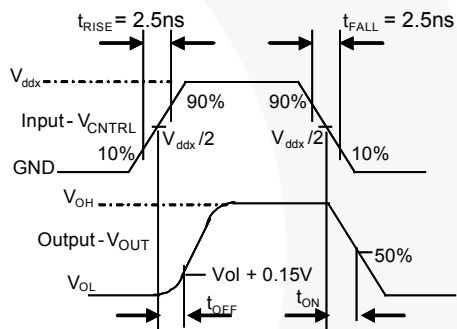


Figure 8. Turn On/Off Time Waveforms

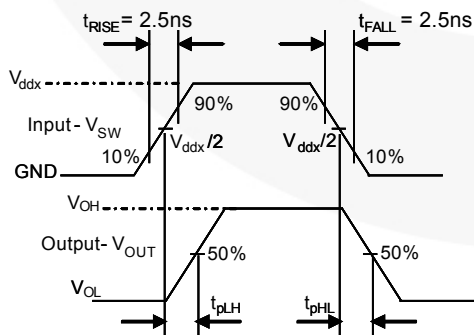
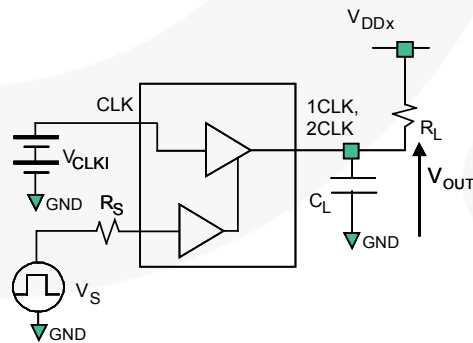


Figure 9. Switch Propagation Delay Waveform



R_L , R_S , and C_L are function of application environment (see AC Tables for specific values)
 C_L includes test fixture and stray capacitance

Figure 10. AC Test Circuit Load (CLK)

Test Diagrams (Continued)

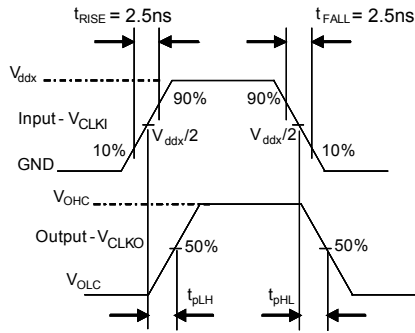


Figure 11. CLK Propagation Delay Waveforms

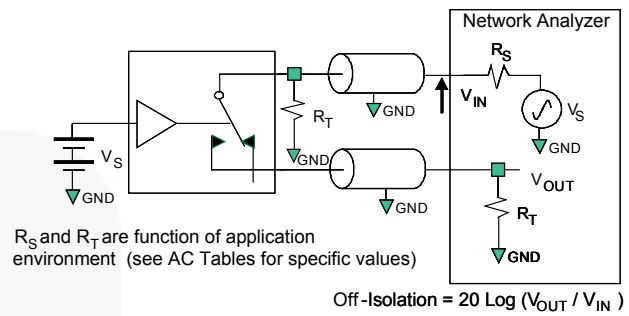


Figure 12. Channel Off Isolation

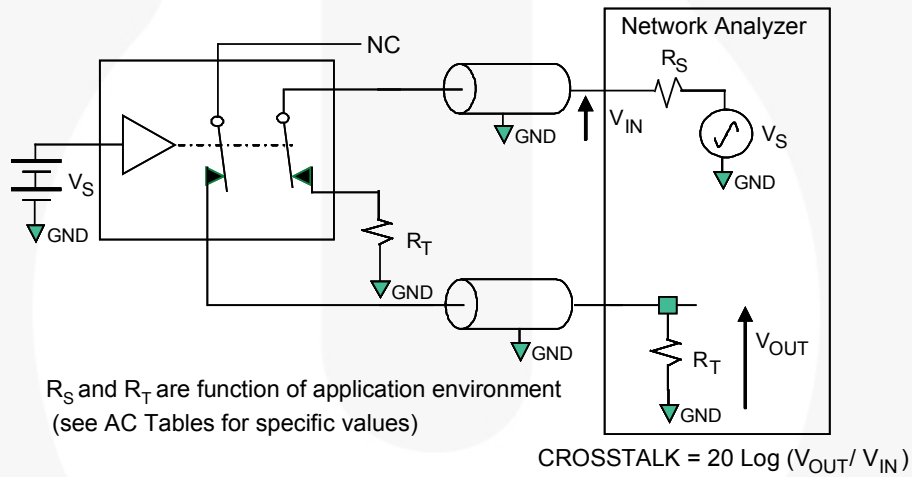


Figure 13. Channel-to-Channel Crosstalk

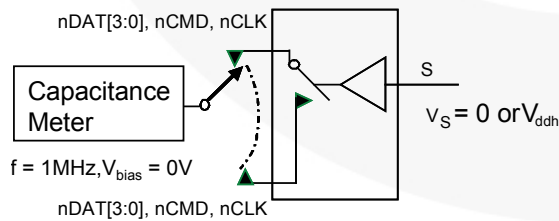


Figure 14. Channel Off Capacitance

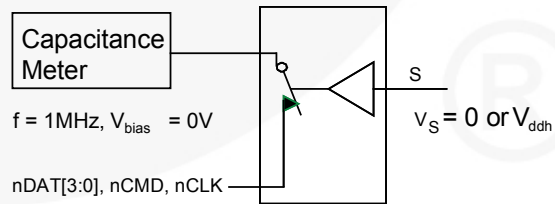


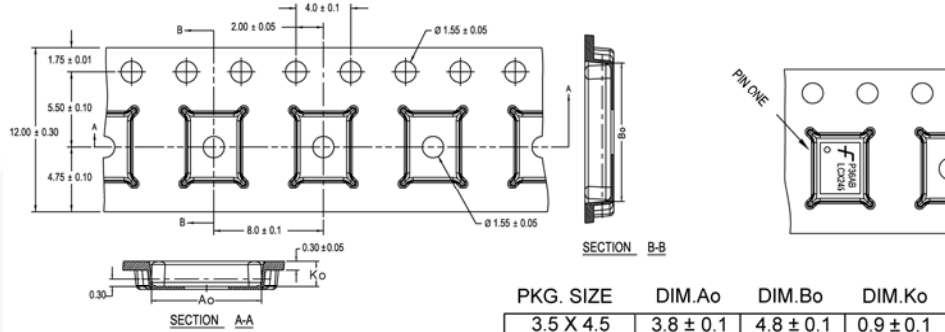
Figure 15. Channel On Capacitance

Tape and Reel Specifications

Package Designator	Tape Selection	Number Cavities	Cavity Status	Cover Tape Status
MPX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Tape Dimensions

Dimensions are in millimeters unless otherwise noted.



PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

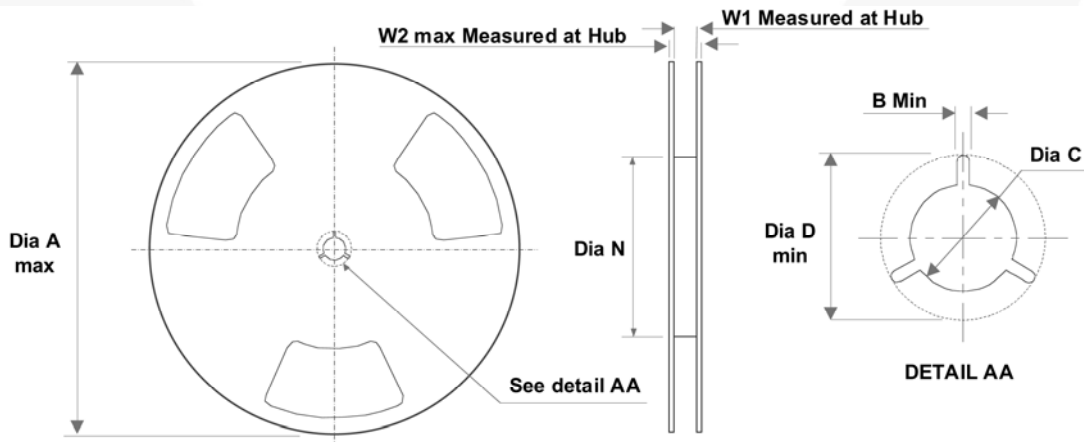
DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is $\pm 0.002[0.05]$ for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Reel Dimensions

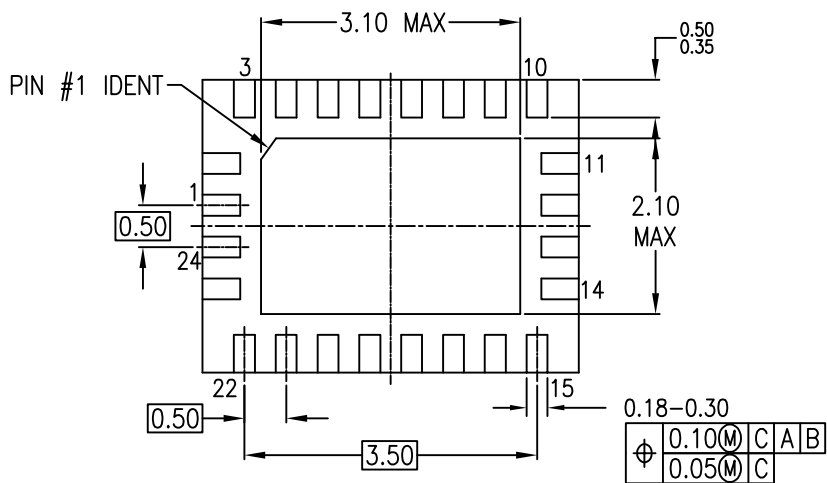
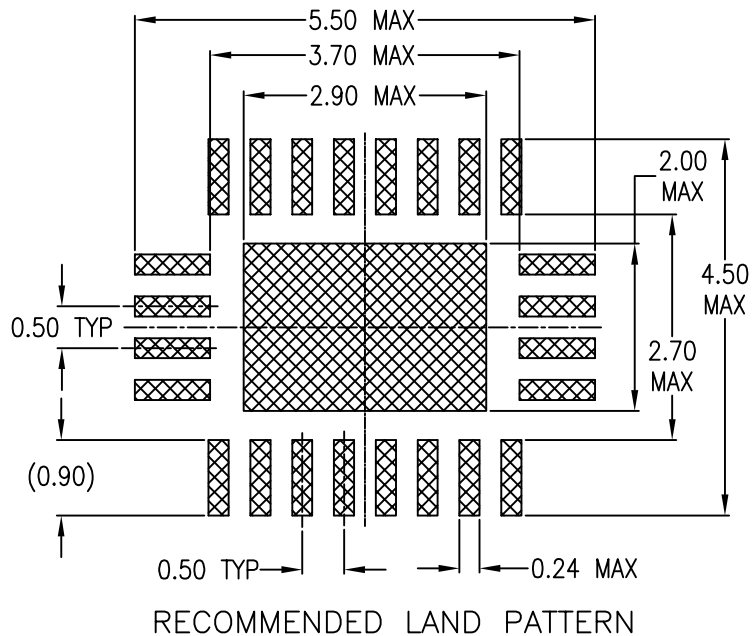
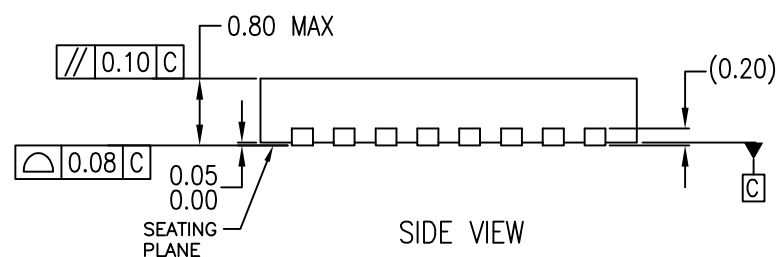
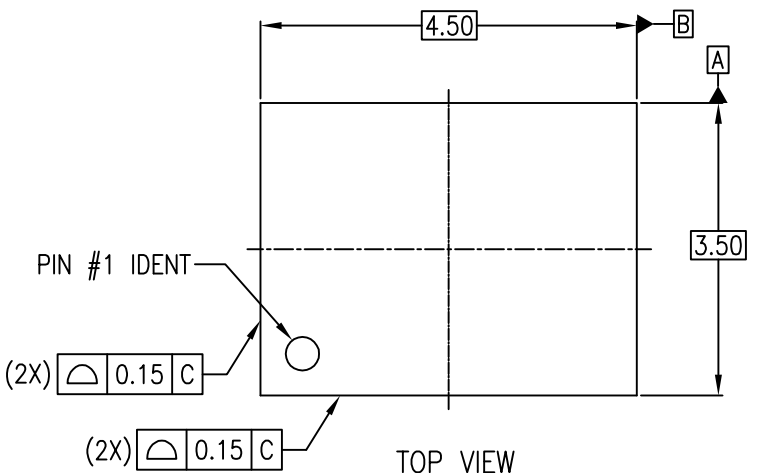
Dimensions are in inches (millimeters) unless otherwise noted.



Tape Size	A	B	C	D	N	W1	W2
	13.000	0.059	0.512	0.795	2.165	0.488	0.724
(12.00mm)	(330.00)	(1.50)	(13.00)	(20.00)	(55.00)	(12.40)	(18.40)

THIS DRAWING IS THE PROPERTY OF FAIRCHILD SEMICONDUCTOR CORPORATION. NO USE THEREOF SHALL BE MADE OTHER THAN AS A REFERENCE FOR PROPOSALS AS SUBMITTED TO FAIRCHILD SEMICONDUCTOR CORPORATION FOR JOBS TO BE EXECUTED IN CONFORMITY WITH SUCH PROPOSALS UNLESS THE CONSENT OF SAID FAIRCHILD SEMICONDUCTOR CORPORATION HAS PREVIOUSLY BEEN OBTAINED. NO PART OF THIS DRAWING SHALL BE COPIED OR DUPLICATED OR ITS CONTENTS DISCLOSED. THE INFORMATION CONTAINED ON THIS DRAWING IS CONFIDENTIAL AND PROPRIETARY.

REVISIONS				
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		7-4-2003	FEITAN
B	REVISE DWG NAME AND NOTE 1.		12-11-2003	FEITAN
C	CORRECTED PIN NUMBERING AND DAP DIM REMOVED LAND PATTERN NUMBERING. REVISED NOTE 1. TOP VIEW ADDED PIN #1 DOT		17-11-2003	HALLÉN
4	CORRECTED THE LEAD LENGTH FROM 0.35~0.75 TO 0.35~0.50		26 JAN 2007	CHIPKING

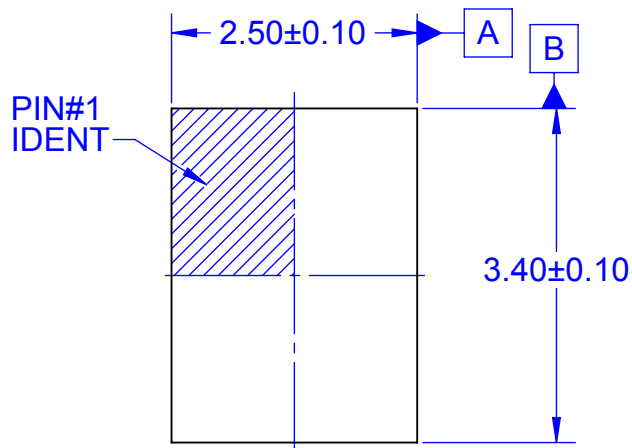


NOTES:

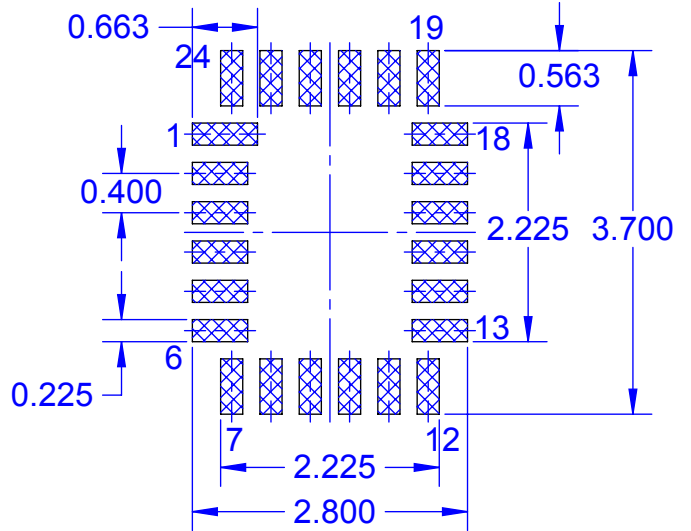
- A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WFS-2 FOR DIMENSIONS ONLY. PIN NUMBERING DOES NOT COMPLY.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP24Brev4

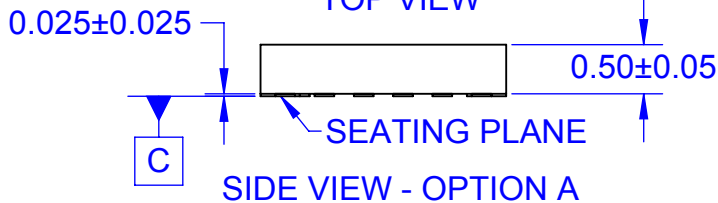
APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR			
DRAWN FEITAN	31-3-2003	Bayan Lepas, FIZ, 11900, Penang, Malaysia.			
DFTG. CHK.		24LD, MLP, QUAD, JEDEC MO-220, 3.5x4.5 MM			
ENGR. CHK.					
PROJECTION		SCALE	SIZE	DRAWING NUMBER	REV
INCH MM		N/A	N/A	MKT-MLP24B	4
DO NOT SCALE DRAWING				SHEET 1 of 1	



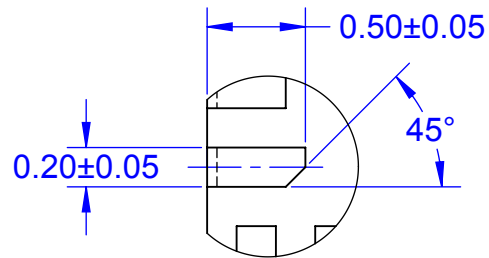
TOP VIEW



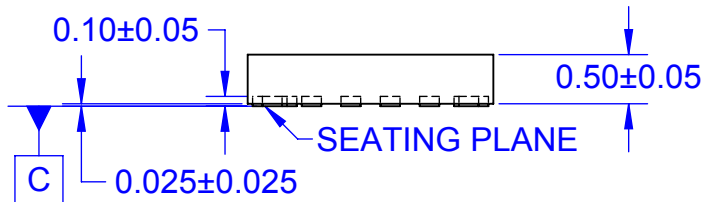
LAND PATTERN RECOMMENDATION



SIDE VIEW - OPTION A



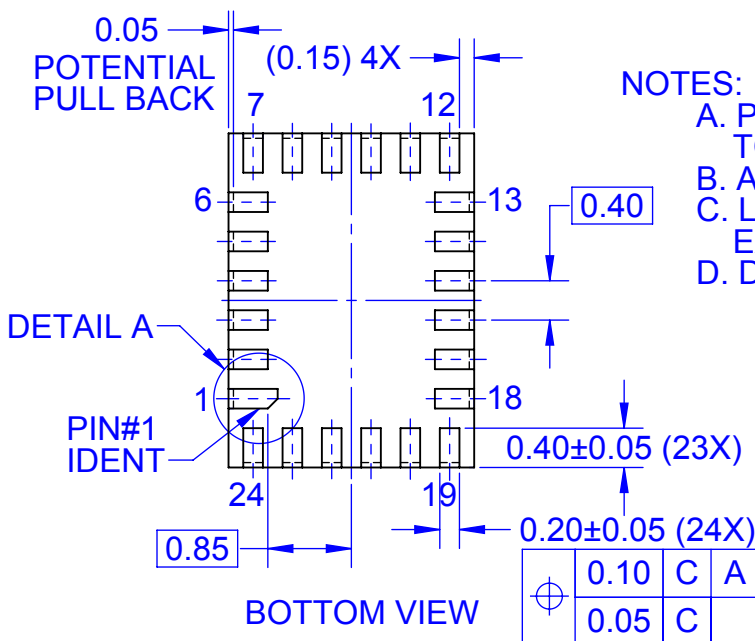
DETAIL A
SCALE 2:1



SIDE VIEW - OPTION B

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- D. DRAWING FILENAME: MKT-UMLP24ArevE



BOTTOM VIEW

⊕	0.10	C	A	B
	0.05	C		

ON Semiconductor



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative