



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at

www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



FDMS7600AS

Dual N-Channel PowerTrench[®] MOSFET

N-Channel: 30 V, 30 A, 7.5 mΩ N-Channel: 30 V, 40 A, 2.8 mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 7.5 mΩ at $V_{GS} = 10$ V, $I_D = 12$ A
- Max $r_{DS(on)}$ = 12 mΩ at $V_{GS} = 4.5$ V, $I_D = 10$ A

Q2: N-Channel

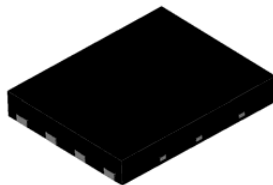
- Max $r_{DS(on)}$ = 2.8 mΩ at $V_{GS} = 10$ V, $I_D = 20$ A
- Max $r_{DS(on)}$ = 3.3 mΩ at $V_{GS} = 4.5$ V, $I_D = 18$ A
- RoHS Compliant

General Description

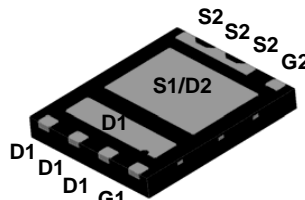
This device includes two specialized N-Channel MOSFETs in a dual MLP package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET[™] (Q2) have been designed to provide optimal power efficiency.

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook V_{CORE}

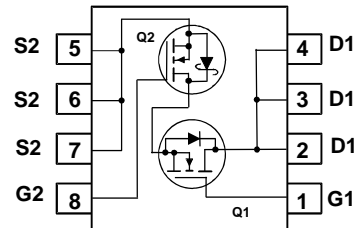


Top



Bottom

Power 56



MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	30	30	V
V_{GS}	Gate to Source Voltage (Note 3)	± 20	± 20	V
I_D	Drain Current -Continuous $T_C = 25$ °C	30	40	A
	-Continuous $T_A = 25$ °C	12 ^{1a}	22 ^{1b}	
	-Pulsed	40	60	
P_D	Power Dissipation for Single Operation $T_A = 25$ °C	2.2 ^{1a}	2.5 ^{1b}	W
	$T_A = 25$ °C	1.0 ^{1c}	1.0 ^{1d}	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 ^{1a}	50 ^{1b}	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 ^{1c}	120 ^{1d}	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7600AS	FDMS7600AS	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 1\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		15 18		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	Q1 Q2			1 500	μA μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}, I_D = 1\text{ mA}$	Q1 Q2	1 1	1.8 1.5	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ $I_D = 1\text{ mA}$, referenced to $25\text{ }^\circ\text{C}$	Q1 Q2		-6 -5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 12\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q1		6.0 8.5 8.3	7.5 12 12	m Ω
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	Q2		2.2 2.6 2.6	2.8 3.3 3.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 12\text{ A}$ $V_{DS} = 5\text{ V}, I_D = 20\text{ A}$	Q1 Q2		63 190		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1: $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		1315 5265	1750 7005	pF
C_{oss}	Output Capacitance	Q2: $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		445 2150	600 2860	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1 Q2		45 200	70 300	pF
R_g	Gate Resistance		Q1 Q2		0.9 0.3		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		8.6 18	18 32	ns
t_r	Rise Time	$V_{DD} = 15\text{ V}, I_D = 12\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		2.5 7.6	10 16	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2: $V_{DD} = 15\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		20 45	32 72	ns
t_f	Fall Time	$V_{DD} = 15\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$	Q1 Q2		2.3 5.2	10 10	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	Q1 Q2		20 81	28 113	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	Q1 Q2		9.3 37	13 52	nC
Q_{gs}	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}$	Q1 Q2		4.3 13		nC
Q_{gd}	Gate to Drain "Miller" Charge	Q2 $V_{DD} = 15\text{ V},$ $I_D = 20\text{ A}$	Q1 Q2		2.2 9.6		nC

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics							
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12\text{ A}$ (Note 2)	Q1		0.8	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 20\text{ A}$ (Note 2)	Q2		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 12\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Q1		27	43	ns
			Q2		47	75	
Q_{rr}	Reverse Recovery Charge	$I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		10	18	nC
			Q2		80	128	

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 57 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in² pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3: As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

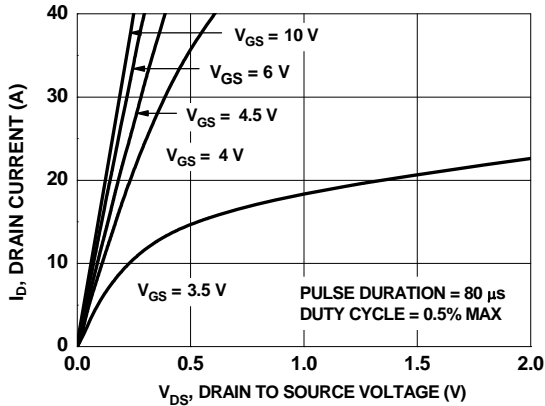


Figure 1. On Region Characteristics

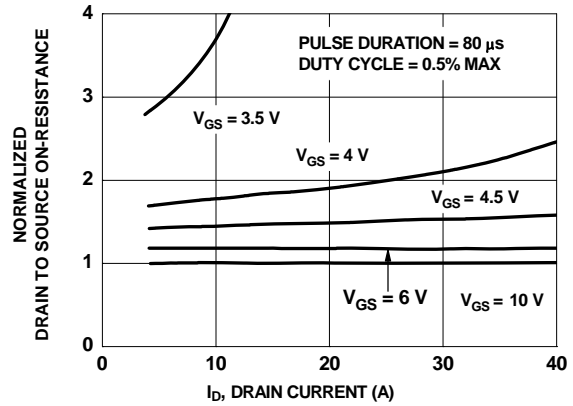


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

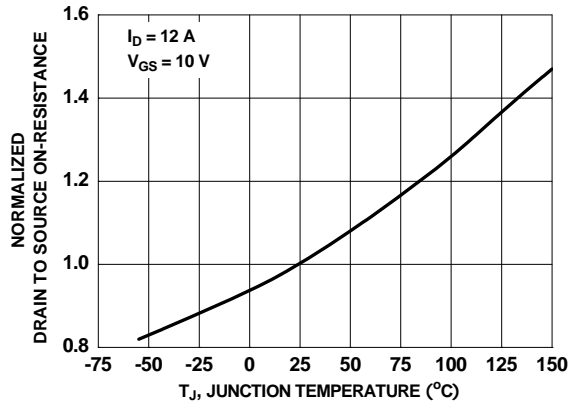


Figure 3. Normalized On Resistance vs Junction Temperature

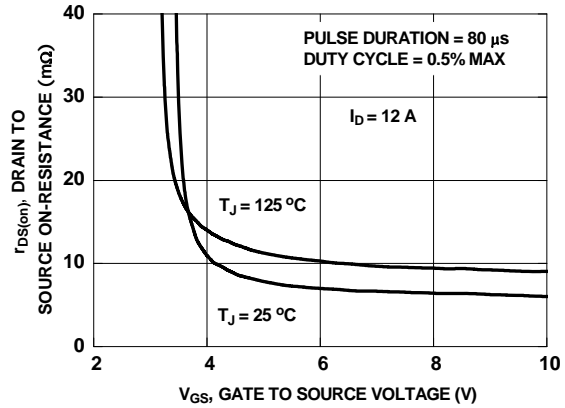


Figure 4. On-Resistance vs Gate to Source Voltage

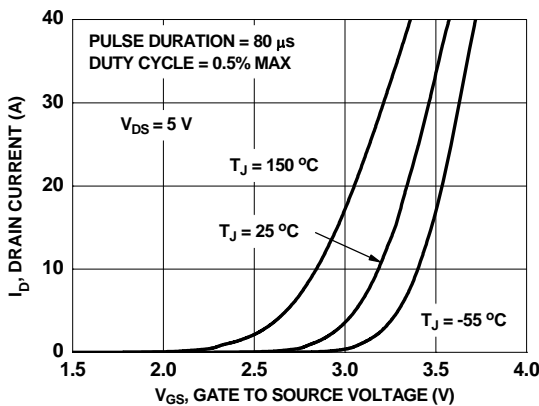


Figure 5. Transfer Characteristics

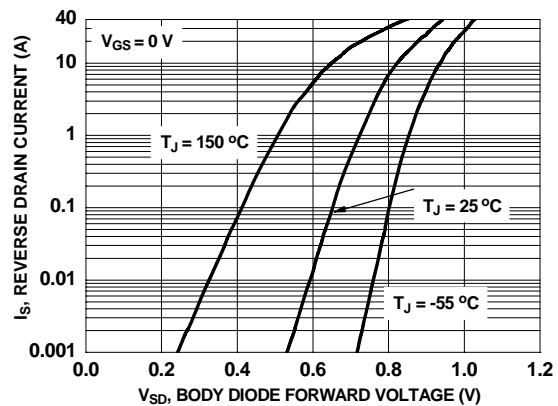


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

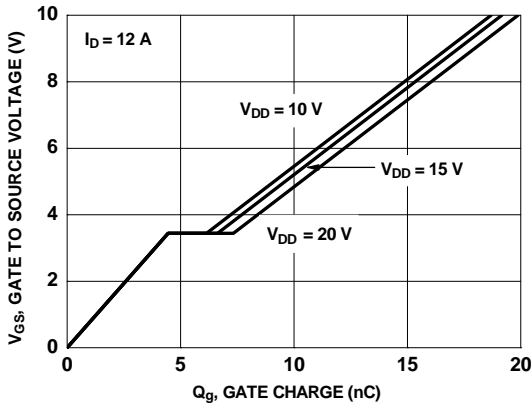


Figure 7. Gate Charge Characteristics

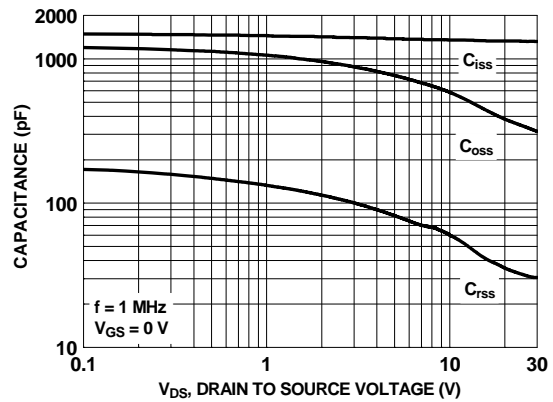


Figure 8. Capacitance vs Drain to Source Voltage

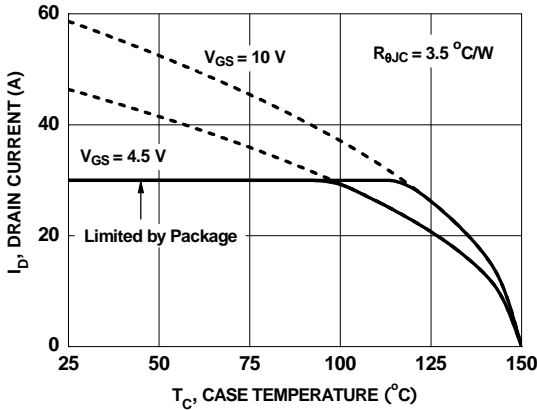


Figure 9. Maximum Continuous Drain Current vs Case Temperature

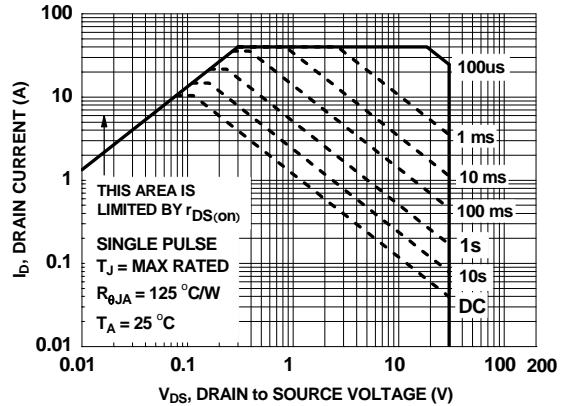


Figure 10. Forward Bias Safe Operating Area

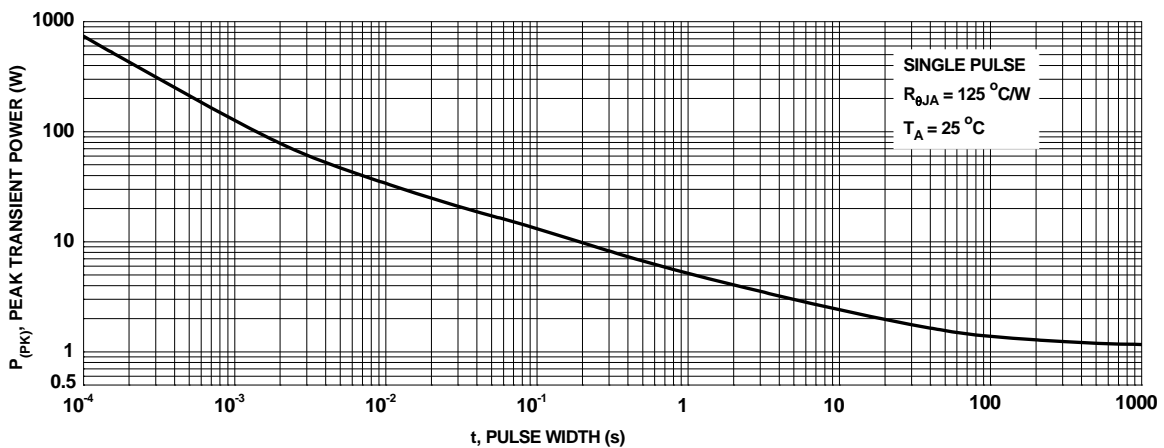


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

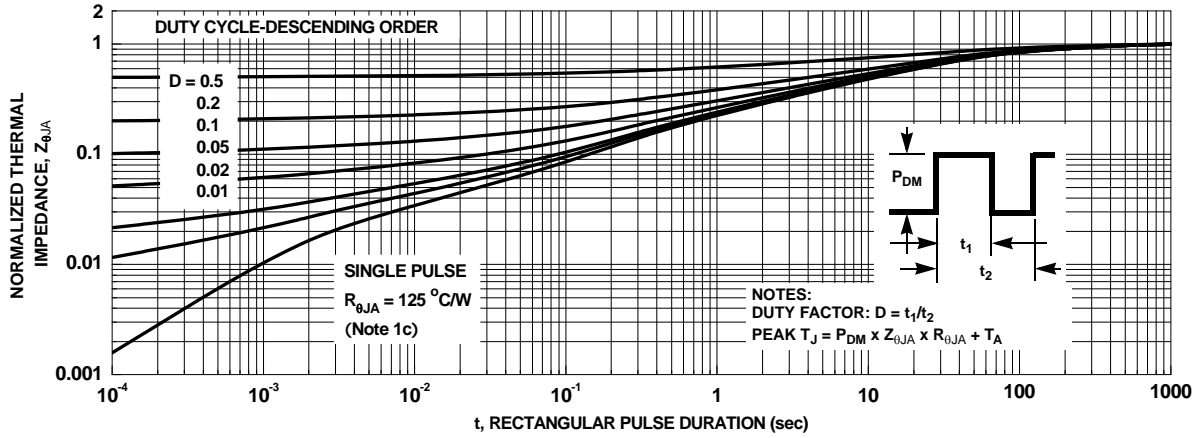


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

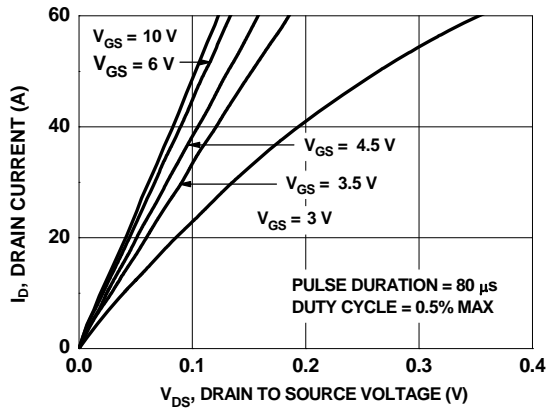


Figure 13. On-Region Characteristics

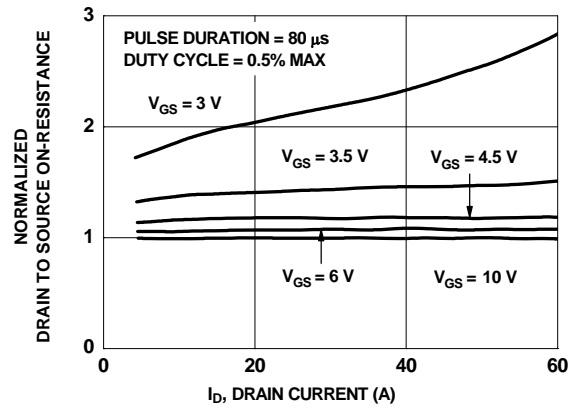


Figure 14. Normalized on-Resistance vs Drain Current and Gate Voltage

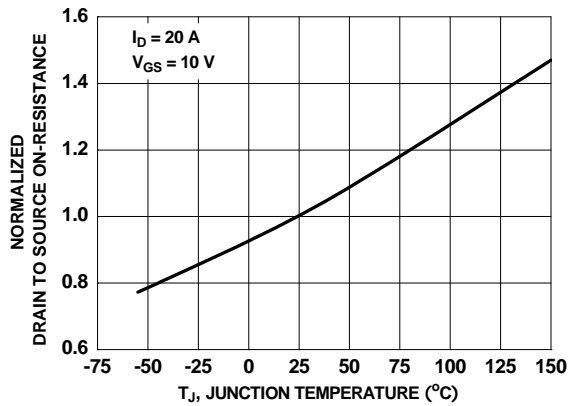


Figure 15. Normalized On-Resistance vs Junction Temperature

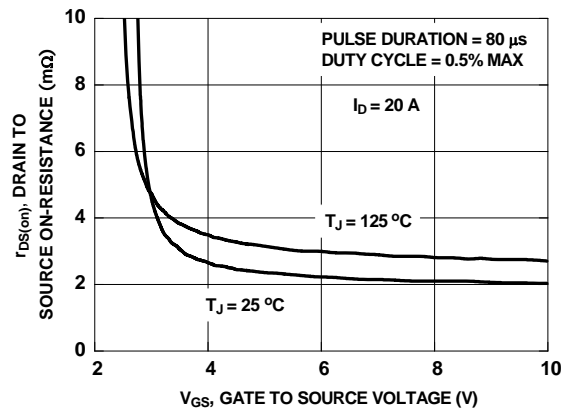


Figure 16. On-Resistance vs Gate to Source Voltage

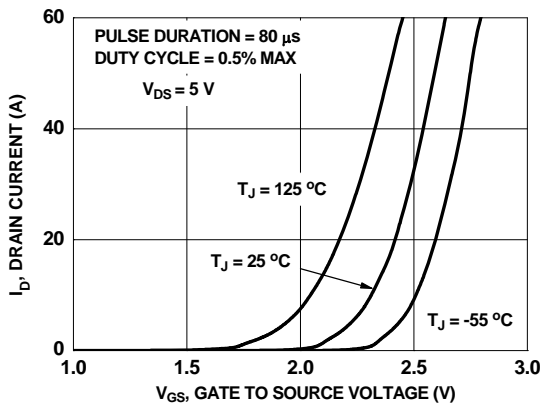


Figure 17. Transfer Characteristics

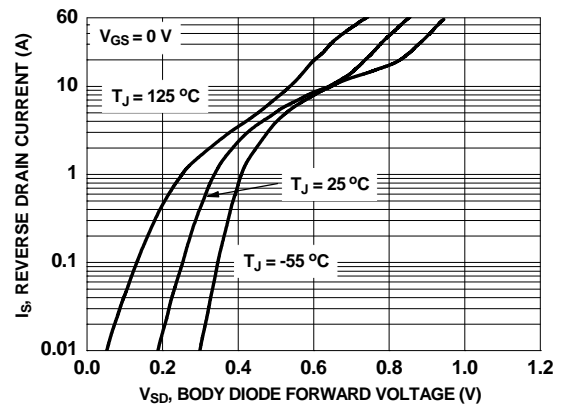


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

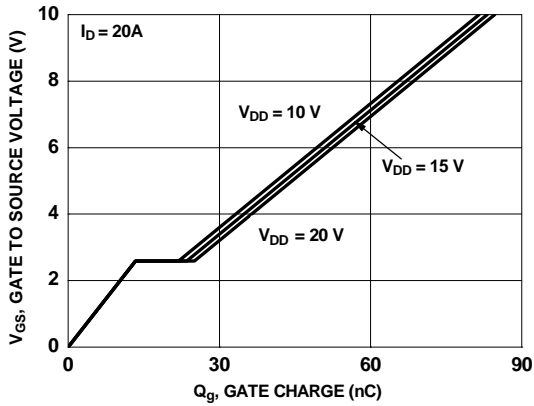


Figure 19. Gate Charge Characteristics

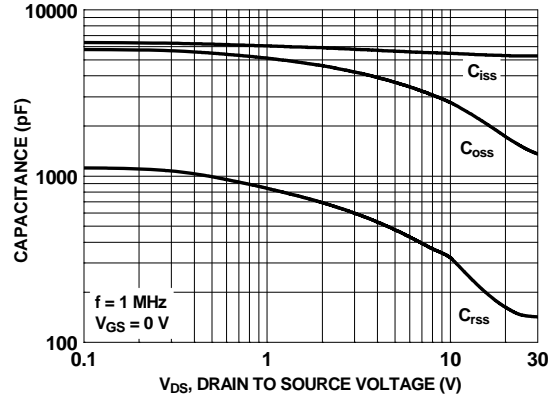


Figure 20. Capacitance vs Drain to Source Voltage

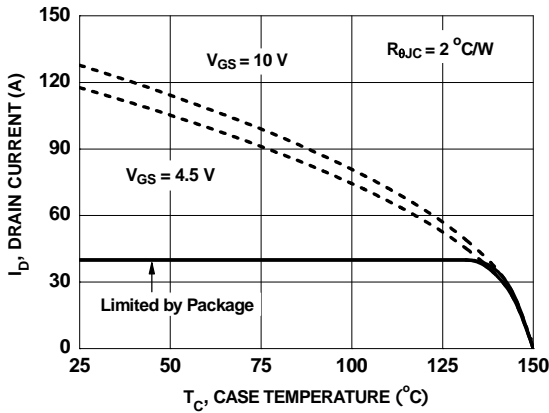


Figure 21. Maximum Continuous Drain Current vs Case Temperature

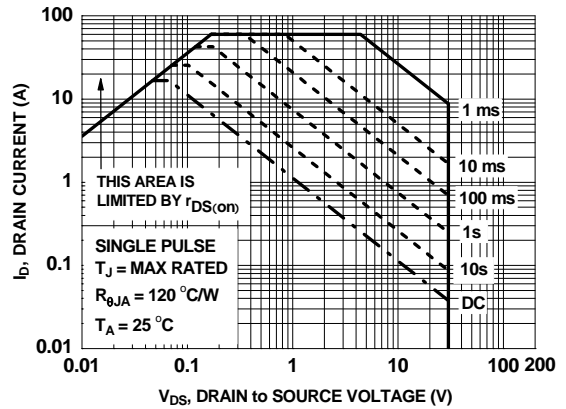


Figure 22. Forward Bias Safe Operating Area

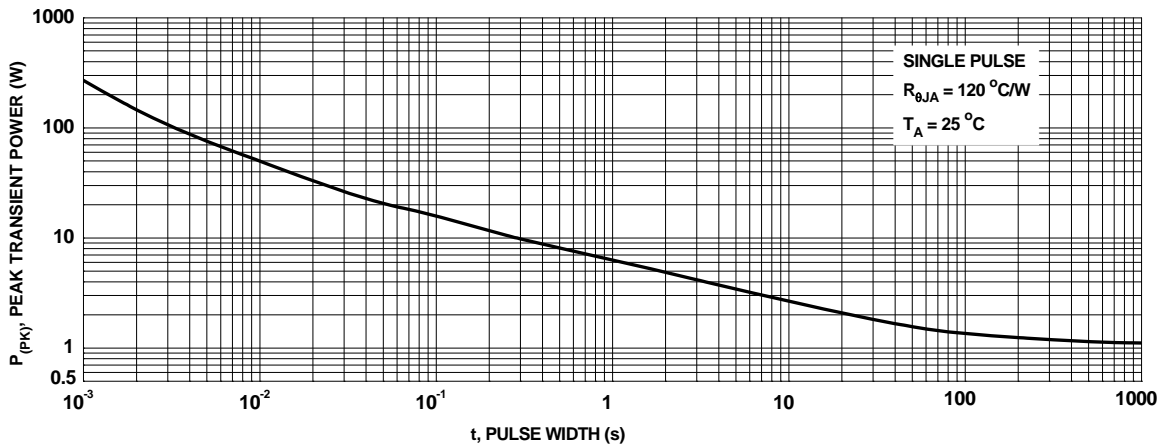


Figure 23. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 N_Channel) $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

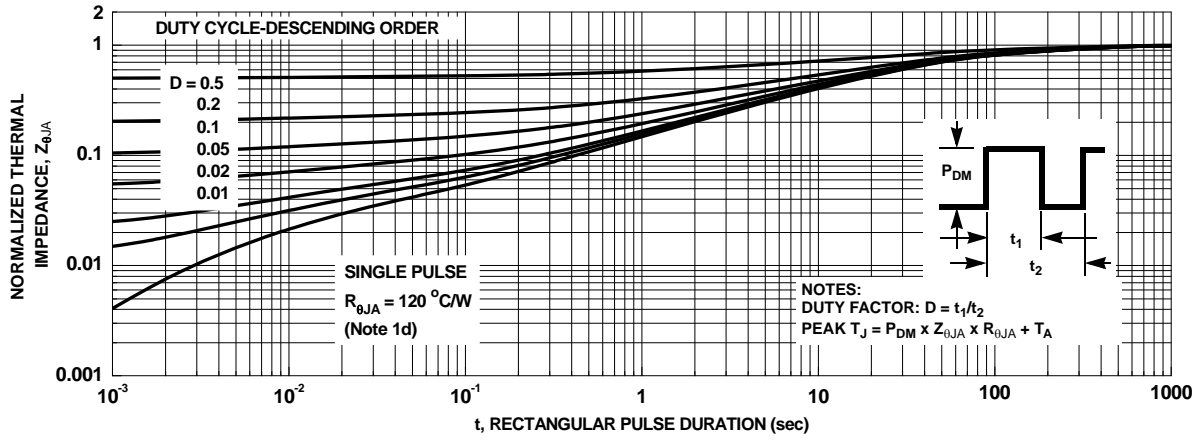


Figure24. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (continued)

SyncFET[™] Schottky body diode Characteristics

Fairchild's SyncFET[™] process embeds a Schottky diode in parallel with PowerTrench[®] MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 25 shows the reverse recovery characteristic of the FDMS7600AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

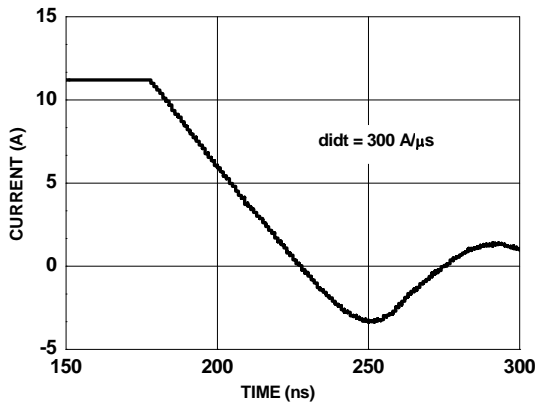


Figure 25. FDMS7600AS SyncFET[™] Body Diode Reverse Recovery Characteristic

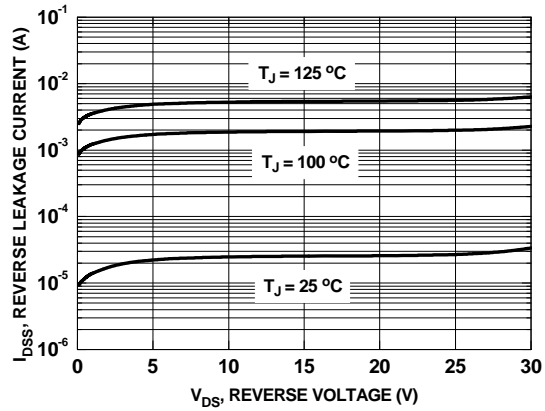
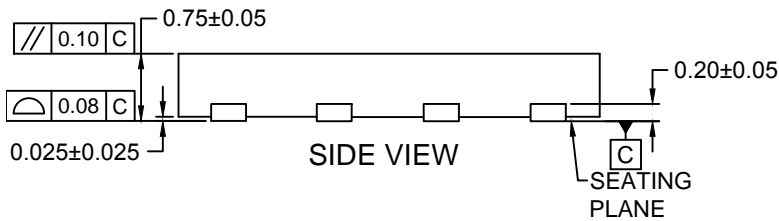
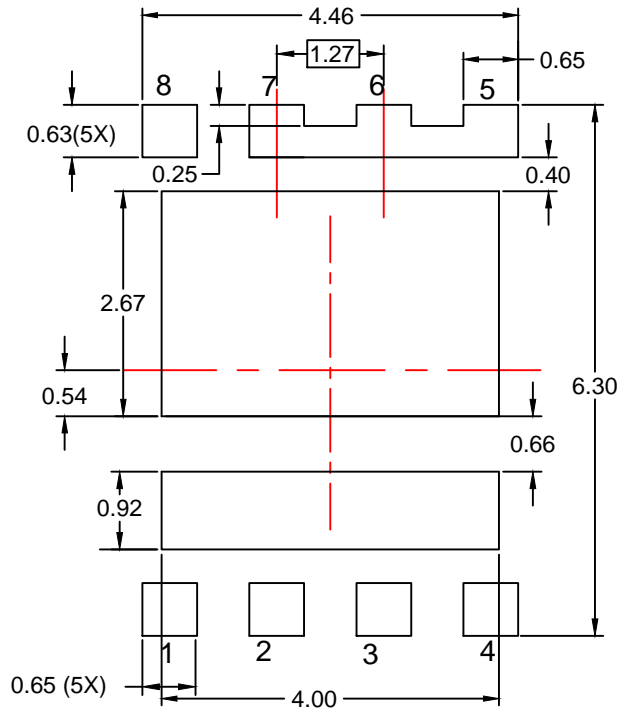
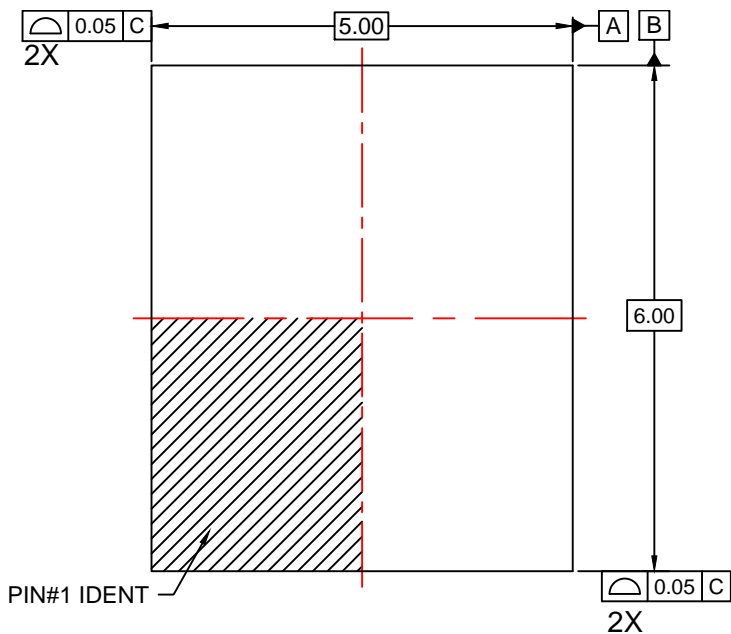
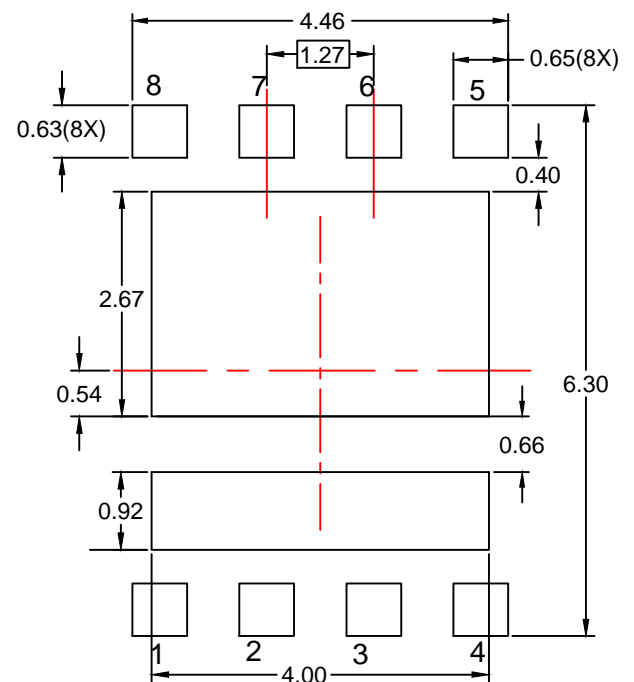
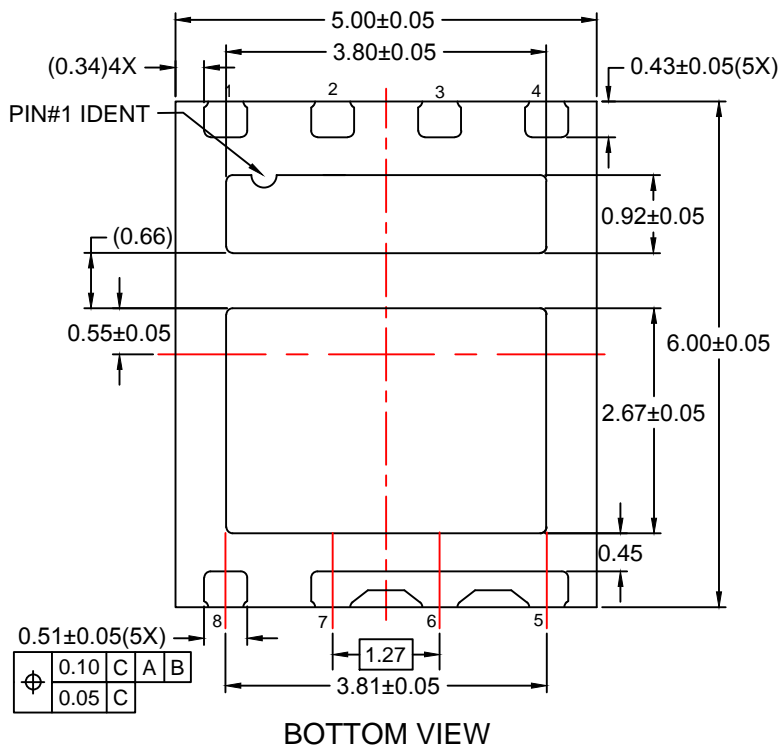


Figure 26. SyncFET[™] Body Diode Reverse Leakage vs. Drain-Source Voltage



RECOMMENDED LAND PATTERN (OPTION 1 - FUSED LEADS 5,6,7)



RECOMMENDED LAND PATTERN (OPTION 2 - ISOLATED LEADS)

NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Prev2.



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative