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June 2007

MM74HCT540, Inverting Octal 3-STATE Buffer
MM74HCT541, Octal 3-STATE Buffer

Features

- TTL input compatible
- Typical propagation delay: 12ns
- 3-STATE outputs for connection to system buses
- Low quiescent current: 80μA
- Output current: 6mA (Min.)

General Description

The MM74HCT540 and MM74HCT541 3-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM74HCT540 is an inverting buffer and the MM74HCT541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are HIGH, all eight outputs are in the high-impedance state.

In order to enhance PC board layout, the MM74HCT540 and MM74HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

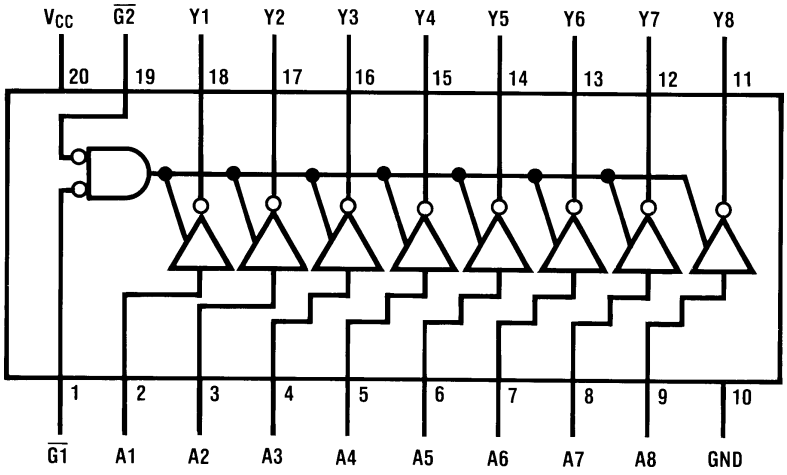
Ordering Information

Order Number	Package Number	Package Description
MM74HCT540WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT540SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT540MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT541WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HCT541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT541N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

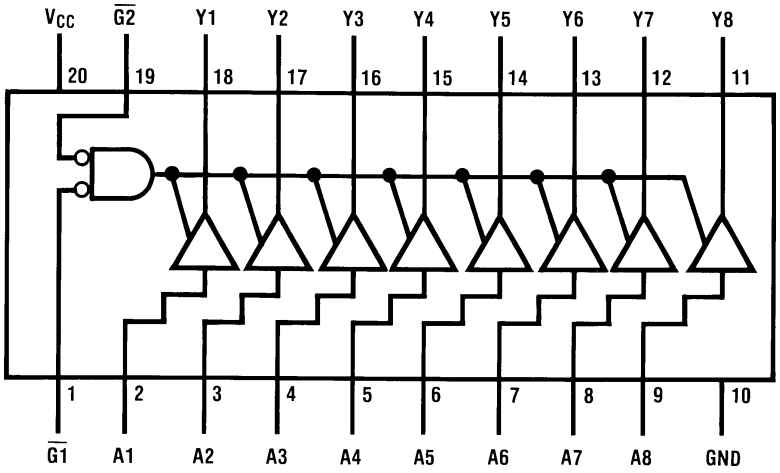
Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagrams

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View, MM74HCT540



Top View, MM74HCT541

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5 to +7.0V
V_{IN}	DC Input Voltage	–1.5 to V_{CC} +1.5V
V_{OUT}	DC Output Voltage	–0.5 to V_{CC} +0.5V
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±35mA
I_{CC}	DC V_{CC} or GND Current, per pin	±70mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
P_D	Power Dissipation	
	Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Note:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: –12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	–40	+85	°C
t_r, t_f	Input Rise and Fall Times		500	ns

DC Electrical Characteristics

V_{CC} = 5V ± 10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = –40 to 85°C	T_A = –55 to 125°C	Units
			Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| = 20\mu A$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$\|I_{OUT}\| = 6.0mA$, $V_{CC} = 4.5V$	4.2	3.98	3.84	3.7	
		$\|I_{OUT}\| = 7.2mA$, $V_{CC} = 5.5V$	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$ or V_{IL}: $\|I_{OUT}\| = 20\mu A$	0	0.1	0.1	0.1	V
		$\|I_{OUT}\| = 6.0mA$, $V_{CC} = 4.5V$	0.2	0.26	0.33	0.4	
		$\|I_{OUT}\| = 7.2mA$, $V_{CC} = 5.5V$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{G} = V_{IH}$		±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu A$		8.0	80	160	µA
		V_{IN} = 2.4V or 0.5V(3)	0.6	1.0	1.3	1.5	mA

Note:

3. Measured per input. All other inputs at V_{CC} or GND.

AC Electrical Characteristics

MM74HCT540: $V_{CC} = 5.0V$, $t_r = t_f = 6ns$, $T_A = 25°C$, (unless otherwise specified).

Symbol	Parameter	Conditions	Typ.	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45pF$	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45pF$, $R_L = 1k\Omega$	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5pF$, $R_L = 1k\Omega$	13	25	ns

AC Electrical Characteristics

MM74HCT540: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6ns$ (unless otherwise specified).

Symbol	Parameter	Conditions		$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$		Units
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50pF$		12	20	25	30	ns
		$C_L = 150pF$		22	30	38	45	
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1k\Omega$	$C_L = 50pF$	15	30	38	45	ns
			$C_L = 150pF$	20	40	50	60	
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1k\Omega$, $C_L = 50pF$		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50pF$		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance(4)	(per output)	$\overline{G} = V_{CC}$	12				pF
			$\overline{G} = GND$	50				

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Electrical Characteristics

MM74HCT541: $V_{CC} = 5.0V$, $t_r = t_f = 6ns$, $T_A = 25°C$, (unless otherwise specified).

Symbol	Parameter	Conditions	Typ.	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45pF$	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45pF$, $R_L = 1k\Omega$	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5pF$, $R_L = 1k\Omega$	15	25	ns

AC Electrical Characteristics

MM74HCT541: $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6ns$ (unless otherwise specified).

Symbol	Parameter	Conditions		$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$		Units
				Typ.	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50pF$		14	23	29	34	ns
		$C_L = 150pF$		17	33	42	49	
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1k\Omega$	$C_L = 50pF$	17	30	38	45	ns
			$C_L = 150pF$	22	40	50	60	
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1k\Omega$, $C_L = 50pF$		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50pF$		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance(5)	(per output)	$\overline{G} = V_{CC}$	12				pF
			$\overline{G} = GND$	45				

Note:

5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

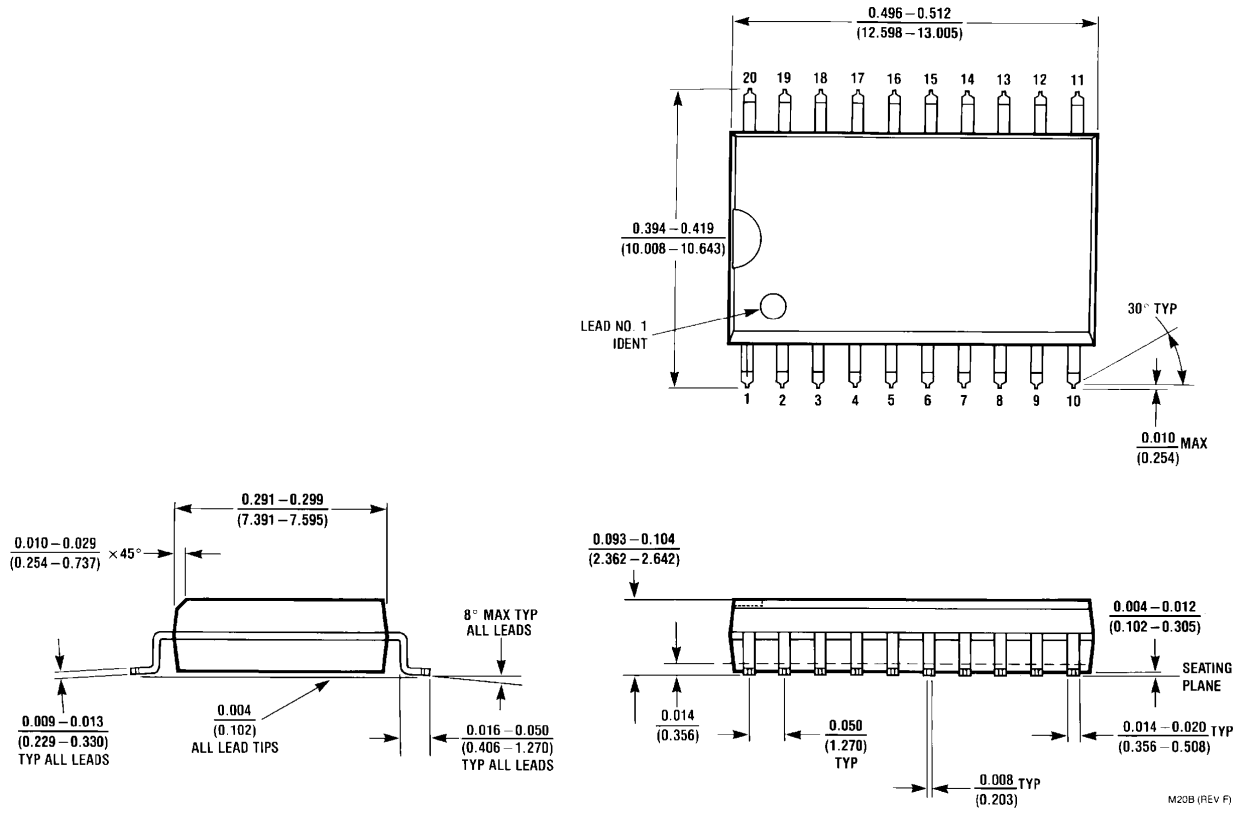
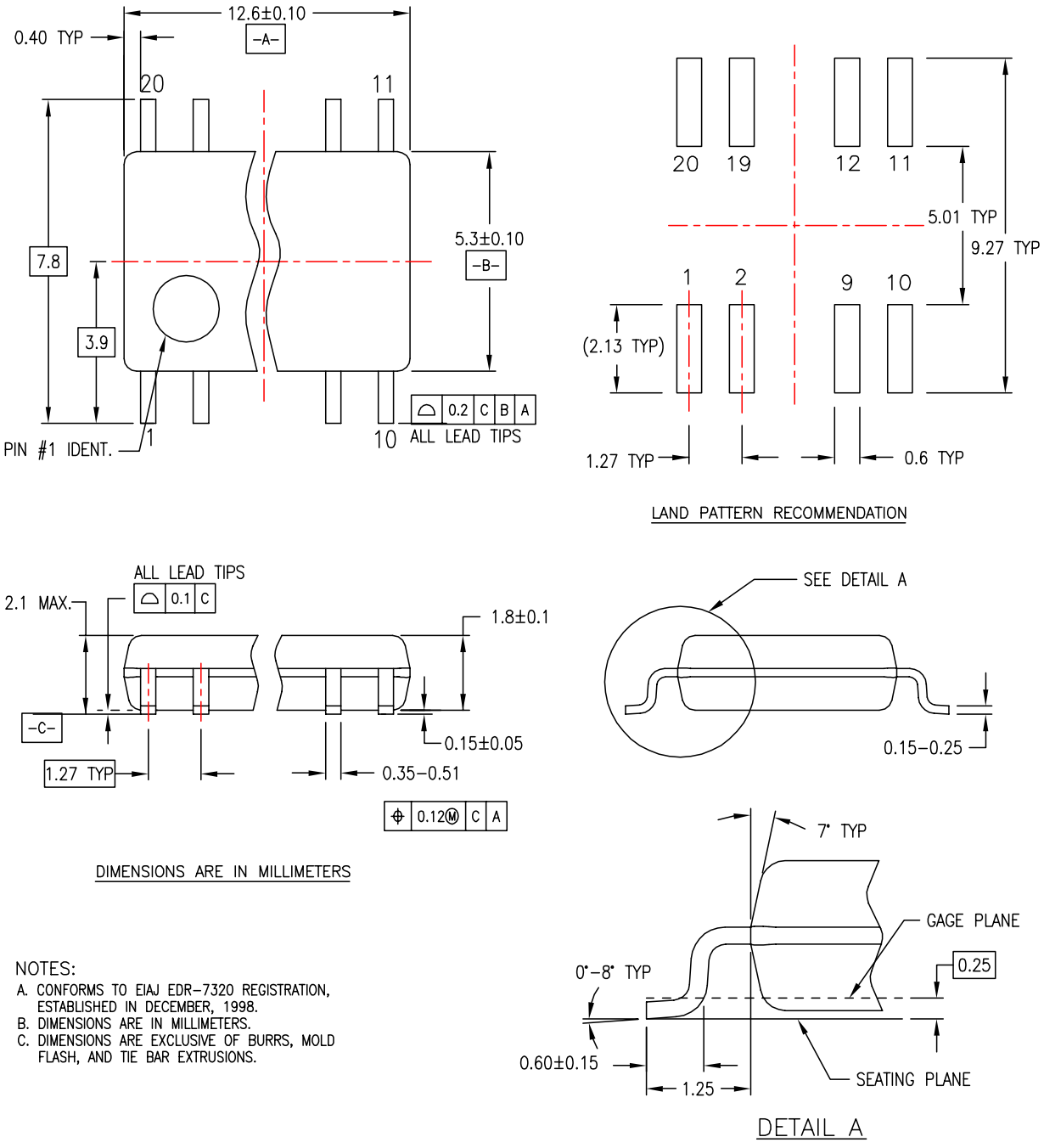


Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

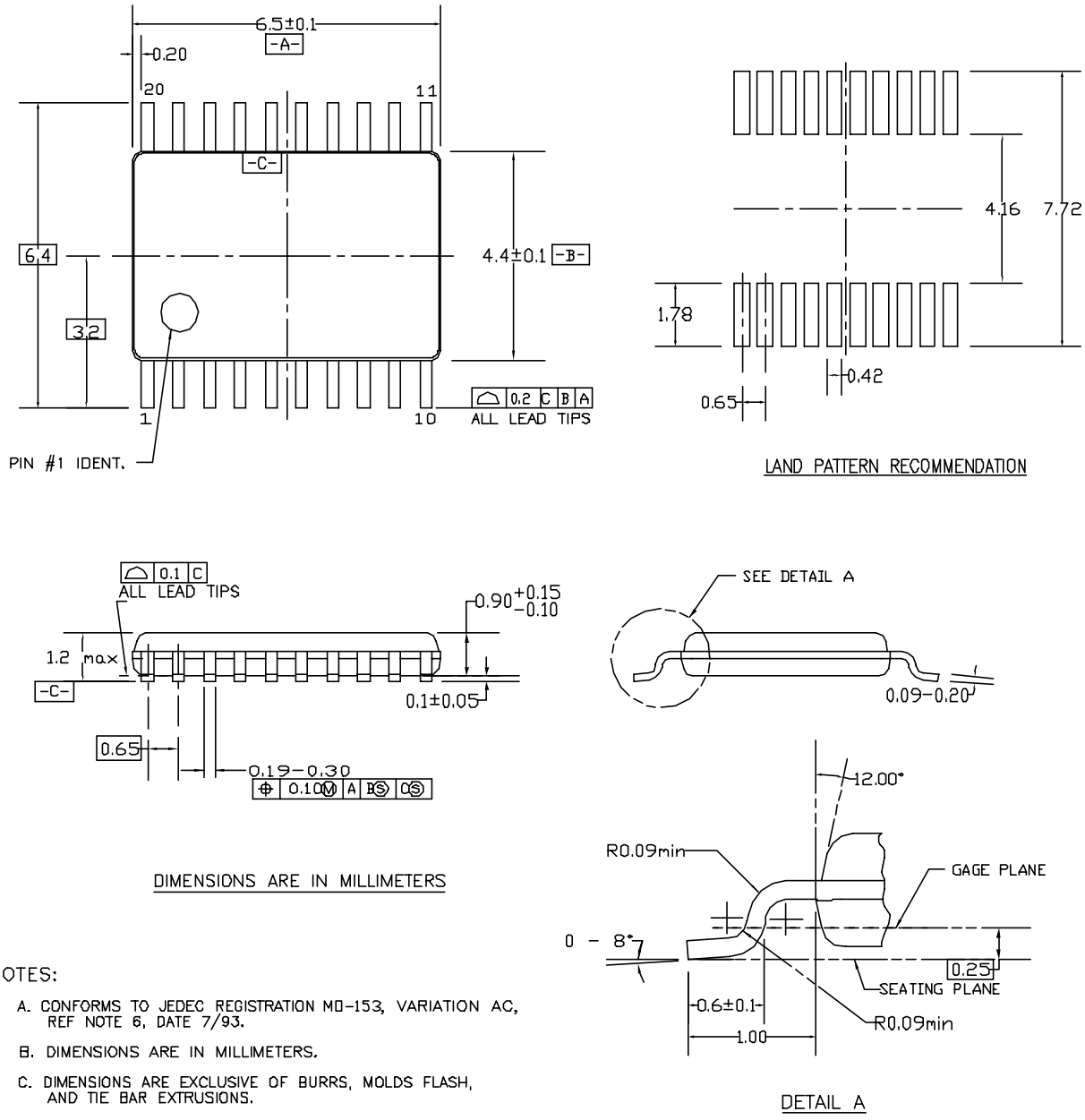
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

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C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

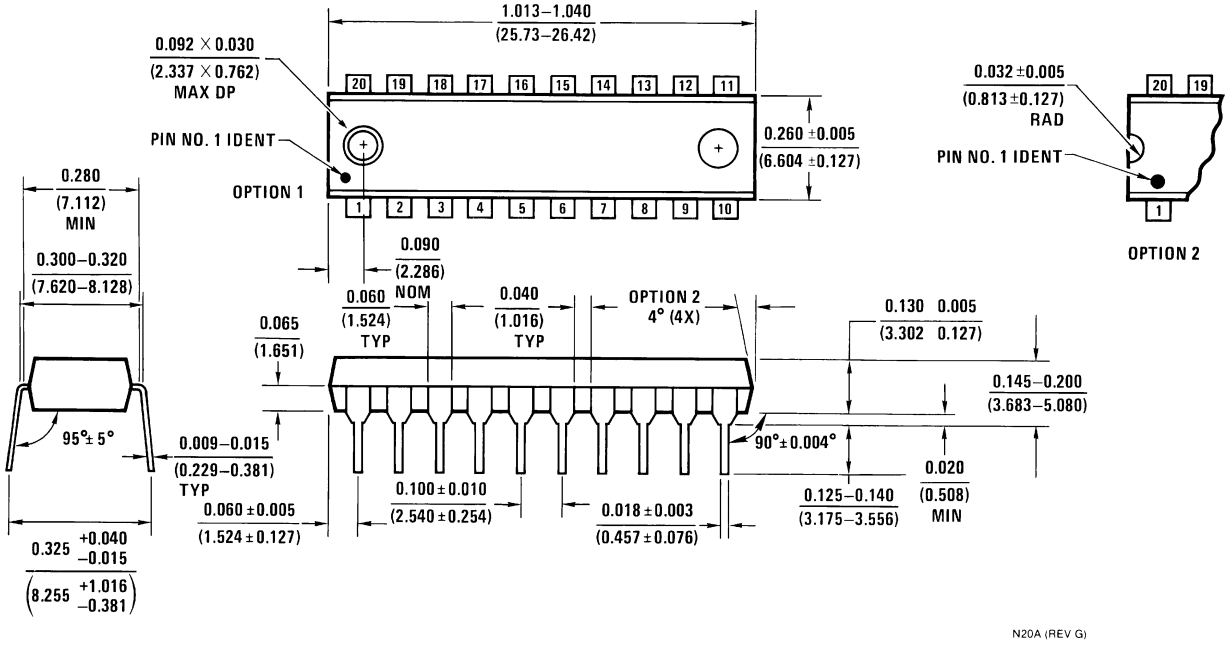

Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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Rev. I28

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