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# NC7WZ02

## TinyLogic® UHS Dual 2-Input NOR Gate

### General Description

The NC7WZ02 is a dual 2-Input NOR Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V<sub>CC</sub> operating range. The device is specified to operate over the 1.65V to 5.5V V<sub>CC</sub> range. The inputs and output are high impedance when V<sub>CC</sub> is 0V. Inputs tolerate voltages up to 7V independent of V<sub>CC</sub> operating voltage.

### Features

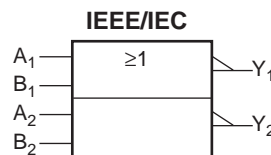
- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Ultra High Speed: t<sub>PD</sub> 2.4ns typ into 50pF at 5V V<sub>CC</sub>
- High Output Drive: ±24mA at 3V V<sub>CC</sub>
- Broad V<sub>CC</sub> Operating Range: 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V<sub>CC</sub>
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Proprietary noise/EMI reduction circuitry implemented

### Ordering Information

Order Number	Package Number	Package Code Top Mark	Package Description	Supplied As
NC7WZ02K8X	MAB08A	WZ02	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WZ02L8X	MAC08A	P5	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

Pb-Free package per JEDEC J-STD-020B.

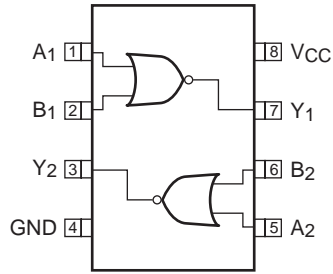
### Logic Symbol



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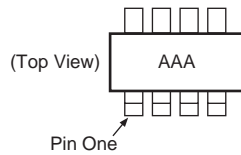
## Connection Diagrams

### Pin Assignment for US8



(Top View)

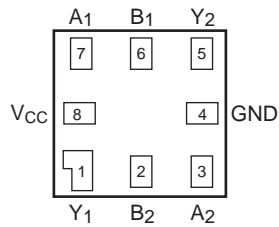
### US8 Pin One Orientation Diagram



AAA represents Product Code Top Mark – see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

### Pad Assignments for MicroPak



(Top Through View)

## Pin Descriptions

Pin Name	Description
$A_n, B_n$	Inputs
$Y_n$	Outputs

## Function Table

$$Y = \overline{A + B}$$

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH Logic Level    L = LOW Logic Level

## Absolute Maximum Ratings

(The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.)

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7V
$V_{IN}$	DC Input Voltage	-0.5V to +7V
$V_{OUT}$	DC Output Voltage	-0.5V to +7V
$I_{IK}$	DC Input Diode Current @ $V_{IN} \leq -0.5V$	-50mA
$I_{OK}$	DC Output Diode Current @ $V_{OUT} \leq -0.5V$	-50mA
$I_{OUT}$	DC Output Current	$\pm 50mA$
$I_{CC}/I_{GND}$	DC $V_{CC}/GND$ Current	$\pm 100mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature under Bias	150°C
$T_L$	Junction Lead Temperature (Soldering, 10 seconds)	260°C
$P_D$	Power Dissipation @ +85°C	250mW

## Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage Operating	1.65V to 5.5V
$V_{CC}$	Supply Voltage Data Retention	1.5V to 5.5V
$V_{IN}$	Input Voltage	0V to 5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC}$ @ 1.8V $\pm$ 0.15V, 2.5V $\pm$ 0.2V $V_{CC}$ @ 3.3V $\pm$ 0.3V $V_{CC}$ @ 5.0V $\pm$ 0.5V	0ns/V to 20ns/V 0ns/V to 10ns/V 0ns/V to 5ns/V
$\theta_{JA}$	Thermal Resistance	250°C/W

### Notes:

1. Unused inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =					Units
				25°C			-40°C to +85°C		
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 to 1.95	0.75 V <sub>CC</sub>			0.75 V <sub>CC</sub>		V
			2.3 to 5.5	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		
V <sub>IL</sub>	LOW Level Input Voltage		1.65 to 1.95			0.25 V <sub>CC</sub>		0.25 V <sub>CC</sub>	V
			2.3 to 5.5			0.3 V <sub>CC</sub>		0.3 V <sub>CC</sub>	
V <sub>OH</sub>	High Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub> , I <sub>OH</sub> = -100μA	1.65	1.55	1.65		1.55		V
			2.3	2.2	2.3		2.2		
			3.0	2.9	3.0		2.9		
			4.5	4.4	4.5		4.4		
		I <sub>OH</sub> = -4mA	1.65	1.29	1.52		1.29		
		I <sub>OH</sub> = -8mA	2.3	1.9	2.15		1.9		
		I <sub>OH</sub> = -16mA	3.0	2.4	2.80		2.4		
		I <sub>OH</sub> = -24mA	3.0	2.3	2.68		2.3		
V <sub>OL</sub>	Low Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> , I <sub>OL</sub> = 100μA	1.65		0.0	0.1		0.1	V
			2.3		0.0	0.1		0.1	
			3.0		0.0	0.1		0.1	
			4.5		0.0	0.1		0.1	
		I <sub>OL</sub> = 4mA	1.65		0.08	0.24		0.24	
		I <sub>OL</sub> = 8mA	2.3		0.10	0.3		0.3	
		I <sub>OL</sub> = 16mA	3.0		0.15	0.4		0.4	
		I <sub>OL</sub> = 24mA	3.0		0.22	0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5V, GND	0 to 5.5			±0.1		±1.0	μA
I <sub>OFF</sub>	Power OFF Leakage Current	V <sub>IN</sub> or V <sub>OUT</sub> = 5.5V	0.0			1		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = 5.5V, GND	1.65 to 5.5			1		10	μA

## AC Electrical Characteristics

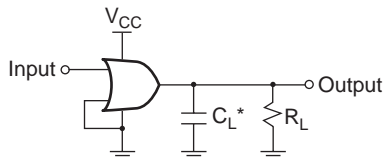
Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =					Units	Figure Number
				+25°C			-40°C to +85°C			
				Min	Typ	Max	Min	Max		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	R <sub>L</sub> = 1MΩ, C <sub>L</sub> = 15pF	1.8 ± 0.15	2.0	5.4	9.8	2.0	10	ns	Figure 1 Figure 3
			2.5 ± 0.2	1.2	3.3	5.4	1.2	5.8		
			3.3 ± 0.3	0.8	2.5	3.8	0.8	4.1		
			5.0 ± 0.5	0.5	2.0	3.0	0.5	3.3		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay	R <sub>L</sub> = 500Ω, C <sub>L</sub> = 50pF	3.3 ± 0.3	1.2	3.1	4.6	1.2	5.0	ns	Figure 1 Figure 3
			5.0 ± 0.5	0.8	2.4	3.7	0.8	4.0		
C <sub>IN</sub>	Input Capacitance		0		2.5				pF	
C <sub>PD</sub>	Power Dissipation Capacitance	Note 2	3.3		13.5				pF	Figure 2
			5.0		17.5					

### Notes:

2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2.) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:

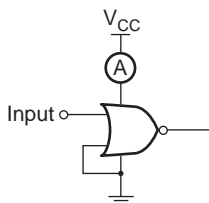
$$C_{PD} = I_{CCD} / (V_{CC}) (F).$$

## AC Loading and Waveforms



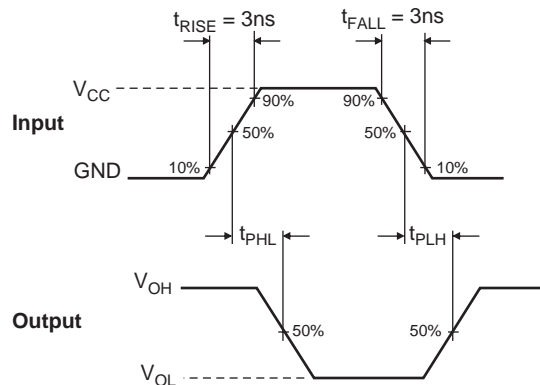
\*C<sub>L</sub> includes load and stray capacitance.  
Input PRR = 1.0MHz; t<sub>W</sub> = 500ns

**Figure 1. AC Test Circuit**



Input = AC Waveform; t<sub>r</sub>, t<sub>f</sub> = 1.8ns;  
PRR = 10MHz; Duty Cycle = 50%

**Figure 2. I<sub>CCD</sub> Test Circuit**



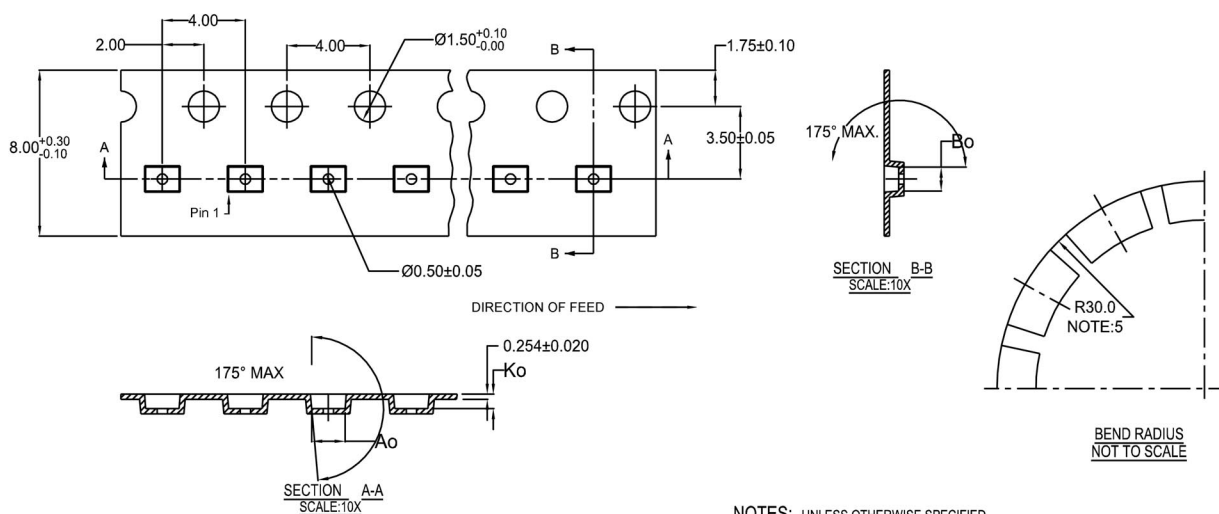
**Figure 3. AC Waveforms**

## Tape and Reel Specification

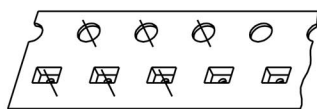
### Tape Format for MircoPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### Tape Dimension inches (millimeters)



10	300056	2.30±0.05	1.78±0.05	0.68±0.05
8	300038	1.78±0.05	1.78±0.05	0.68±0.05
6	300033	1.60±0.05	1.15±0.05	0.70±0.05

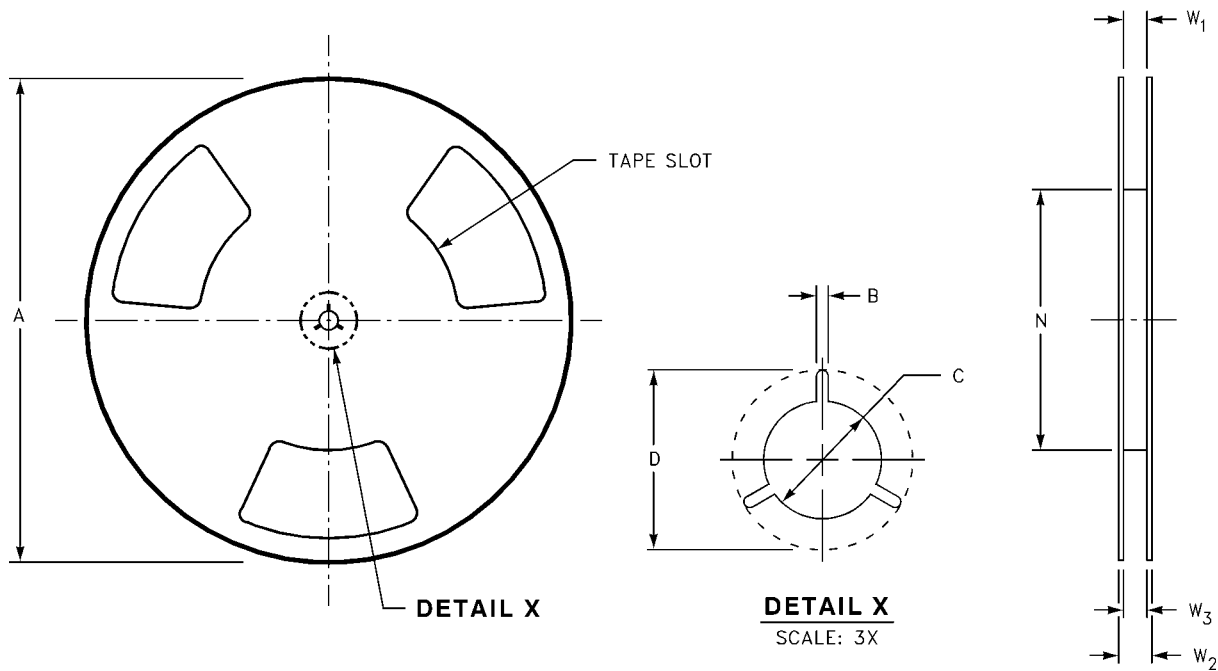


SCALE: 6X

#### NOTES: UNLESS OTHERWISE SPECIFIED

- ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ±0.30MM
- NO INDICATED CORNER RADIUS IS 0.127MM
- CAMBER NOT TO EXCEED 1MM IN 100MM
- SMALLEST ALLOWABLE BENDING RADIUS
- POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

**Reel Dimension for MircoPak inches (millimeters)**



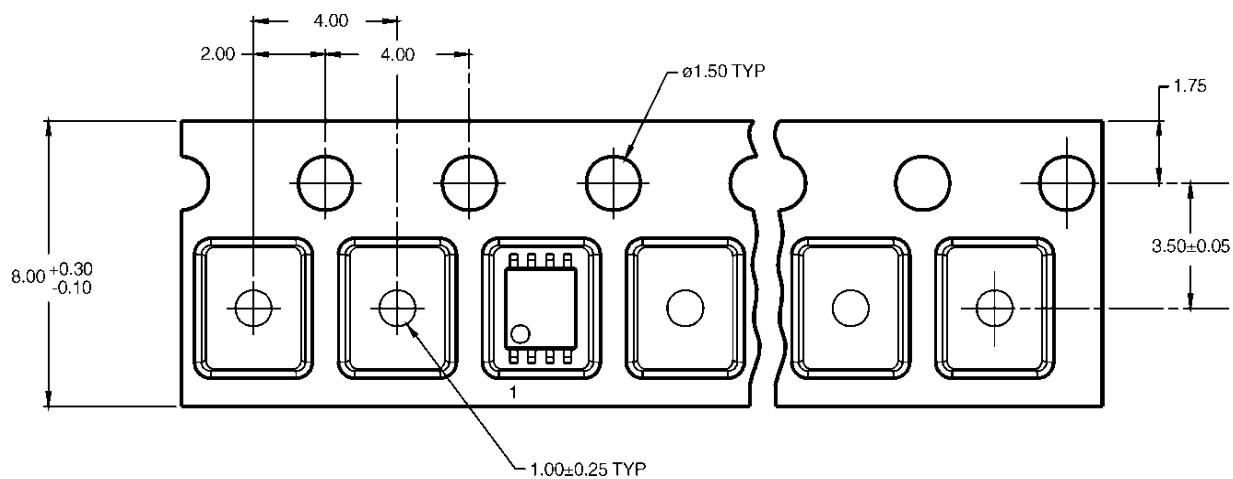
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

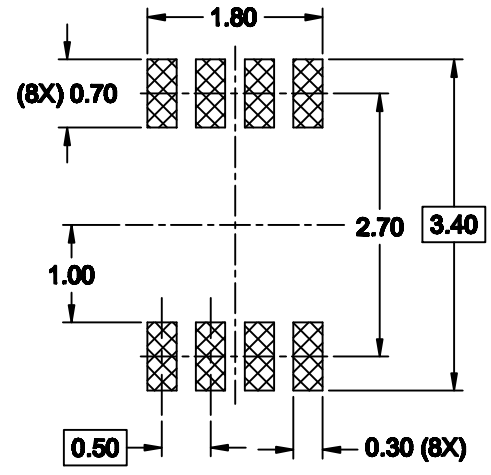
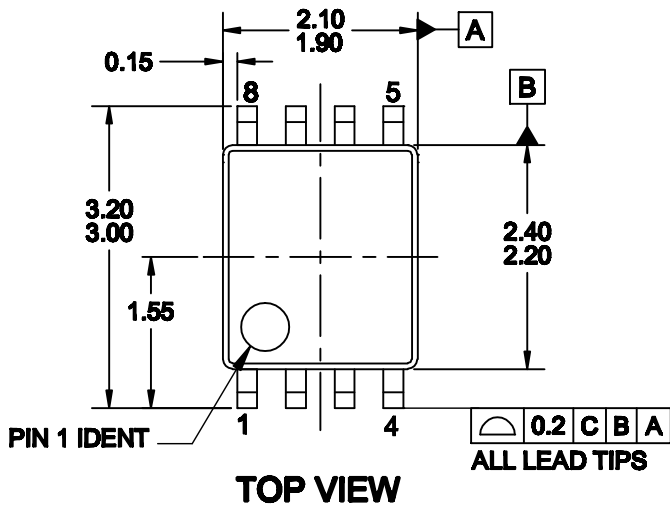


**Tape Format for US8**

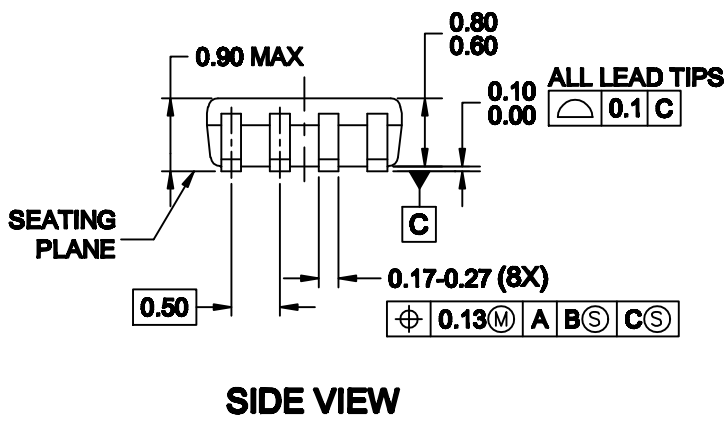
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

**Tape Dimension** inches (millimeters)



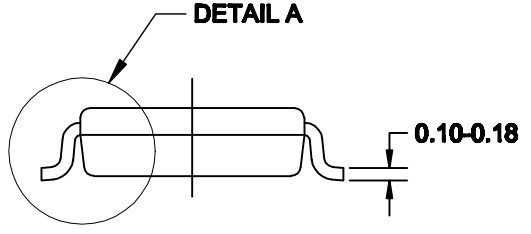
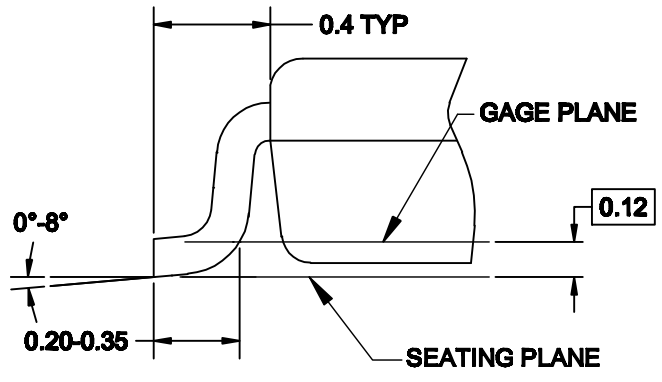


**RECOMMENDED LAND PATTERN**

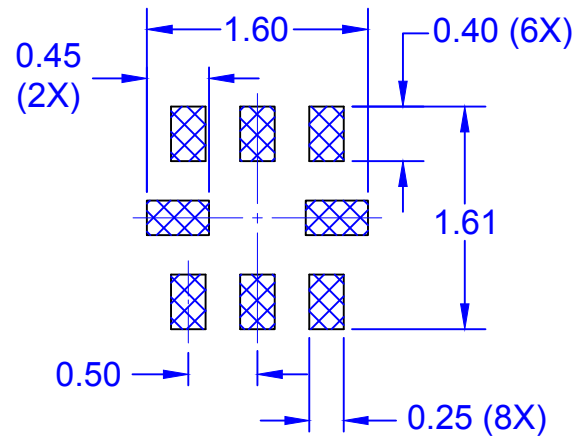
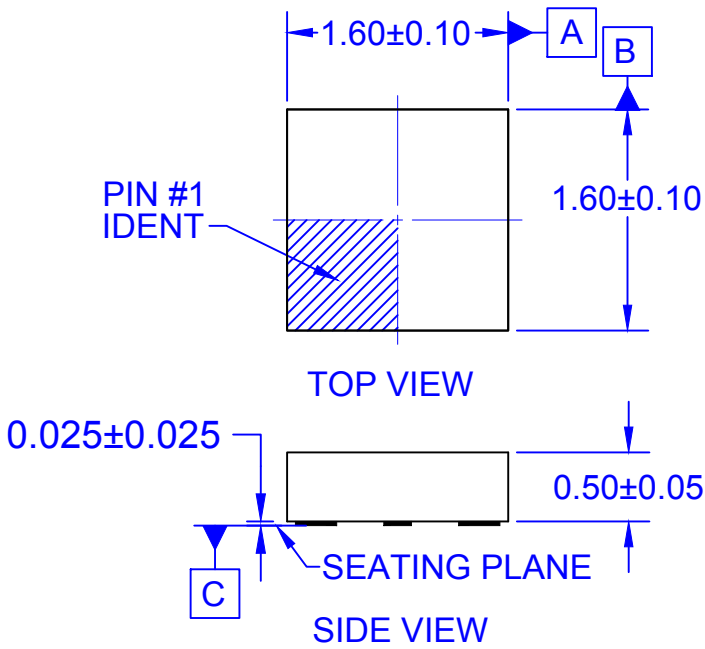


**NOTES:**

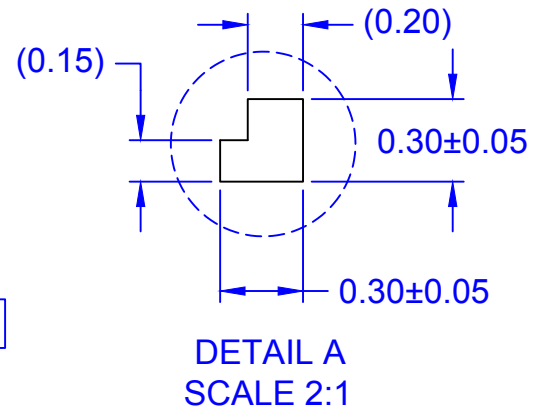
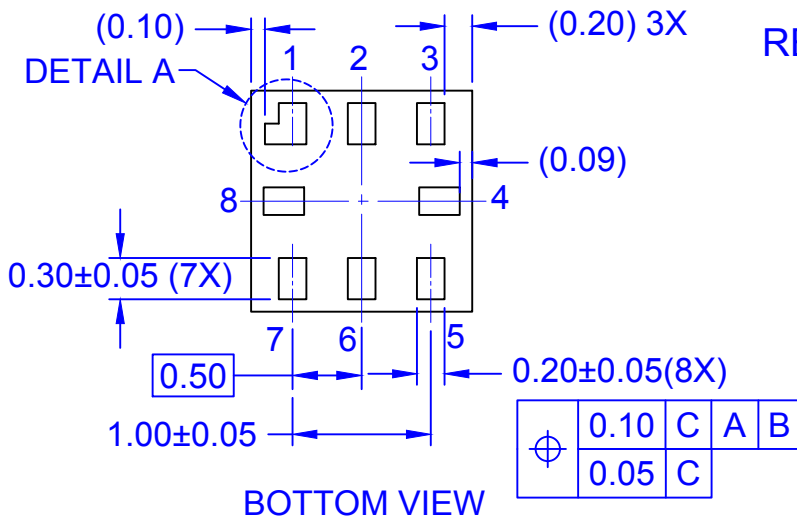
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**DETAIL A**



### RECOMMENDED LAND PATTERN



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