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FDMA291P Single P-Channel 1.8V Specified PowerTrench[®] MOSFET

FDMA291P

Single P-Channel 1.8V Specified PowerTrench[®] MOSFET

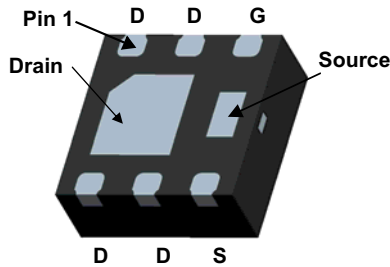
General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultra-portable applications. It features a MOSFET with low on-state resistance.

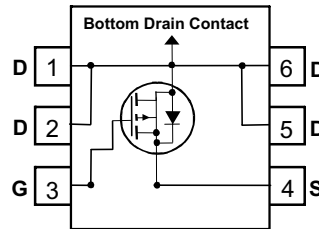
The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- -6.6 A, -20V. $r_{DS(ON)} = 42\text{ m}\Omega @ V_{GS} = -4.5\text{V}$
 $r_{DS(ON)} = 58\text{ m}\Omega @ V_{GS} = -2.5\text{V}$
 $r_{DS(ON)} = 98\text{ m}\Omega @ V_{GS} = -1.8\text{V}$
- Low profile – 0.8 mm maximum – in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant



MicroFET 2x2



Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | Ratings | Units |
|-----------------------------------|--|-------------|-------|
| V _{DS} | Drain-Source Voltage | -20 | V |
| V _{GS} | Gate-Source Voltage | ±8 | V |
| I _D | Drain Current – Continuous (Note 1a) | -6.6 | A |
| | – Pulsed | -24 | |
| P _D | Power Dissipation for Single Operation (Note 1a) | 2.4 | W |
| | (Note 1b) | 0.9 | |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|------------------|---|-----|------|
| R _{θJC} | Thermal Resistance, Junction-to-Case | 13 | °C/W |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient (Note 1a) | 52 | |
| R _{θJA} | Thermal Resistance, Junction-to-Ambient (Note 1b) | 145 | |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|----------|-----------|------------|------------|
| 291 | FDMA291P | 7" | 8mm | 3000 units |

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
|--------|-----------|-----------------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|--|-----|-----|-----------|---------------|
| BV_{DSS} | Drain–Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$ | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | -12 | | mV/°C |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$ | | | -1 | μA |
| I_{GSS} | Gate–Body Leakage | $V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 100 | nA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|---|------|----------------------|----------------------|------------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$ | -0.4 | -0.7 | -1.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250\ \mu\text{A}$, Referenced to 25°C | | 3 | | mV/°C |
| $r_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS} = -4.5\text{ V}, I_D = -6.6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -5.1\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -3.9\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -6.6\text{ A}, T_J = 125^\circ\text{C}$ | | 36 51 79 49 | 42 58 98 64 | m Ω |
| g_{FS} | Forward Transconductance | $V_{DS} = -5\text{ V}, I_D = -6.6\text{ A}$ | | 16 | | S |

Dynamic Characteristics

| | | | | | | |
|------------|------------------------------|--|--|------|--|----|
| C_{iss} | Input Capacitance | $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}$ | | 1000 | | pF |
| C_{oss} | Output Capacitance | $f = 1.0\text{ MHz}$ | | 190 | | pF |
| C_{riss} | Reverse Transfer Capacitance | | | 100 | | pF |

Switching Characteristics (Note 2)

| | | | | | | |
|--------------|---------------------|---|--|----|----|----|
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD} = -10\text{ V}, I_D = -1\text{ A}$ | | 13 | 23 | ns |
| t_r | Turn–On Rise Time | $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$ | | 9 | 18 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 42 | 68 | ns |
| t_f | Turn–Off Fall Time | | | 25 | 40 | ns |
| Q_g | Total Gate Charge | $V_{DS} = -10\text{ V}, I_D = -6.6\text{ A}$ | | 10 | 14 | nC |
| Q_{gs} | Gate–Source Charge | $V_{GS} = -4.5\text{ V}$ | | 2 | | nC |
| Q_{gd} | Gate–Drain Charge | | | 3 | | nC |

Drain–Source Diode Characteristics and Maximum Ratings

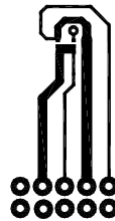
| | | | | | | |
|----------|---|---|--|------|------|----|
| I_S | Maximum Continuous Drain–Source Diode Forward Current | | | | -2 | A |
| V_{SD} | Drain–Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = -2\text{ A}$ (Note 2) | | -0.8 | -1.2 | V |
| t_{rr} | Diode Reverse Recovery Time | $I_F = -6.6\text{ A}$ | | 20 | | ns |
| Q_{rr} | Diode Reverse Recovery Charge | $dI_F/dt = 100\text{ A}/\mu\text{s}$ | | 8 | | nC |

Notes:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52°C/W when mounted on a 1 in² pad of 2 oz copper.



b. 145°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

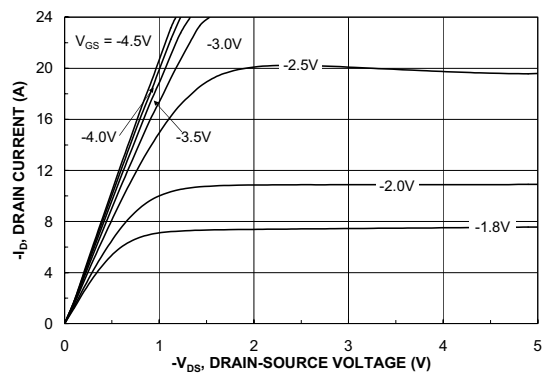


Figure 1. On-Region Characteristics.

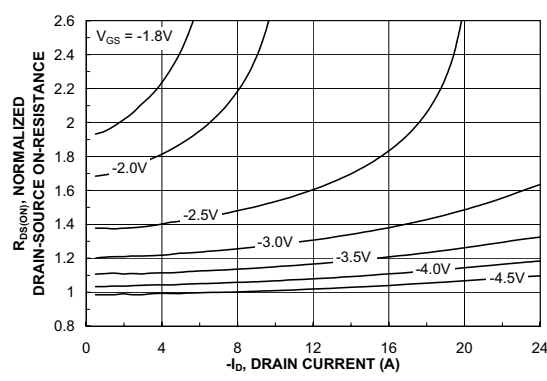


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

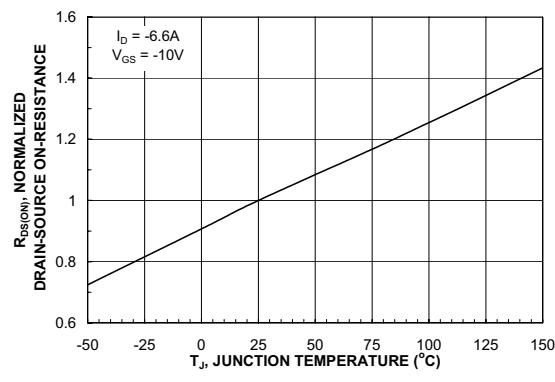


Figure 3. On-Resistance Variation with Temperature.

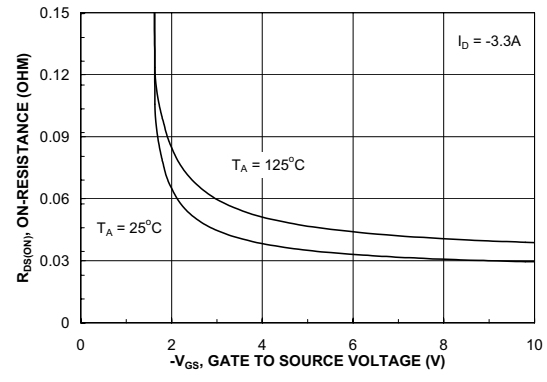


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

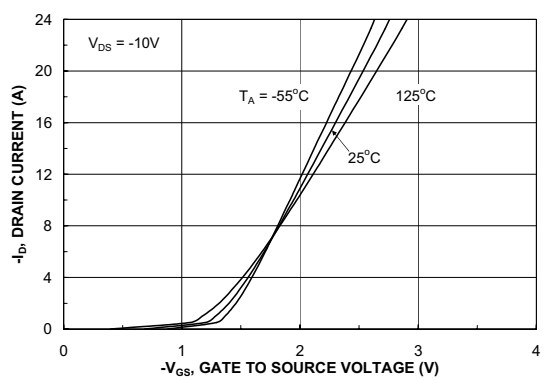


Figure 5. Transfer Characteristics.

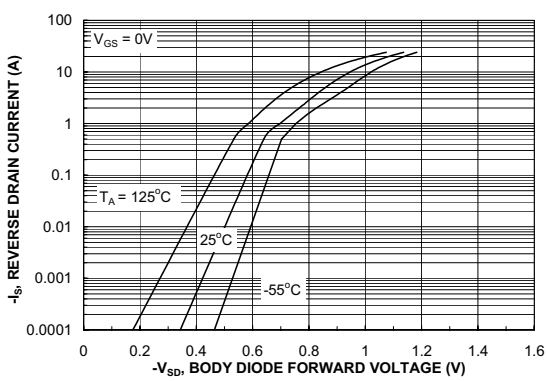


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

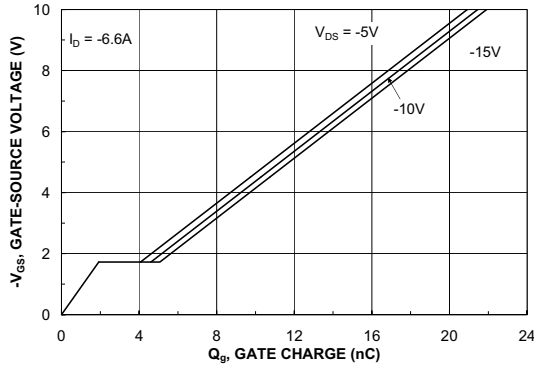


Figure 7. Gate Charge Characteristics.

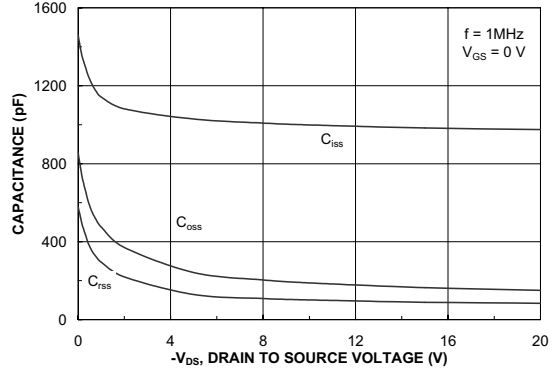


Figure 8. Capacitance Characteristics.

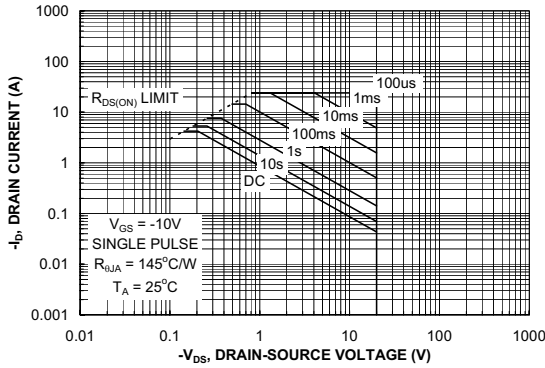


Figure 9. Maximum Safe Operating Area.

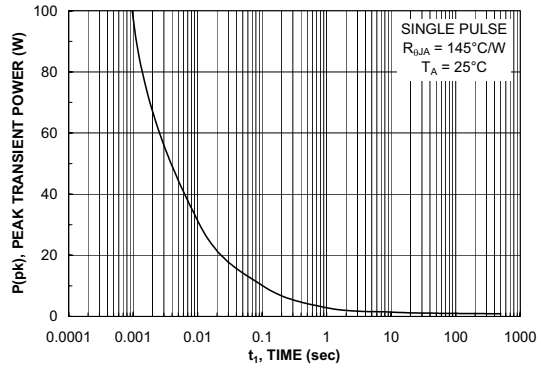


Figure 10. Single Pulse Maximum Power Dissipation.

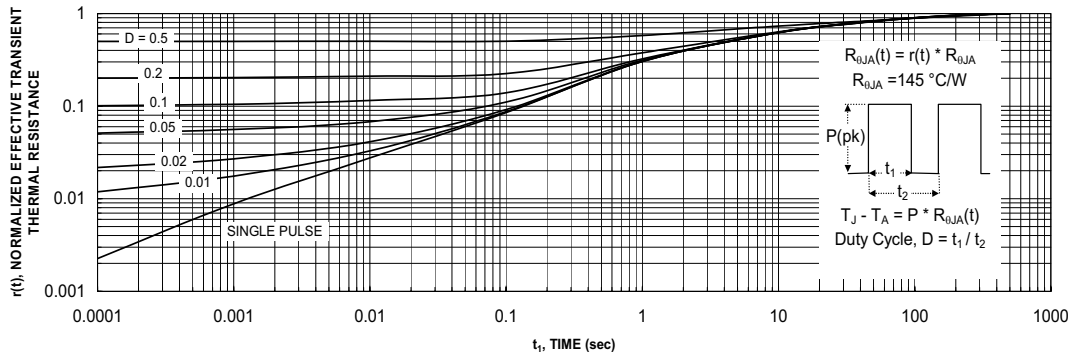
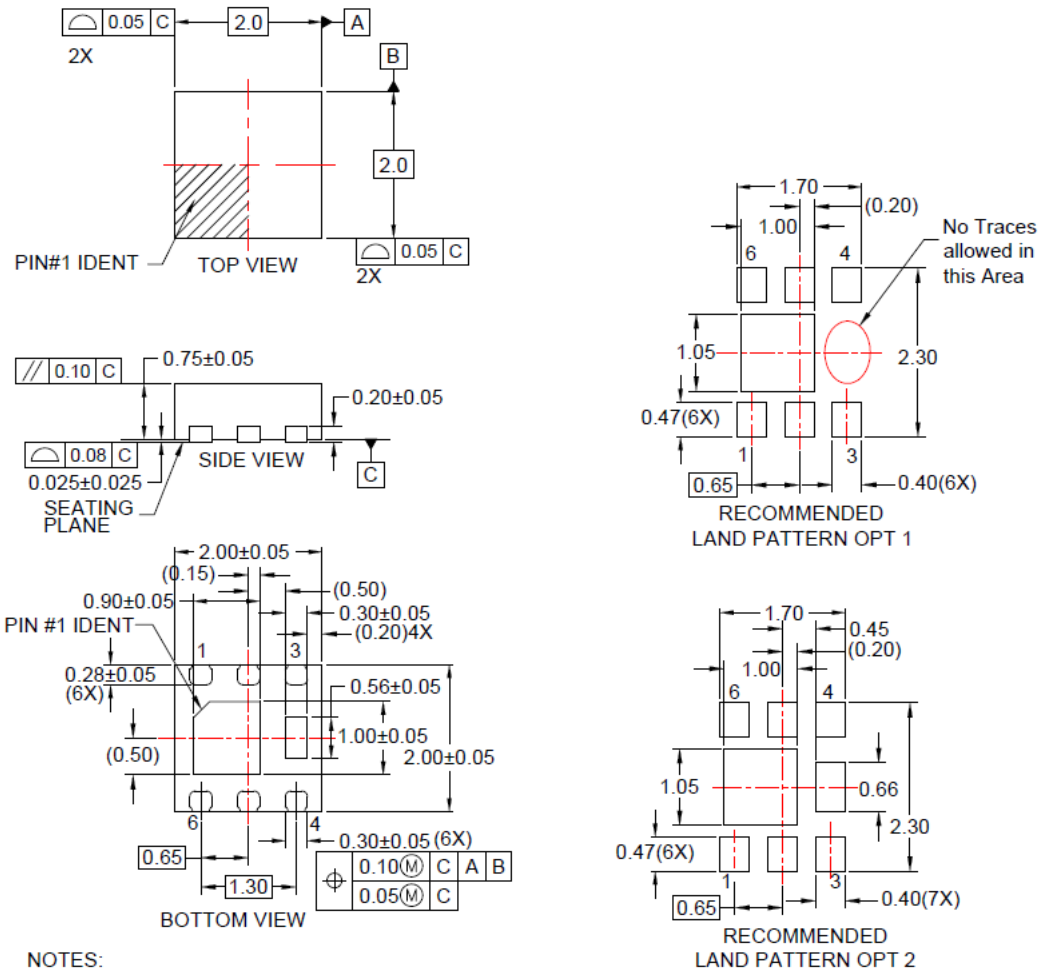


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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