LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97530KVT-M MAX 445 Segment(89segx5COM)

General Description

The BU97530KVT-M is 1/5, 1/4, 1/3 or 1/1 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU97530KVT-M can drive up to 445 LCD Segments directly. The BU97530KVT-M can also control up to 9 general-purpose output ports.
These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wring.

Features

- AEC-Q100 Qualified (Note1)
- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- Either 1/5, 1/4, 1/3 or 1/1 duty (static) can be selected with the serial control data.
  1/5 duty drive: Up to 445 segments can be driven
  1/4 duty drive: Up to 360 segments can be driven
  1/3 duty drive: Up to 270 segments can be driven
  1/1 duty drive: Up to 90 segments can be driven
- Serial data control of frame frequency for common and segment output waveforms.
- Serial data control of switching between the segment output port , PWM output port and general-purpose output port functions.(Max 9 ports)
- Built-in OSC circuit
- Integrated Power-on Reset circuit
- No external component
- Low power consumption design
- Supports Line and Frame Inversion

(Note1) Grade 3

Applications

- Car audio, Home electrical appliance, Meter equipment etc.

Key Specifications

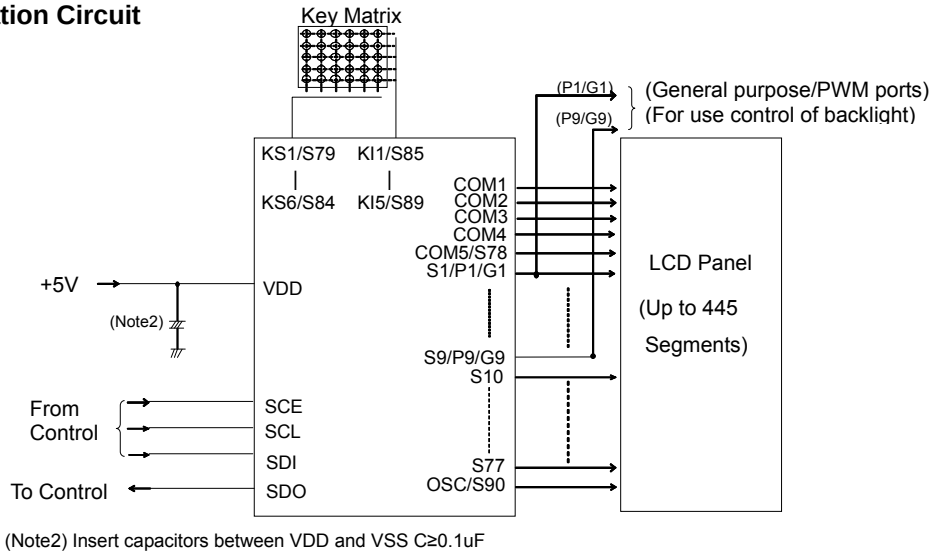
- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 445 Segments
- Display Duty: 1/1,1/3,1/4,1/5 selectable
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

Packages

TQFP100V W(Typ.)×D(Typ.)×H(Max.)

TQFP100V
16.00mm x 16.00mm x 1.20mm

Typical Application Circuit



(Note2) Insert capacitors between VDD and VSS C≥0.1uF

Figure 1. Typical Application Circuit

Block Diagram

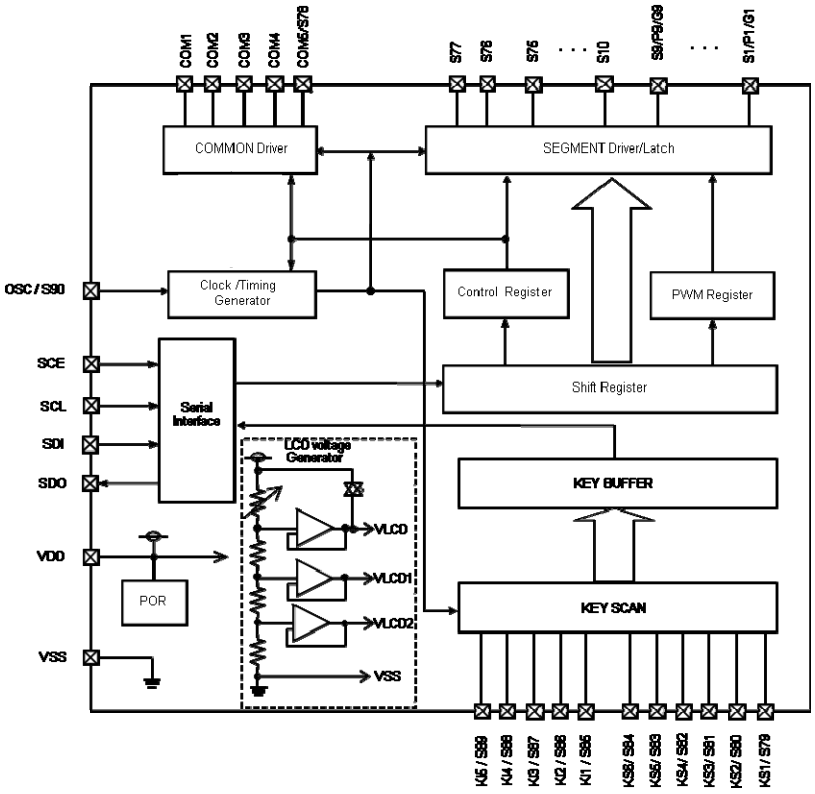


Figure 2. Block Diagram

Pin Arrangement

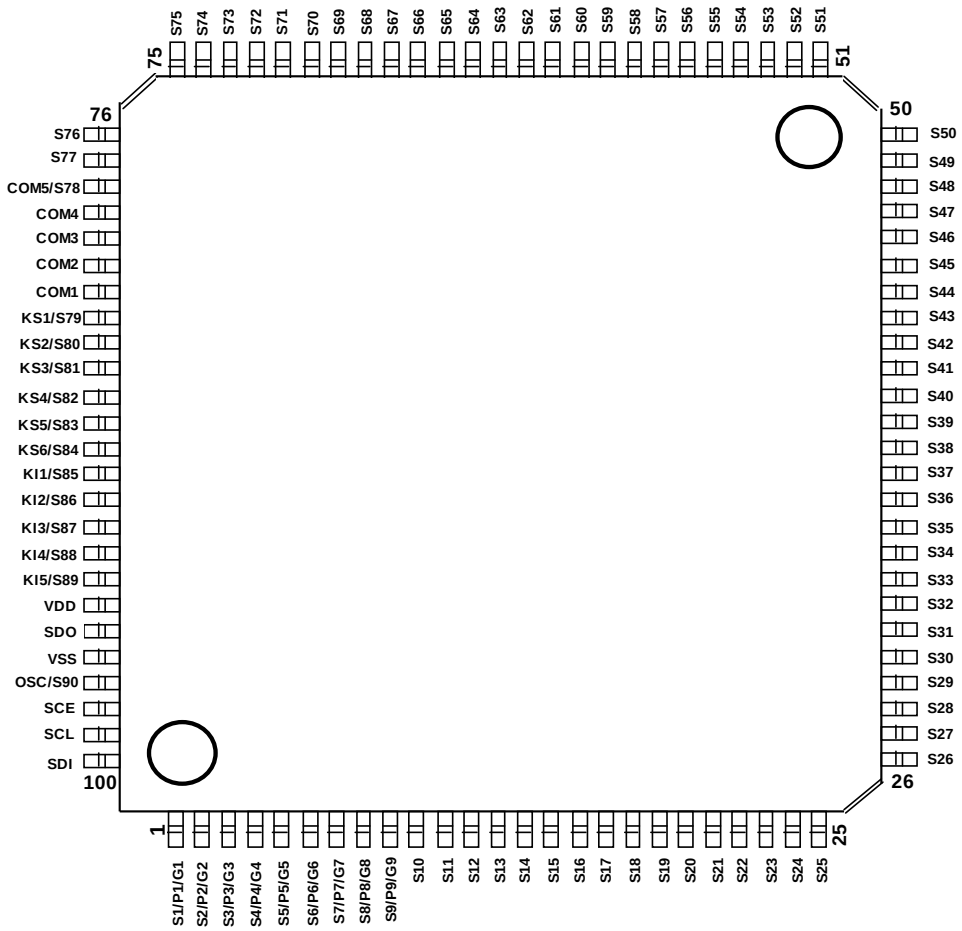


Figure 3. Pin Configuration(TOP VIEW)

Absolute Maximum Ratings(Ta = 25°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VDD max	VDD	-0.3 to +6.5	V
Input voltage	VIN1	SCE, SCL, SDI	-0.3 to +6.5	V
	VIN2	KI1 to KI5	-0.3 to +6.5	V
Allowable loss	Pd		1.49(Note3)	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

(Note3) Derate by 1.49mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 to +85°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	VH1	SCE, SCL, SDI		-	0.03VDD	-	V
	VH2	KI1 to KI5		-	0.1VDD	-	V
Power-on Detection Voltage	VDET	VDD		1.4	1.8	2.2	V
"H" Level Input Voltage	VIH1	SCE, SCL, SDI	4.0V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	VIH2	SCE, SCL, SDI	2.7V ≤ VDD < 4.0V	0.8VDD	-	VDD	V
	VIH3	KI1 to KI5		0.7VDD	-	VDD	V
"L" Level Input Voltage	VIL1	SCE, SCL, SDI KI1 to KI5		0	-	0.2VDD	V
Input Floating Voltage	VIF	KI1 to KI5		-	-	0.05VDD	V
Pull-down Resistance	RPD	KI1 to KI5	VDD=5.0V	50	100	250	KΩ
Output Off Leakage Current	IOFFH	SDO	VO=6.0V	-	-	6.0	μA
"H" Level Input Current	IIH1	SCE, SCL, SDI	VI = 5.5V	-	-	5.0	μA
"L" Level Input Current	IIL1	SCE, SCL, SDI	VI = 0V	-5.0	-	-	μA
"H" Level Output Voltage	VOH1	S1 to S90	IO = -20μA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	VOH2	COM1 to COM5	IO = -100μA, VLCD=1.00*VDD	VDD-0.9	-	-	
	VOH3	P1/G1 to P9/G9	IO = -1mA	VDD-0.9	-	-	
	VOH4	KS1 to KS6	IO = -500uA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	VOL1	S1 to S90	IO = 20μA	-	-	0.9	V
	VOL2	COM1 to COM5	IO = 100μA	-	-	0.9	
	VOL3	P1/G1 to P9/G9	IO = 1mA	-	-	0.9	
	VOL4	KS1 to KS6	IO = 25uA	0.2	0.5	1.5	
	VOL5	SDO	IO = 1mA	-	0.1	0.5	
Middle Level Output Voltage	VMID1	S1 to S90	1/2 bias IO = ±20μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	V
	VMID2	COM1 to COM5	1/2 bias IO = ±100μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	
	VMID3	S1 to S90	1/3 bias IO = ±20μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID4	S1 to S90	1/3 bias IO = ±20μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
	VMID5	COM1 to COM5	1/3 bias IO = ±100μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID6	COM1 to COM5	1/3 bias IO = ±100μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
Current Consumption	IDD1	VDD	Power-saving mode	-	-	15	μA
	IDD2	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	100	200	
	IDD3	VDD	VDD = 5.0V Output open,1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	250	

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	fosc1	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	fosc2	-	VDD = 5V	510	600	690	kHz
External Clock Frequency(Note4)	fosc3	OSC/S90	External clock mode (OC=1)	30	-	1000	kHz
External Clock Duty	tdty	OSC/S90	External clock mode (OC=1)	30	50	70	%

(Note4) Frame frequency is decided external frequency and dividing ratio of FC0,FC1,FC2 setting.

【Reference Data】

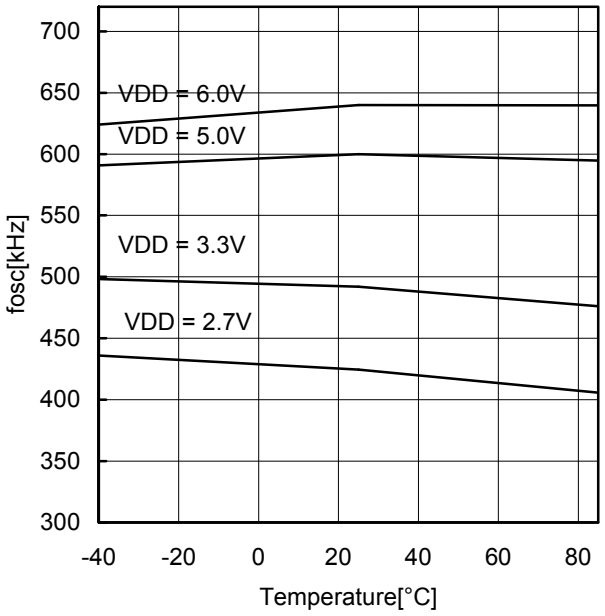
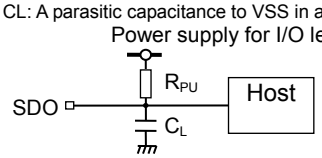


Figure 4. Typical Temperature Characteristics

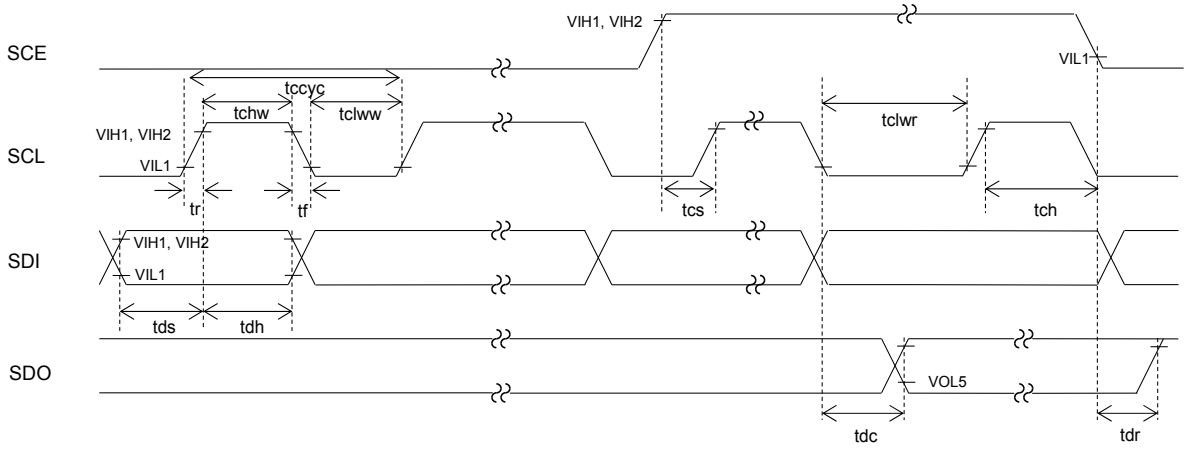
MPU Interface Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	tds	SCL, SDI		120	-	-	ns
Data Hold Time	tdh	SCL, SDI		120	-	-	ns
SCE Wait Time	tcp	SCE, SCL		120	-	-	ns
SCE Setup Time	tcs	SCE, SCL		120	-	-	ns
SCE Hold Time	tch	SCE, SCL		120	-	-	ns
Clock Cycle Time	tccyc	SCL		320	-	-	ns
High-level Clock Pulse Width	tchw	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	tclww	SCL		120	-	-	ns
Low-Level Clock Pulse Width (Read)	tclwr	SCL	RPU=4.7KΩ CL=10pF(Note5)	1.6	-	-	us
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
SDO Output Delay Time	tdc	SDO	RPU=4.7KΩ CL=10pf(Note5)	-	-	1.5	μs
SDO Rise Time	Tdr	SDO	RPU=4.7KΩ CL=10pf(Note5)	-	-	1.5	μs

(Note5) Since SDO is an open-drain output, “tdc” and “tdr” depend on the resistance of the pull-up resistor RPU and the load capacitance CL.
RPU: 1kΩ≤RPU≤10kΩ is recommended.
CL: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

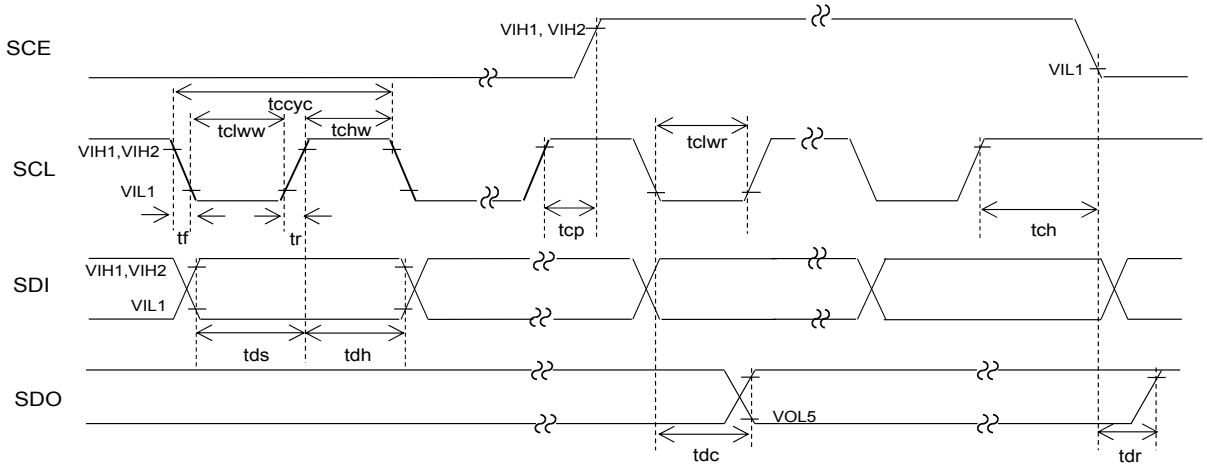


Figure 5.Serial Interface Timing

Pin Description

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	1 to 9	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S9/P9/G9 pins can also be used as General –purpose outputs when so set up by the control data.	-	O	OPEN
S10 to S77	10 to 77	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S79 to KS6/S84	83 to 88	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S79 to KS6/S84 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S85 to KI5/S89	89 to 93	Key scan inputs These pins have built-in pull-down resistors. The KI1/S85 to KI5/S89 pins can be used as segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	79 to 82	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
COM5/S78	78	COMMON / SEGMENT output for LCD driving Assigned as COMMON output in1/5 Duty mode and SEGMENT output in 1/1 Duty, 1/3 Duty and 1/4 Duty modes	-	O	OPEN
OSC/S90	97	Segment output for displaying the display data transferred by serial data input. The pin OSC/S90 can be used as external frequency input pin when set up by the control data.	-	I/O	OPEN
SCE SCL SDI	98 99 100	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	H ↑ -	I I I	GND
SDO	95	Output data	-	O	OPEN
VDD	94	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	96	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalent Circuit

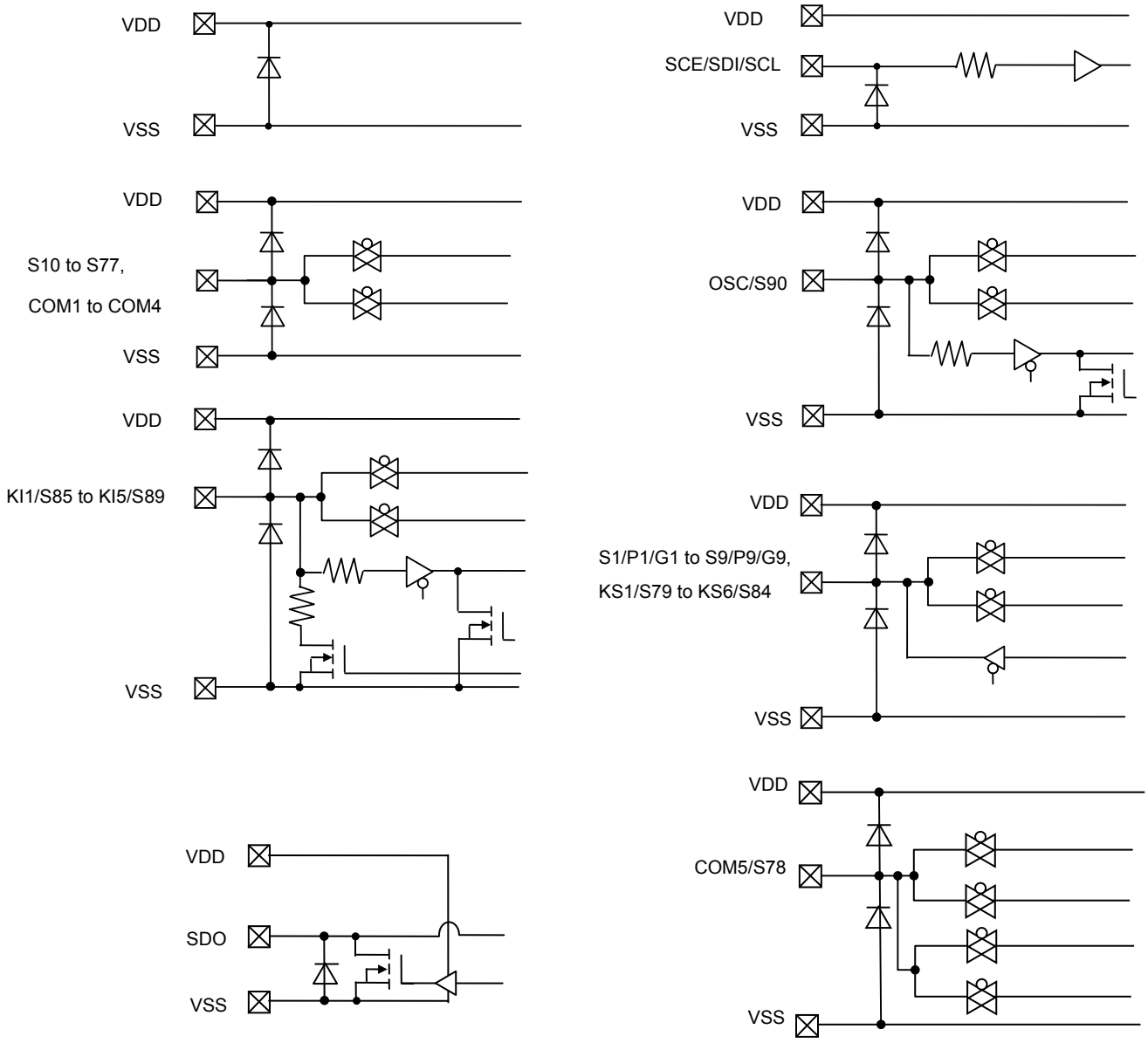


Figure 6. I/O Equivalent Circuit

Serial Data Transfer Formats

1.1/5-Duty

(1)When SCL is stopped at the low level

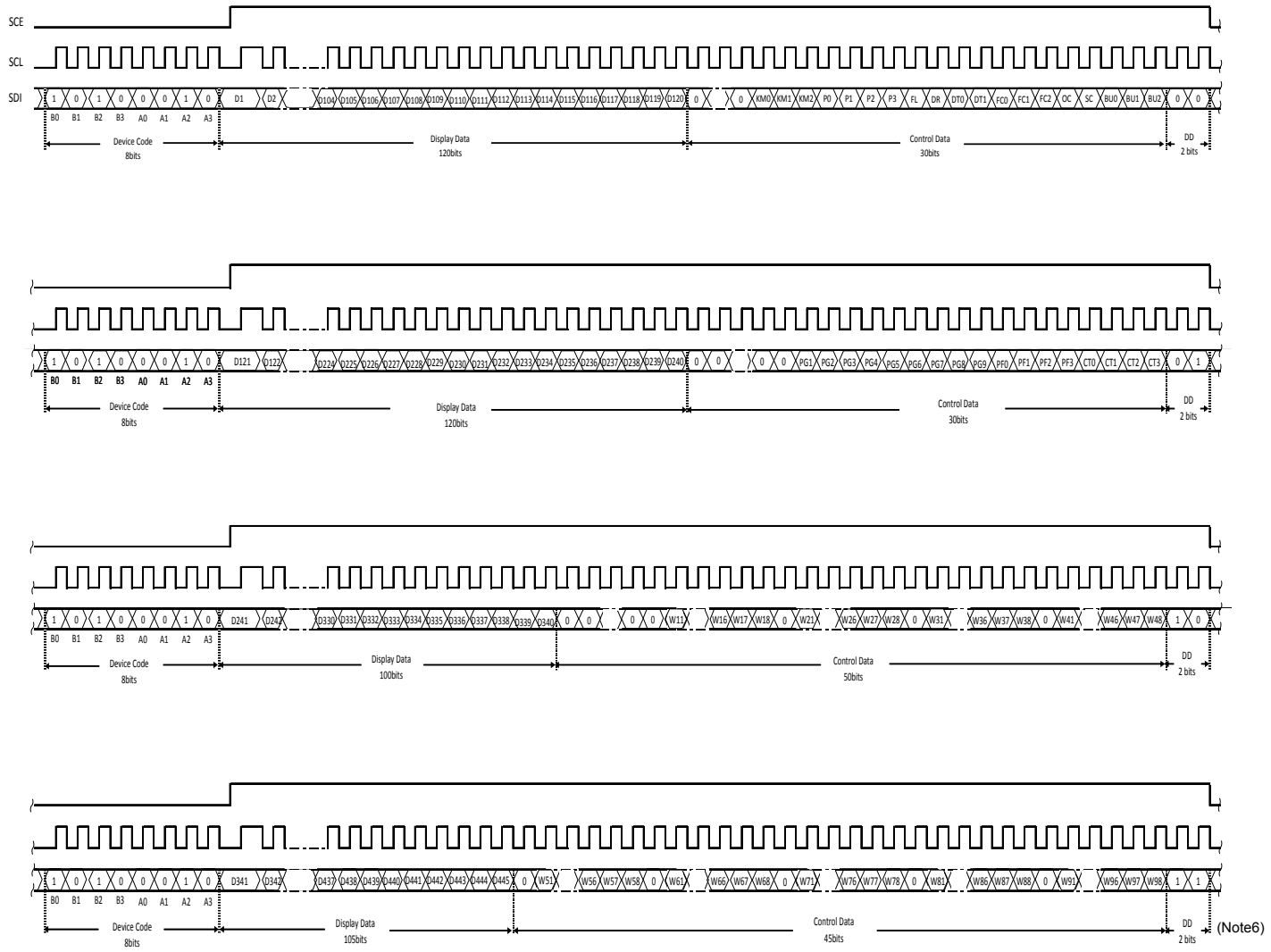


Figure 7. 3-SPI Data Transfer Format

(Note6) DD is direction data.

(2)When SCL is stopped at the high level

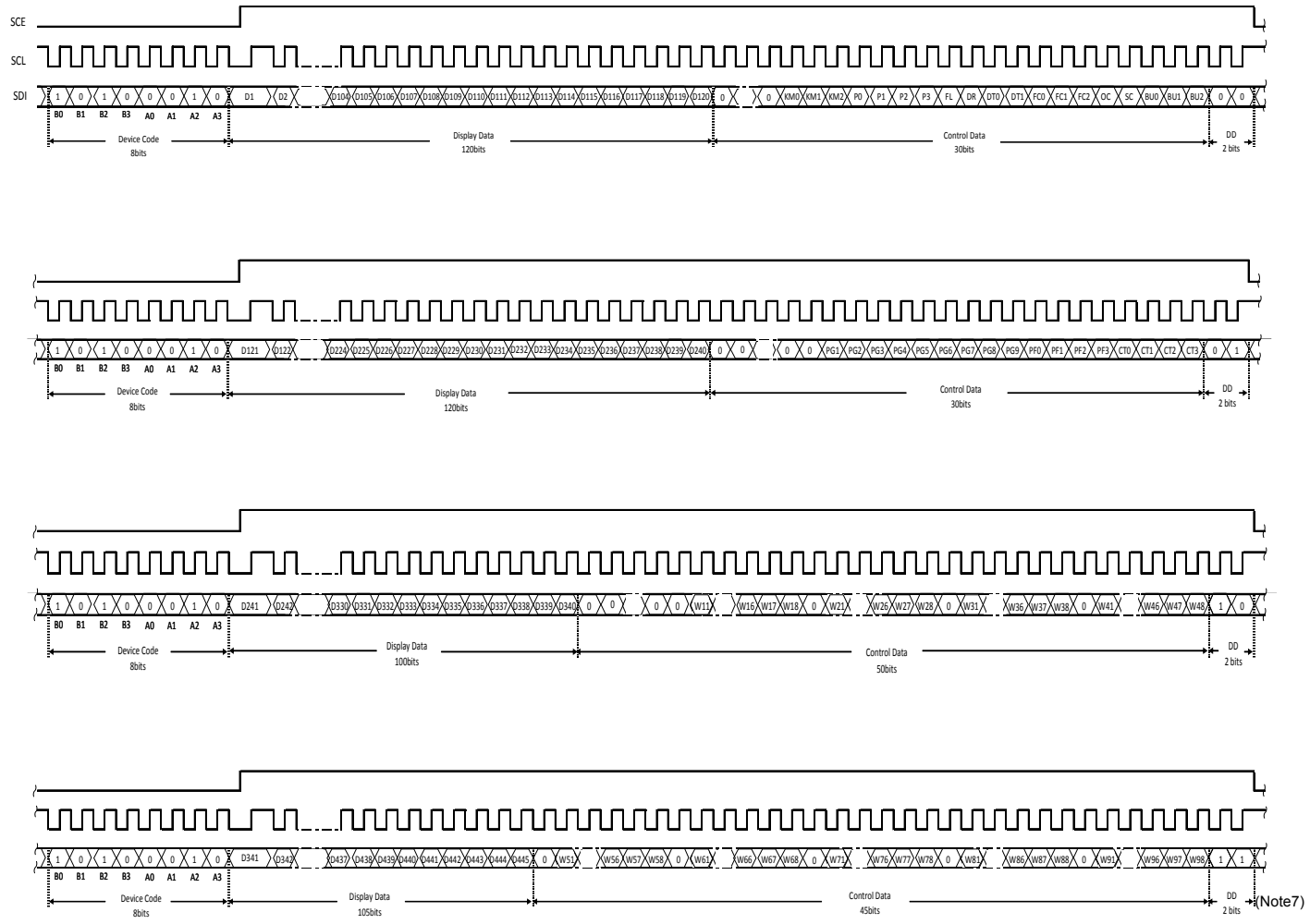


Figure 8. 3-SPI Data Transfer Format

(Note7) DD is direction data.

- Device code·····”45H”
- KM0～KM2·····Key Scan output port/Segment output port switching control data
- D1～D445·····Display data
- P0～P3·····Segment / PWM / General Purpose output port switching control data
- FL·····Line Inversion or Frame Inversion switching control data
- DR·····1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1·····1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0～FC3·····Common/Segment output waveform frame frequency switching control data
- OC····· Internal oscillator operating mode/External clock operating mode switching control data
- SC·····Segment on/off switching control data
- BU0～BU2·····Normal mode/power-saving mode switching control data
- PG1～PG9····· PWM/General Purpose output switching control data
- PF0～PF3·····PWM output waveform frame frequency switching control data
- CT0～CT3·····LCD display contrast switching control data
- W11～W18, W21～W28, W31～W38,W41～W48, W51～W58, W61～W68, W71~W78, W81~W88, W91~W98 ·····PWM output duty switching control data

2. 1/4-Duty

(1)When SCL is stopped at the low level

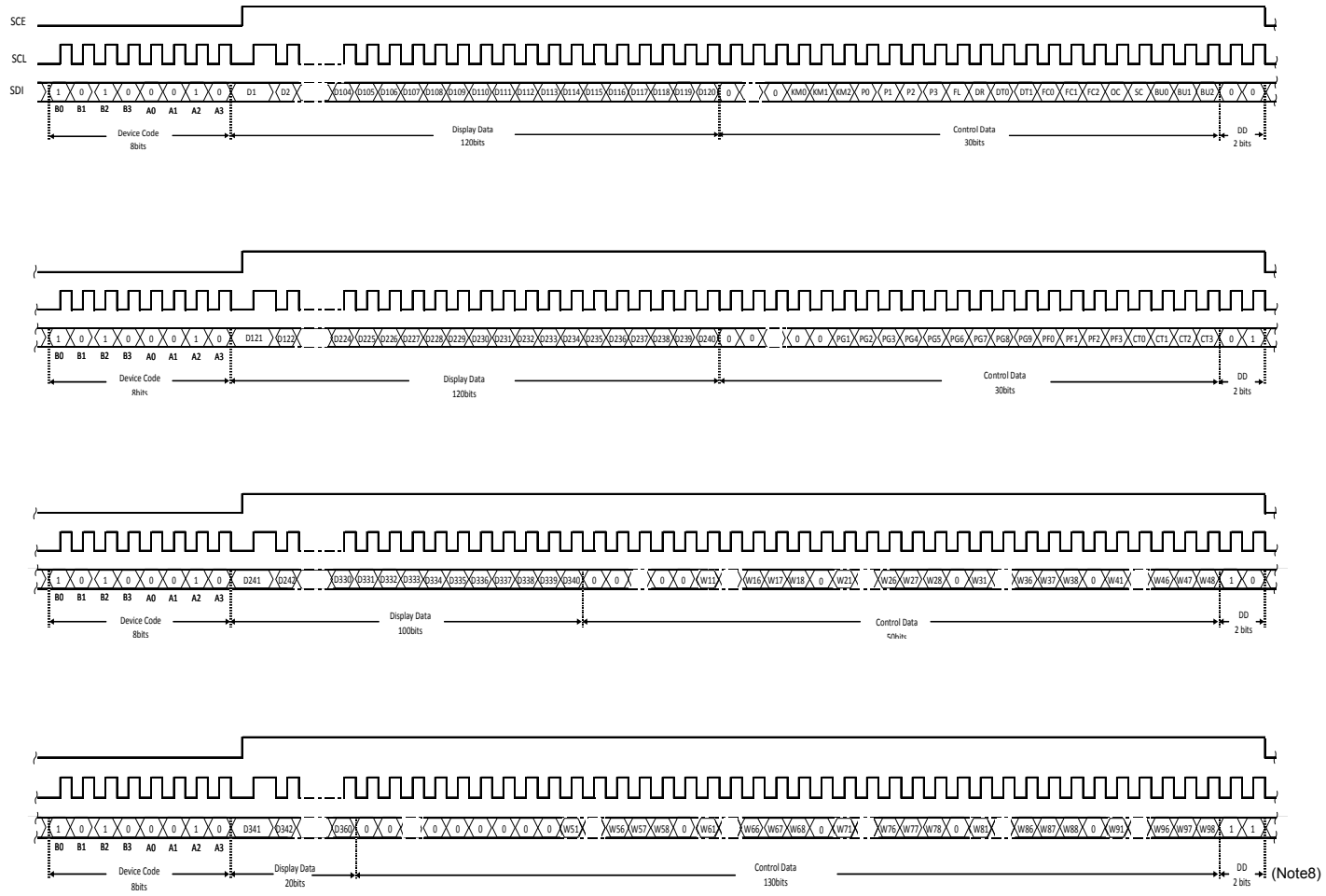


Figure 9. 3-SPI Data Transfer Format

(Note8) DD is direction data.

(2)When SCL is stopped at the high level

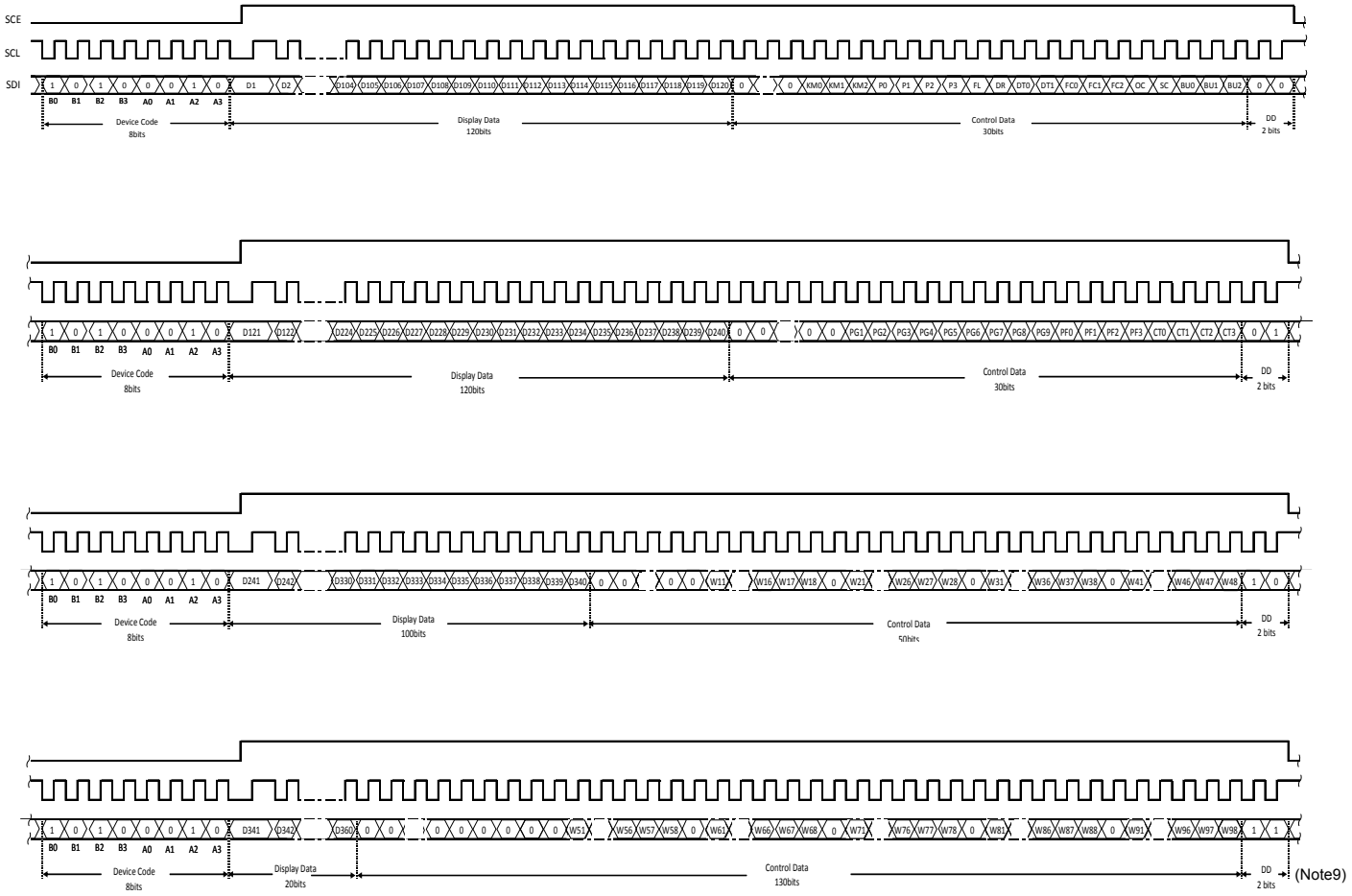


Figure 10. 3-SPI Data Transfer Format

(Note9) DD is direction data.

- Device code·····”45H”
- KM0～KM2·····Key Scan output port/Segment output port switching control data
- D1～D445·····Display data
- P0～P3·····Segment / PWM / General Purpose output port switching control data
- FL·····Line Inversion or Frame Inversion switching control data
- DR·····1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1·····1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0～FC3·····Common/Segment output waveform frame frequency switching control data
- OC····· Internal oscillator operating mode/External clock operating mode switching control data
- SC·····Segment on/off switching control data
- BU0～BU2·····Normal mode/power-saving mode switching control data
- PG1～PG9····· PWM/General Purpose output switching control data
- PF0～PF3·····PWM output waveform frame frequency switching control data
- CT0～CT3·····LCD display contrast switching control data
- W11～W18, W21～W28, W31～W38,W41～W48, W51～W58, W61～W68, W71~W78, W81~W88, W91~W98 ·····PWM output duty switching control data

3. 1/3-Duty

(1) When SCL is stopped at the low level

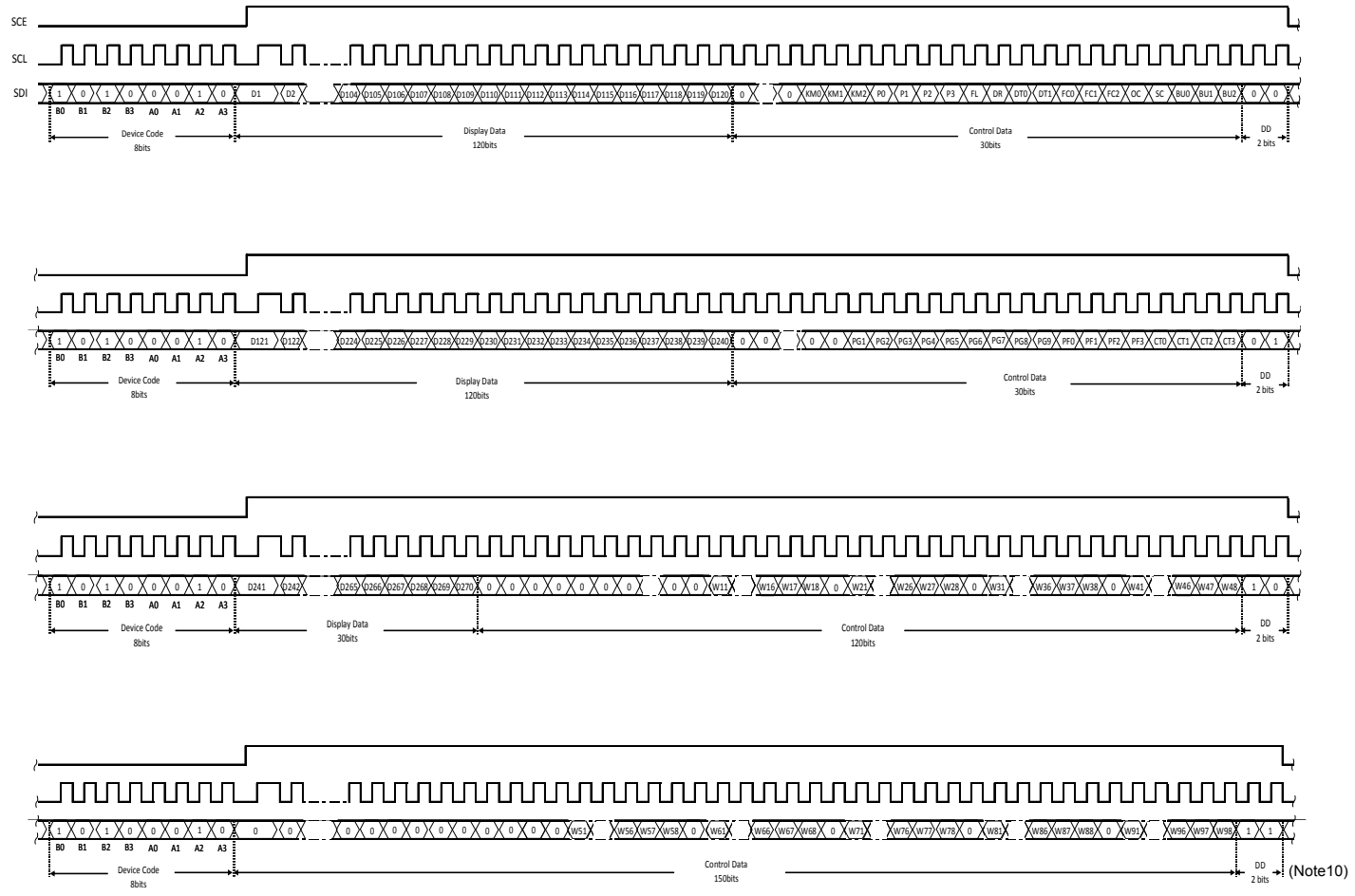


Figure 11. 3-SPI Data Transfer Format

(Note10) DD is direction data.

(2)When SCL is stopped at the high level

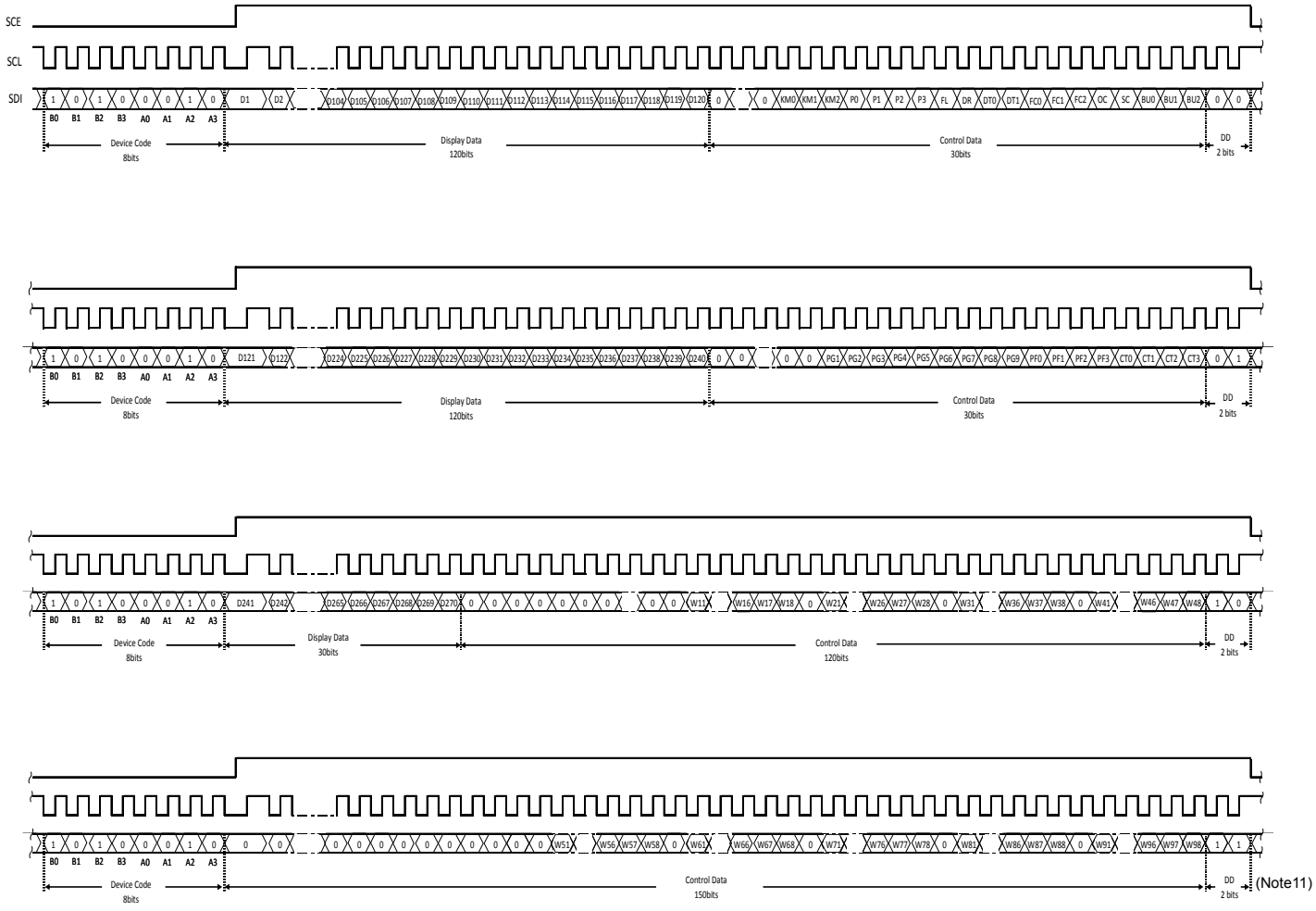


Figure 12. 3-SPI Data Transfer Format

(Note11) DD is direction data.

・Device code・・・・・・・・・・・・・・・・・・・”45H”
・KM0～KM2・・・・・・・・・・・・・・・・・・・Key Scan output port/Segment output port switching control data
・D1～D445・・・・・・・・・・・・・・・・・・・・Display data
・P0～P3・・・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
・FL・・・・・・・・・・・・・・・・・・・・・・・・・・Line Inversion or Frame Inversion switching control data
・DR・・・・・・・・・・・・・・・・・・・・・・・・・1/3 bias drive or 1/2 bias drive switching control data
・DT0~DT1・・・・・・・・・・・・・・・・・・・・1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
・FC0～FC3・・・・・・・・・・・・・・・・・・・・Common/Segment output waveform frame frequency switching control data
・OC・・・・・・・・・・・・・・・・・・・・・・・・・ Internal oscillator operating mode/External clock operating mode switching control data
・SC・・・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
・BU0～BU2・・・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
・PG1～PG9・・・・・・・・・・・・・・・・・・・ PWM/General Purpose output switching control data
・PF0～PF3・・・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data
・CT0～CT3・・・・・・・・・・・・・・・・・・・・LCD display contrast switching control data
・W11～W18, W21～W28, W31～W38,W41～W48, W51～W58, W61～W68, W71~W78, W81~W88, W91~W98
・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・PWM output duty switching control data

4. 1/1-Duty(Static)

(1)When SCL is stopped at the low level

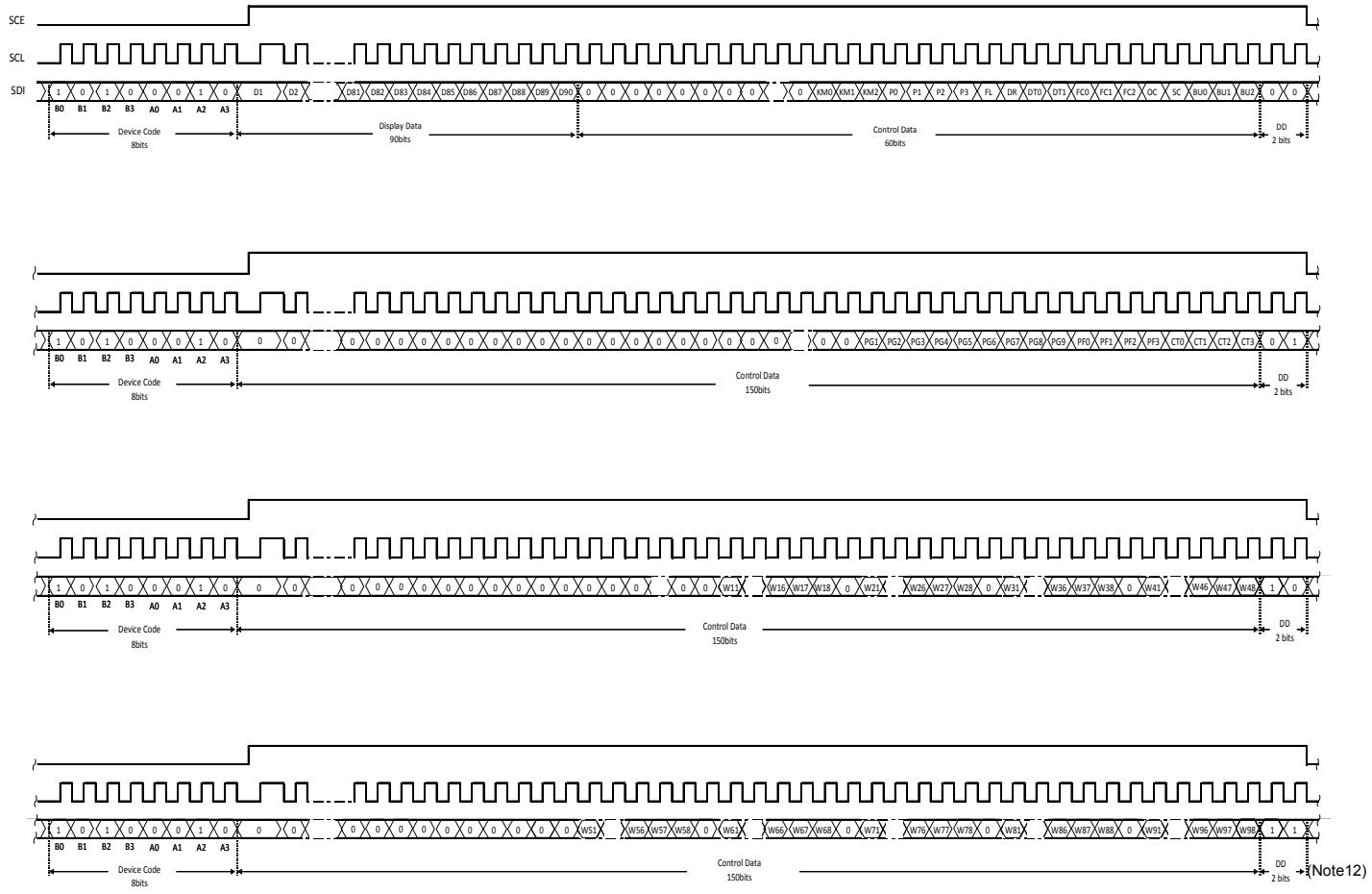


Figure 13. 3-SPI Data Transfer Format

(Note12) DD is direction data.

(2)When SCL is stopped at the high level

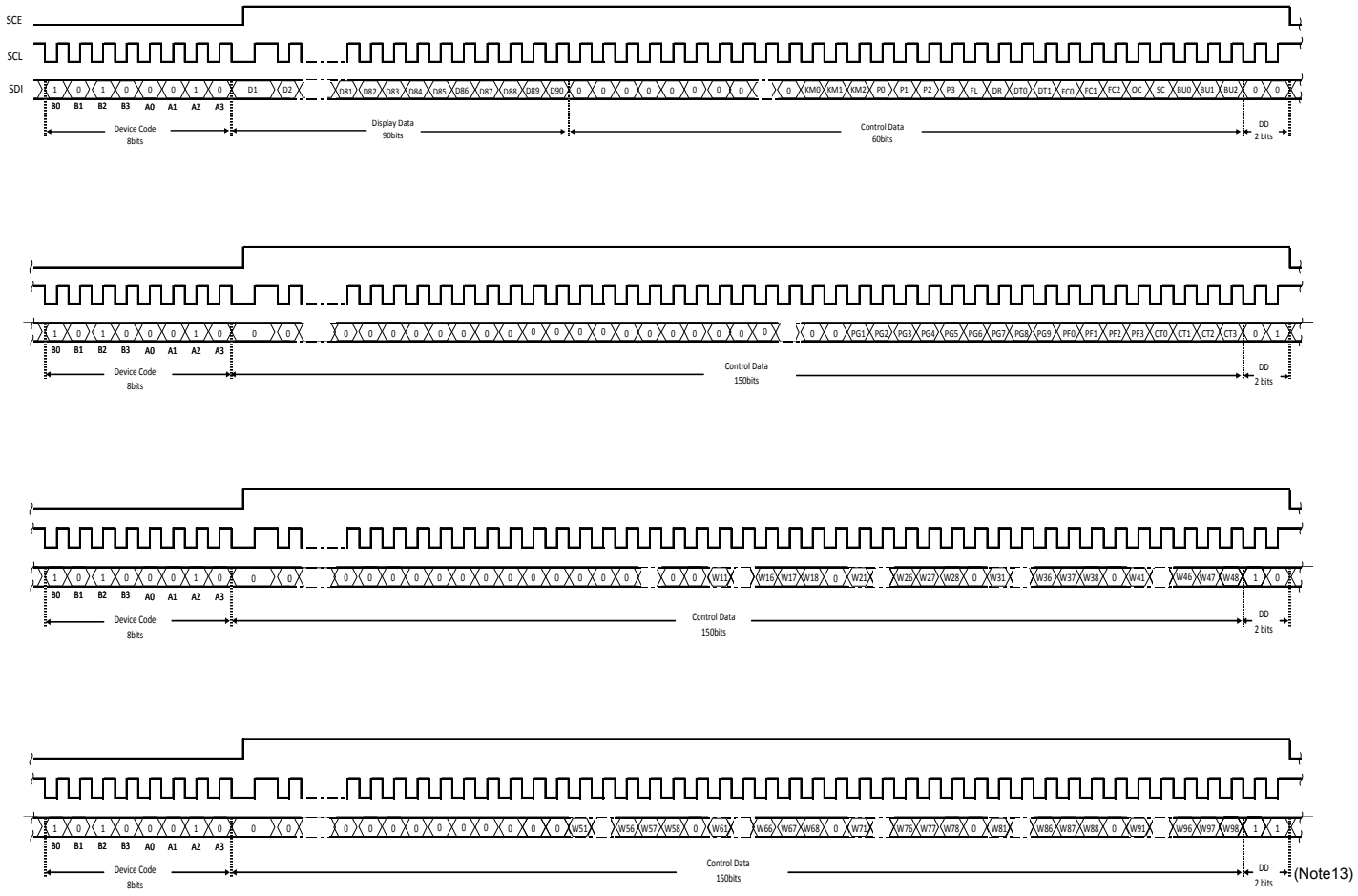


Figure 14. 3-SPI Data Transfer Format

(Note13) DD is direction data.

・Device code・・・・・・・・・・・・・・・・・・・・”45H”
・KM0～KM2・・・・・・・・・・・・・・・・・・・・Key Scan output port/Segment output port switching control data
・D1～D445・・・・・・・・・・・・・・・・・・・・Display data
・P0～P3・・・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
・FL・・・・・・・・・・・・・・・・・・・・・・・・・・Line Inversion or Frame Inversion switching control data
・DR・・・・・・・・・・・・・・・・・・・・・・・・・1/3 bias drive or 1/2 bias drive switching control data
・DT0~DT1・・・・・・・・・・・・・・・・・・・・・1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
・FC0～FC3・・・・・・・・・・・・・・・・・・・・Common/Segment output waveform frame frequency switching control data
・OC・・・・・・・・・・・・・・・・・・・・・・・・・ Internal oscillator operating mode/External clock operating mode switching control data
・SC・・・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
・BU0～BU2・・・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
・PG1～PG9・・・・・・・・・・・・・・・・・・・・ PWM/General Purpose output switching control data
・PF0～PF3・・・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data.
・CT0～CT3・・・・・・・・・・・・・・・・・・・・LCD display contrast switching control data.
・W11～W18, W21～W28, W31～W38,W41～W48, W51～W58, W61～W68, W71~W78, W81~W88, W91~W98
・・PWM output duty switching control data.

Control Data Functions

1. KM0,KM1 and KM2: Key Scan output port/Segment output port switching control data
These control data bits switch the functions of the KS1/S79 to KS6/S84 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys
			KS1/S79	KS2/S80	KS3/S81	KS4/S82	KS5/S83	KS6/S84	
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30
0	0	1	S79	KS2	KS3	KS4	KS5	KS6	25
0	1	0	S79	S80	KS3	KS4	KS5	KS6	20
0	1	1	S79	S80	S81	KS4	KS5	KS6	15
1	0	0	S79	S80	S81	S82	KS5	KS6	10
1	0	1	S79	S80	S81	S82	S83	KS6	5
1	1	0	S79	S80	S81	S82	S83	S84	0
1	1	1	S79	S80	S81	S82	S83	S84	0

2. P0,P1,P2 and P3: Segment / PWM / General Purpose output port switching control data
These control bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/S9
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9

PWM output or General Purpose output is selected by PGx(x=1～9) control data bit.

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/5 Duty mode	1/4 Duty mode	1/3 Duty mode	1/1 Duty (static) mode
S1/P1/G1	D1	D1	D1	D1
S2/P2/G2	D6	D5	D4	D2
S3/P3/G3	D11	D9	D7	D3
S4/P4/G4	D16	D13	D10	D4
S5/P5/G5	D21	D17	D13	D4
S6/P6/G6	D26	D21	D16	D5
S7/P7/G7	D31	D25	D19	D7
S8/P8/G8	D36	D29	D22	D8
S9/P9/G9	D41	D33	D25	D9

When the General Purpose Output Port Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, at 1/4 Duty mode, S4/P4/G4 is used as a General Purpose Output Port, if its corresponding display data D13 is set to “1”, then S4/P4/G4 will output “HIGH” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “LOW” level.

3. FL: Line Inversion or Frame Inversion switching control data
This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode
0	Line Inversion
1	Frame Inversion

4. DR: 1/3 bias drive or 1/2 bias drive switching control data
This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

5. DT: 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
These control data bits select either 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty (static) drive

DT0	DT1	Duty drive scheme
0	0	1/1 duty (static) drive
0	1	1/3 duty drive
1	0	1/4 duty drive
1	1	1/5 duty drive

6. FC0, FC1, FC2 and FC3: Common/Segment output waveform frame frequency switching control data
These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	FC3	Frame Frequency fo(Hz)
0	0	0	0	fosc(Note14) / 12288
0	0	0	1	fosc / 10752
0	0	1	0	fosc / 9216
0	0	1	1	fosc / 7680
0	1	0	0	fosc / 6144
0	1	0	1	fosc / 4608
0	1	1	0	fosc / 3840
0	1	1	1	fosc / 3072
1	0	0	0	fosc / 2880
1	0	0	1	fosc / 2688
1	0	1	0	fosc / 2496
1	0	1	1	fosc / 2304
1	1	0	0	fosc / 2112
1	1	0	1	fosc / 1920
1	1	1	0	fosc / 1728
1	1	1	1	fosc / 1536

(Note14) fosc: Internal oscillation frequency (600 [kHz] typ.)

7. OC: Internal oscillator operating mode/External clock operating mode switching control data

OC	Operating mode	In/Out pin(OSC/S90) status
0	Internal oscillator	S90 (segment output)
1	External Clock	OSC (clock input)

8. SC: Segment on/off switching control data
This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

9. BU0,BU1 and BU2: Normal mode/power-saving mode switching control data
These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs / Common outputs	Output Pin States During Key Scan Standby					
						KS1	KS2	KS3	KS4	KS5	KS6
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	L	H
0	1	0				L	L	L	L	H	H
0	1	1				L	L	L	H	H	H
1	0	0				L	L	H	H	H	H
1	0	1				L	H	H	H	H	H
1	1	0				H	H	H	H	H	H
1	1	1				H	H	H	H	H	H

Power-saving mode status: S1/P1/G1 to S9/P9/G9 = active only General Purpose output
S10 to OSC/S90 = low (VSS)
COM1 to COM5 = low (VSS)
Stop the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when at Power-saving mode.

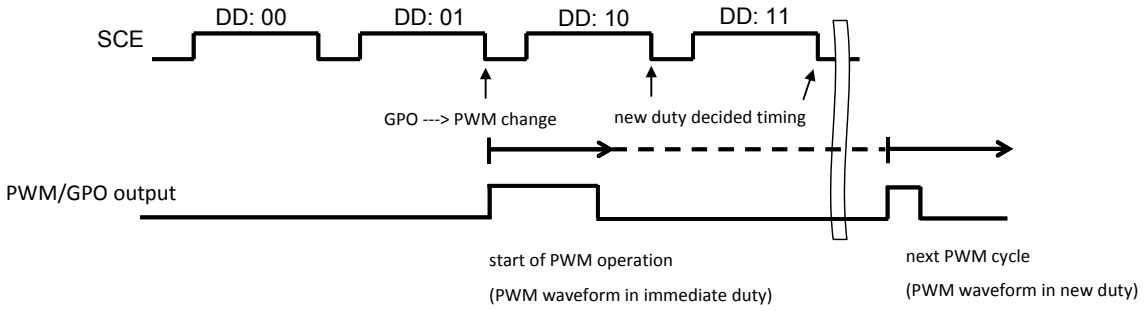
10. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM/General Purpose output switching control data
This control data bit select either PWM output or General Purpose output of Sx/Px/Gx pins. (x=1～9)

PGx(x=1～9)	Mode
0	PWM output
1	General Purpose output

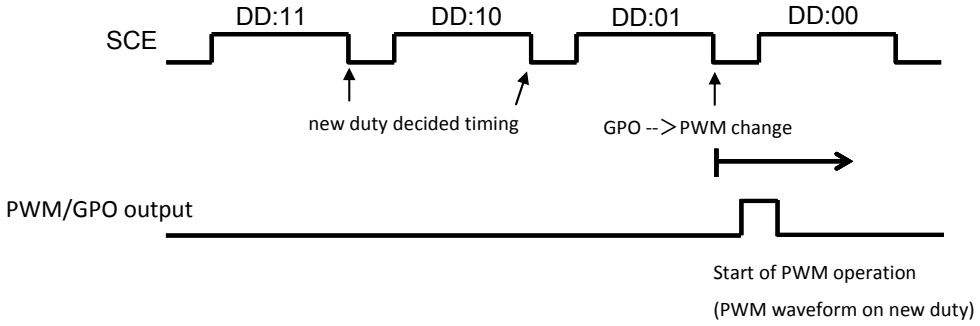
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO -→ PWM change.
- Please take care of reflect timing of new duty setting of DD: 10 and DD: 11 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency switching control data
These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)
0	0	0	0	fosc / 4096
0	0	0	1	fosc / 3840
0	0	1	0	fosc / 3584
0	0	1	1	fosc / 3328
0	1	0	0	fosc / 3072
0	1	0	1	fosc / 2816
0	1	1	0	fosc / 2560
0	1	1	1	fosc / 2304
1	0	0	0	fosc / 2048
1	0	0	1	fosc / 1792
1	0	1	0	fosc / 1536
1	0	1	1	fosc / 1280
1	1	0	0	fosc / 1024
1	1	0	1	fosc / 768
1	1	1	0	fosc / 512
1	1	1	1	fosc / 256

12. CT0, CT1, CT2 and CT3: LCD display contrast switching control data
These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level
0	0	0	0	1.000*VDD
0	0	0	1	0.975*VDD
0	0	1	0	0.950*VDD
0	0	1	1	0.925*VDD
0	1	0	0	0.900*VDD
0	1	0	1	0.875*VDD
0	1	1	0	0.850*VDD
0	1	1	1	0.825*VDD
1	0	0	0	0.800*VDD
1	0	0	1	0.775*VDD
1	0	1	0	0.750*VDD
1	0	1	1	0.725*VDD
1	1	0	0	0.700*VDD
1	1	0	1	0.675*VDD
1	1	1	0	0.650*VDD
1	1	1	1	0.625*VDD

13. W11～W18(Note15), W21～W28, W31～W38, W41～W48, W51～W58, W61～W68, W71～W78, W81～W88 and W90~W97: PWM output waveform duty setting control data.
These control data bits set the high level pulse width (duty) for PWM output waveforms.

N = 1 ~ 9 , Tp = 1/fp

Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty
0	0	0	0	0	0	0	0	(0/256) x Tp
0	0	0	0	0	0	0	1	(1/256) x Tp
0	0	0	0	0	0	1	0	(2/256) x Tp
0	0	0	0	0	0	1	1	(3/256) x Tp
0	0	0	0	0	1	0	0	(4/256) x Tp
0	0	0	0	0	1	0	1	(5/256) x Tp
0	0	0	0	0	1	1	0	(6/256) x Tp
0	0	0	0	0	1	1	1	(7/256) x Tp
0	0	0	0	1	0	0	0	(8/256) x Tp
0	0	0	0	1	0	0	1	(9/256) x Tp
0	0	0	0	1	0	1	0	(10/256) x Tp
0	0	0	0	1	0	1	1	(11/256) x Tp
0	0	0	0	1	1	0	0	(12/256) x Tp
0	0	0	0	1	1	0	1	(13/256) x Tp
0	0	0	0	1	1	1	0	(14/256) x Tp
0	0	0	0	1	1	1	1	(15/256) x Tp
0	0	0	1	0	0	0	0	(16/256) x Tp
0	0	0	1	0	0	0	1	(17/256) x Tp
0	0	0	1	0	0	1	0	(18/256) x Tp
0	0	0	1	0	0	1	1	(19/256) x Tp
0	0	0	1	0	1	0	0	(20/256) x Tp
・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・	・・・
1	1	1	0	1	0	1	1	(235/256) x Tp
1	1	1	0	1	1	0	0	(236/256) x Tp
1	1	1	0	1	1	0	1	(237/256) x Tp
1	1	1	0	1	1	1	0	(238/256) x Tp
1	1	1	0	1	1	1	1	(239/256) x Tp
1	1	1	1	0	0	0	0	(240/256) x Tp
1	1	1	1	0	0	0	1	(241/256) x Tp
1	1	1	1	0	0	1	0	(242/256) x Tp
1	1	1	1	0	0	1	1	(243/256) x Tp
1	1	1	1	0	1	0	0	(244/256) x Tp
1	1	1	1	0	1	0	1	(245/256) x Tp
1	1	1	1	0	1	1	0	(246/256) x Tp
1	1	1	1	0	1	1	1	(247/256) x Tp
1	1	1	1	1	0	0	0	(248/256) x Tp
1	1	1	1	1	0	0	1	(249/256) x Tp
1	1	1	1	1	0	1	0	(250/256) x Tp
1	1	1	1	1	0	1	1	(251/256) x Tp
1	1	1	1	1	1	0	0	(252/256) x Tp
1	1	1	1	1	1	0	1	(253/256) x Tp
1	1	1	1	1	1	1	0	(254/256) x Tp
1	1	1	1	1	1	1	1	(255/256) x Tp

(Note15) W11～W18:S1/P1/G1 pwm duty data
W21～W28:S2/P2/G2 pwm duty data
W31～W38:S3/P3/G3 pwm duty data
W41～W48:S4/P4/G4 pwm duty data
W51～W58:S5/P5/G5 pwm duty data
W61～W68:S6/P6/G6 pwm duty data
W71～W78:S7/P7/G7 pwm duty data
W81～W88:S8/P8/G8 pwm duty data
W91～W98:S9/P9/G9 pwm duty data

Display Data and Output Pin Correspondence

1. 1/5 duty

Output pin(Note16)	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
S53	D261	D262	D263	D264	D265
S54	D266	D267	D268	D269	D270
S55	D271	D272	D273	D274	D275
S56	D276	D277	D278	D279	D280
S57	D281	D282	D283	D284	D285
S58	D286	D287	D288	D289	D290
S59	D291	D292	D293	D294	D295
S60	D296	D297	D298	D299	D300
S61	D301	D302	D303	D304	D305
S62	D306	D307	D308	D309	D310
S63	D311	D312	D313	D314	D315

Output pin(Note16)	COM1	COM2	COM3	COM4	COM5
S64	D316	D317	D318	D319	D320
S65	D321	D322	D323	D324	D325
S66	D326	D327	D328	D329	D330
S67	D331	D332	D333	D334	D335
S68	D336	D337	D338	D339	D340
S69	D341	D342	D343	D344	D345
S70	D346	D347	D348	D349	D350
S71	D351	D352	D353	D354	D355
S72	D356	D357	D358	D359	D360
S73	D361	D362	D363	D364	D365
S74	D366	D367	D368	D369	D370
S75	D371	D372	D373	D374	D375
S76	D376	D377	D378	D379	D380
S77	D381	D382	D383	D384	D385
KS1/S79	D386	D387	D388	D389	D390
KS2/S80	D391	D392	D393	D394	D395
KS3/S81	D396	D397	D398	D399	D400
KS4/S82	D401	D402	D403	D404	D405
KS5/S83	D406	D407	D408	D409	D410
KS6/S84	D411	D412	D413	D414	D415
KI1/S85	D416	D417	D418	D419	D420
KI2/S86	D421	D422	D423	D424	D425
KI3/S87	D426	D427	D428	D429	D430
KI4/S88	D431	D432	D433	D434	D435
KI5/S89	D436	D437	D438	D439	D440
OSC/S90	D441	D442	D443	D444	D445

(Note16) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90. Also, COM5/S78 pin is used as Common output.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data					State of S21 Output Pin
D101	D102	D103	D104	D105	
0	0	0	0	0	LCD Segments corresponding to COM1 to COM5 are OFF.
0	0	0	0	1	LCD Segment corresponding to COM5 is ON.
0	0	0	1	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	1	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	1	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	1	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	1	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	1	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	1	0	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	0	1	LCD Segments corresponding to COM2 and COM5 are ON.
0	1	0	1	0	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	0	1	1	LCD Segments corresponding to COM2, COM4 and COM5 are ON.
0	1	1	0	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	0	1	LCD Segments corresponding to COM2, COM3, and COM5 are ON.
0	1	1	1	0	LCD Segments corresponding to COM2, COM3, and COM4 are ON.
0	1	1	1	1	LCD Segments corresponding to COM2, COM3, COM4 and COM5 are ON.
1	0	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	0	1	LCD Segments corresponding to COM1 and COM5 are ON.
1	0	0	1	0	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	0	1	1	LCD Segments corresponding to COM1, COM4 and COM5 are ON.
1	0	1	0	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	0	1	LCD Segments corresponding to COM1, COM3 and COM5 are ON.
1	0	1	1	0	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	0	1	1	1	LCD Segments corresponding to COM1, COM3, COM4 and COM5 are ON.
1	1	0	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	0	1	LCD Segments corresponding to COM1, COM2 and COM5 are ON.
1	1	0	1	0	LCD Segments corresponding to COM1, COM2 and COM4 are ON.
1	1	0	1	1	LCD Segments corresponding to COM1, COM2, COM4 and COM5 are ON.
1	1	1	0	0	LCD Segments corresponding to COM1, COM2 and COM3 are ON.
1	1	1	0	1	LCD Segments corresponding to COM1, COM2, COM3 and COM5 are ON.
1	1	1	1	0	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.
1	1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3, COM4 and COM5 are ON.

2.1/4 duty

Output pin(Note17)	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7/P7/G7	D25	D26	D27	D28
S8/P8/G8	D29	D30	D31	D32
S9/P9/G9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252

Output pin(Note17)	COM1	COM2	COM3	COM4
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
S70	D277	D278	D279	D280
S71	D281	D282	D283	D284
S72	D285	D286	D287	D288
S73	D289	D290	D291	D292
S74	D293	D294	D295	D296
S75	D297	D298	D299	D300
S76	D301	D302	D303	D304
S77	D305	D306	D307	D308
COM5/S78	D309	D310	D311	D312
KS1/S79	D313	D314	D315	D316
KS2/S80	D317	D318	D319	D320
KS3/S81	D321	D322	D323	D324
KS4/S82	D325	D326	D327	D328
KS5/S83	D329	D330	D331	D332
KS6/S84	D333	D334	D335	D336
KI1/S85	D337	D338	D339	D340
KI2/S86	D341	D342	D343	D344
KI3/S87	D345	D346	D347	D348
KI4/S88	D349	D350	D351	D352
KI5/S89	D353	D354	D355	D356
OSC/S90	D357	D358	D359	D360

(Note17) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.

3. 1/3 duty

Output pin(Note18)	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7/P7/G7	D19	D20	D21
S8/P8/G8	D22	D23	D24
S9/P9/G9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189

Output pin(Note18)	COM1	COM2	COM3
S64	D190	D191	D192
S65	D193	D194	D195
S66	D196	D197	D198
S67	D199	D200	D201
S68	D202	D203	D204
S69	D205	D206	D207
S70	D208	D209	D210
S71	D211	D212	D213
S72	D214	D215	D216
S73	D217	D218	D219
S74	D220	D221	D222
S75	D223	D224	D225
S76	D226	D227	D228
S77	D229	D230	D231
COM5/S78	D232	D233	D234
KS1/S79	D235	D236	D237
KS2/S80	D238	D239	D240
KS3/S81	D241	D242	D243
KS4/S82	D244	D245	D246
KS5/S83	D247	D248	D249
KS6/S84	D250	D251	D252
KI1/S85	D253	D254	D255
KI2/S86	D256	D257	D258
KI3/S87	D259	D260	D261
KI4/S88	D262	D263	D264
KI5/S89	D265	D266	D267
OSC/S90	D268	D269	D270

(Note18) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90

To illustrate further, the states of the S21 output pin is given in the table below.

Display data			State of S21 Output Pin
D61	D62	D63	
0	0	0	LCD Segments corresponding to COM1 to COM3 are OFF.
0	0	1	LCD Segment corresponding to COM3 is ON.
0	1	0	LCD Segment corresponding to COM2 is ON.
0	1	1	LCD Segments corresponding to COM2 and COM3 are ON.
1	0	0	LCD Segment corresponding to COM1 is ON.
1	0	1	LCD Segments corresponding to COM1 and COM3 are ON.
1	1	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	1	LCD Segments corresponding to COM1, COM2 and COM3 are ON.

4. 1/1 duty(Static)

Output pin(Note19)	COM1
S1/P1/G1	D1
S2/P2/G2	D2
S3/P3/G3	D3
S4/P4/G4	D4
S5/P5/G5	D5
S6/P6/G6	D6
S7/P7/G7	D7
S8/P8/G8	D8
S9/P9/G9	D9
S10	D10
S11	D11
S12	D12
S13	D13
S14	D14
S15	D15
S16	D16
S17	D17
S18	D18
S19	D19
S20	D20
S21	D21
S22	D22
S23	D23
S24	D24
S25	D25
S26	D26
S27	D27
S28	D28
S29	D29
S30	D30
S31	D31
S32	D32
S33	D33
S34	D34
S35	D35
S36	D36
S37	D37
S38	D38
S39	D39
S40	D40
S41	D41
S42	D42
S43	D43
S44	D44
S45	D45
S46	D46
S47	D47
S48	D48
S49	D49
S50	D50
S51	D51
S52	D52
S53	D53
S54	D54
S55	D55
S56	D56
S57	D57
S58	D58
S59	D59
S60	D60
S61	D61
S62	D62
S63	D63
S64	D64

Output pin(Note19)	COM1
S65	D65
S66	D66
S67	D67
S68	D68
S69	D69
S70	D70
S71	D71
S72	D72
S73	D73
S74	D74
S75	D75
S76	D76
S77	D77
COM5/S78	D78
KS1/S79	D79
KS2/S80	D80
KS3/S81	D81
KS4/S82	D82
KS5/S83	D83
KS6/S84	D84
KI1/S85	D85
KI2/S86	D86
KI3/S87	D87
KI4/S88	D88
KI5/S89	D89
OSC/S90	D90

(Note19) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data D21	State of S21 Output Pin
0	LCD Segment corresponding to COM1 is ON.
1	LCD Segment corresponding to COM1 is OFF.

Serial Data Output

1. When SCL is stopped at the low level(Note20)

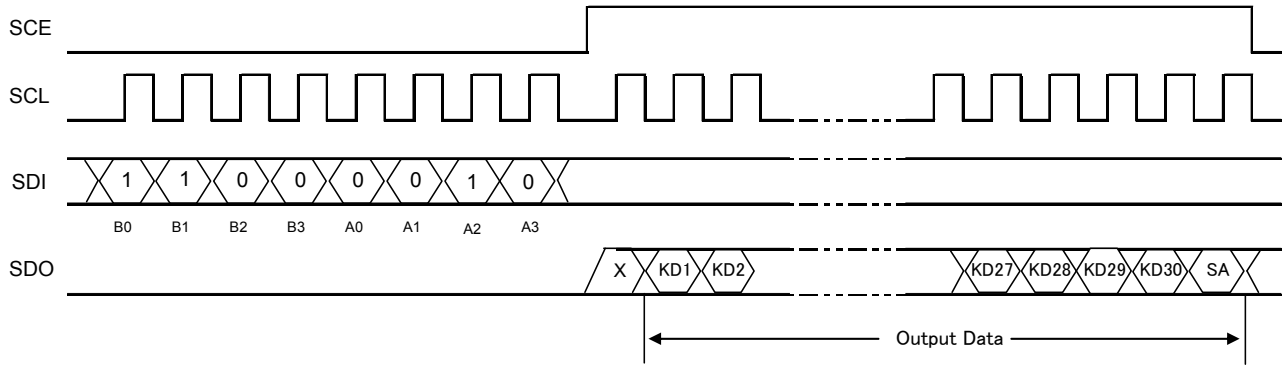


Figure 15. Serial Data Output Format

(Note20)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address

2. When SCL is stopped at the high level(Note21)

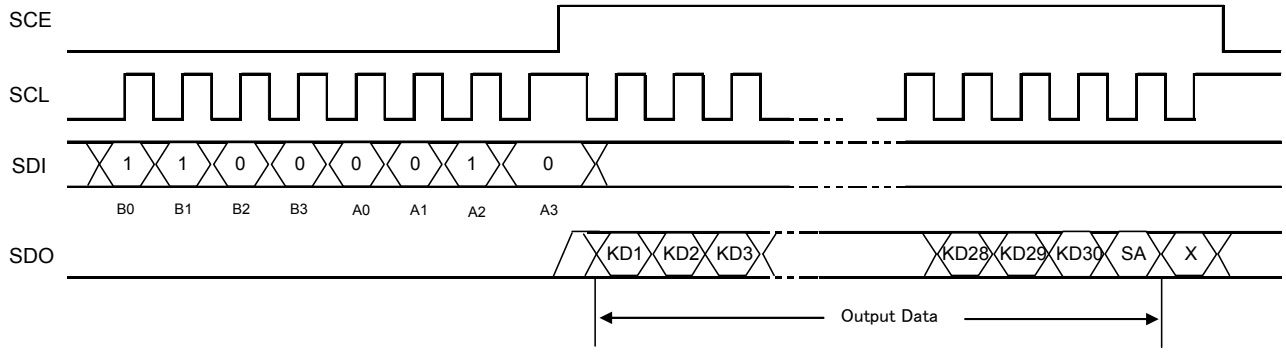


Figure 16. Serial Data Output Format

(Note21)
1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD30: Key data
5. SA: Sleep acknowledge data
6. If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

Output Data

1. KD1 TO KD30: KEY DATA

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

Item	KI1	KI2	KI3	KI4	KI5
KS1	KD1	KD2	KD3	KD4	KD5
KS2	KD6	KD7	KD8	KD9	KD10
KS3	KD11	KD12	KD13	KD14	KD15
KS4	KD16	KD17	KD18	KD19	KD20
KS5	KD21	KD22	KD23	KD24	KD25
KS6	KD26	KD27	KD28	KD29	KD30

2. SA: Sleep Acknowledge Data

This output data is set to the state when the key is pressed. In that case SDO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 1 in the sleep mode and to 0 in the normal mode.

Sleep Mode

Sleep mode is set up by setting the BU0 to BU2 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with all the BU0 to BU2 set to 0. However, note that the S1/P1/G1 to S9/P9/G9 outputs can be used as general-purpose output ports according to the state of the P0 to P3 control data bits, even in sleep mode. (See Control Data Functions.)

Key Scan Operation Function

1. Key scan timing

The key scan period is 4608T(s). To reliably determine the on/off state of the keys, the BU97530KVT-M scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on SDO) 9840T(s) after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the BU97530KVT-M cannot detect a key press shorter than 9840T(s).

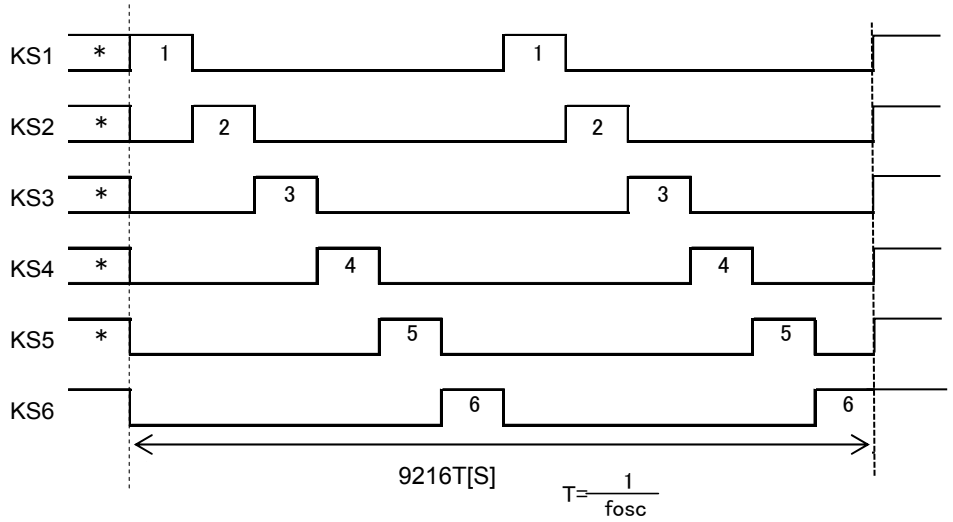


Figure 17. Key Scan Timing(Note22)

(Note22) In sleep mode the high/low state of these pins is determined by the BU0 to BU2 bits in the control data. Key scan output signals are not output from pins that are set “L”.

2. In Normal Mode

The pins KS1 to KS6 are set “H”.

When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.

If a key is pressed for longer than 9840T(s) (Where T=1/fosc) the BU97530KVT-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set “H”.

After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97530KVT-M performs another key scan. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1 KΩ and 10KΩ)

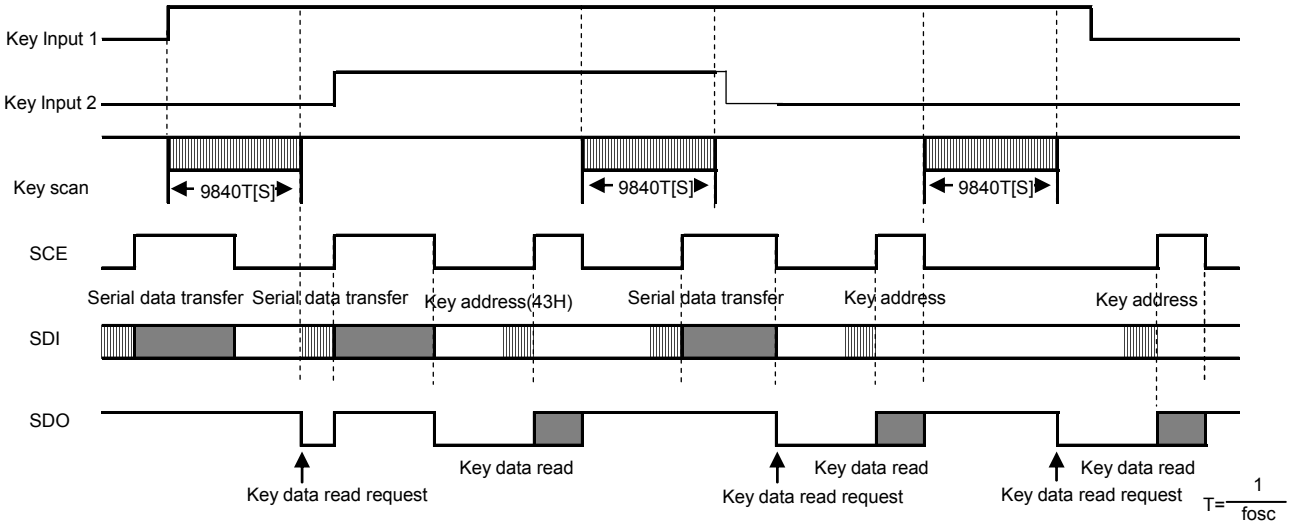
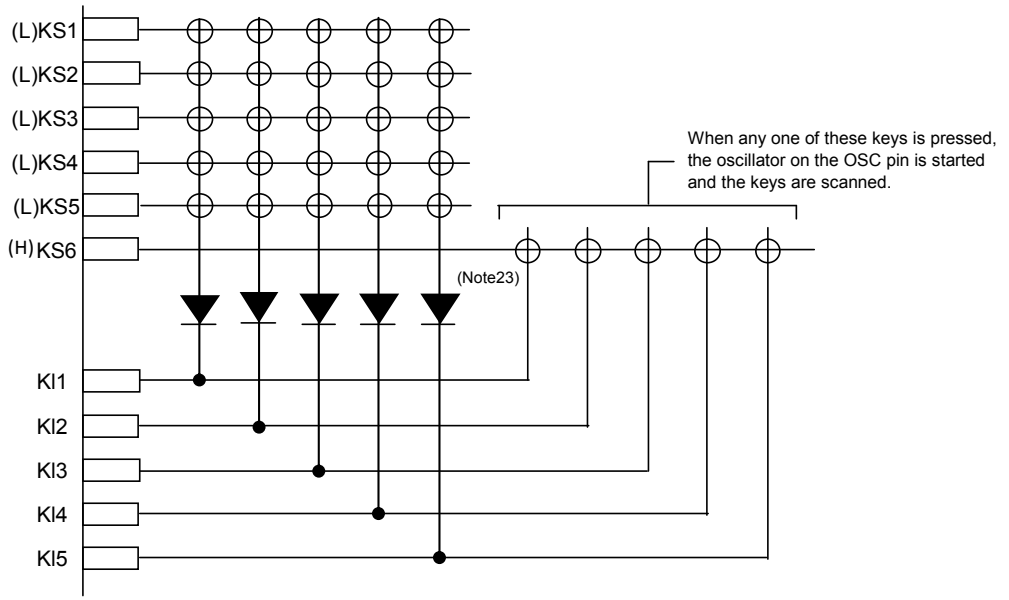


Figure 18. Key Scan Operation in Normal Mode

3. In sleep mode
The pins KS1 to KS6 are set to high or low by the BU0 to BU2 bits in the control data. (See the control data description for details.)
If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
If a key is pressed for longer than 9840T(s)(Where T=1/fosc) the BU97530KVT-M outputs a key data read request (a low level on SDO) to the controller. The controller acknowledges this request and reads the key data. However, if SCE is high during a serial data transfer, SDO will be set high.
After the controller reads the key data, the key data read request is cleared (SDO is set high) and the BU97530KVT-M performs another key scan. However, this does not clear sleep mode. Also note that SDO, being an open-drain output, requires a pull-up resistor (between 1 and 10KΩ).

Sleep mode key scan example

Example: BU0=0, BU1=0, BU2=1 (sleep with only KS6 high)



(Note23)
These diodes are required to reliable recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.

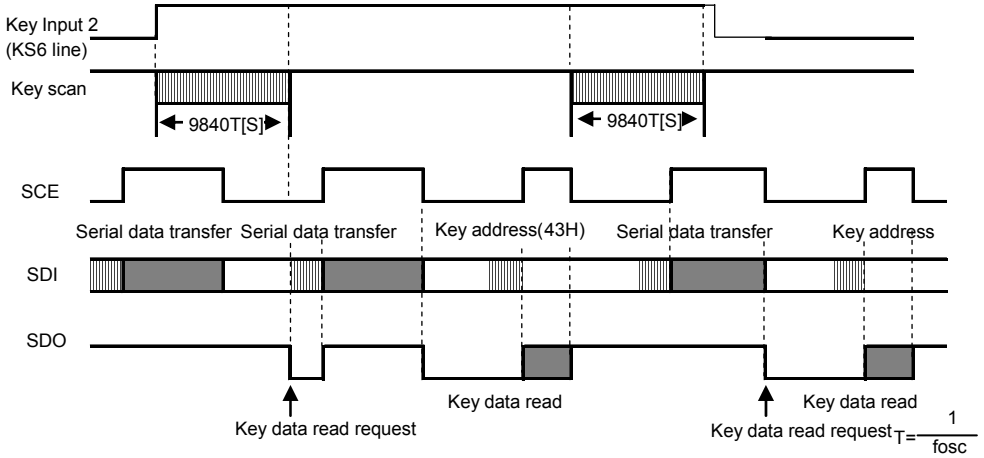


Figure 19. Key Scan Operation in Sleep Mode

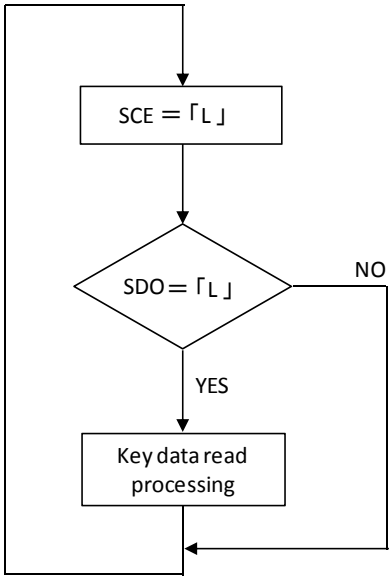
Multiple Key Presses
Although the BU97530KVT-M is capable of key scanning without inserting diodes for dual key presses, triple key presses on the KI1 to KI5 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bit and ignore such data.

Controller Key Data Read Technique

When the controller receives a key data read request from BU97530KVT-M, it performs a key data read acquisition operation using either the Timer Based Key Data Acquisition or the Interrupt Based Key Data Acquisition.

Timer Based Key Data Acquisition Technique

Under the Timer Based Key Data Acquisition Technique, the controller uses a timer to determine the states of the keys (ON or OFF) and read the key data. Please refer to the flowchart below.



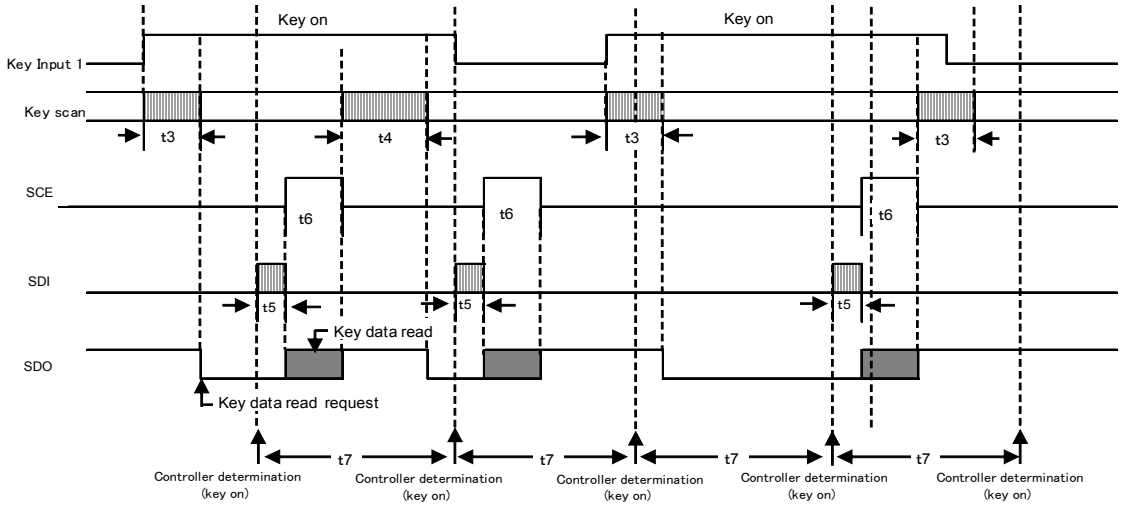
Key data read processing: Refer to “Serial Data Output”

Figure 20. Flowchart

In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low every t7 period without fail. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

The period t7 in this technique must satisfy the following condition.
T7>t4+t5+t6

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

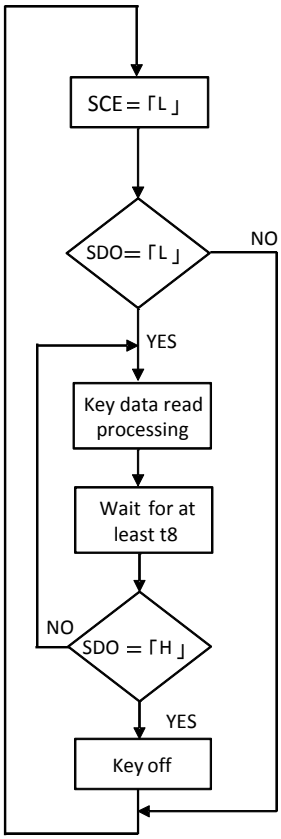


t3: Key scan execution time when the key data agreed for two key scans. (9840T(s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19680T(s)) T = 1 / fosc
t5: Key address (43H) transfer time
t6: Key data read time

Figure 21. Timer based key data read operation

Interrupt Based Key Data Acquisition Technique

Under the Interrupt Based Key Data Acquisition Technique, the controller uses interrupts to determine the state of the keys (ON or OFF) and read the key data. Please refer to the flow chart diagram below.

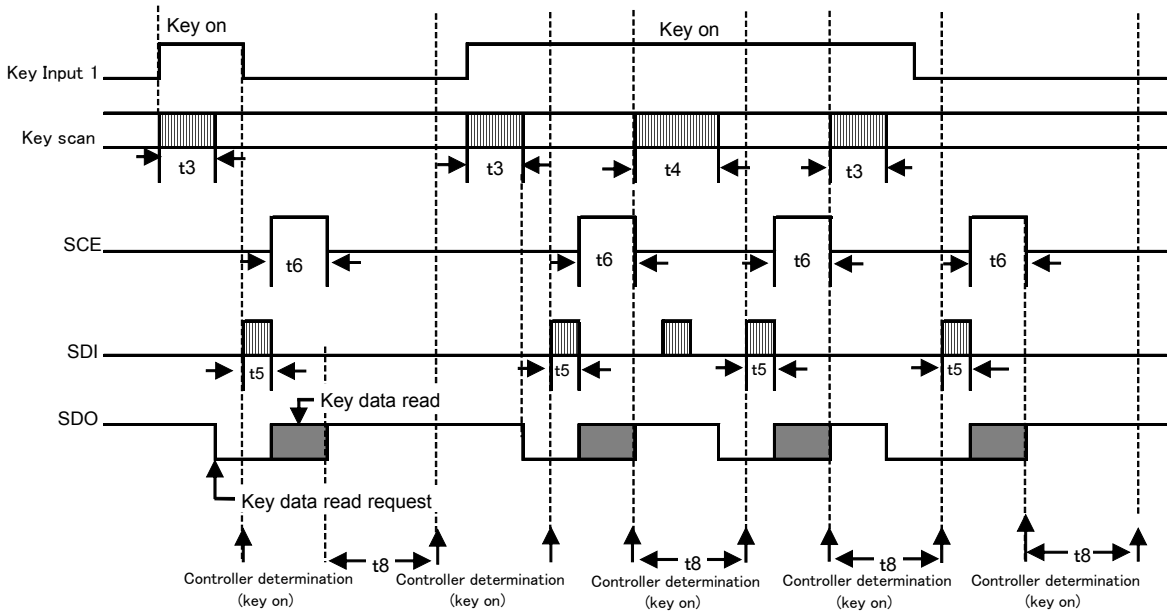


Key data read processing: Refer to “Serial Data Output”

Figure 22. Flowchart

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the SDO state when SCE is low. If SDO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t8 has elapsed by checking the SDO state when SCE is low and reading the key data. The period t8 in this technique must satisfy t8 > t4.

If a key data read operation is executed when SDO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.



t3: Key scan execution time when the key data agreed for two key scans. (9840T(s))
t4: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (19680T(s)) T = 1 / fosc
t5: Key address (43H) transfer time
t6: Key data read time

Figure 23. Interrupt Based Key Data Read Operation

Output Waveform (Line Inversion 1/5 Duty 1/3 Bias Drive Scheme)

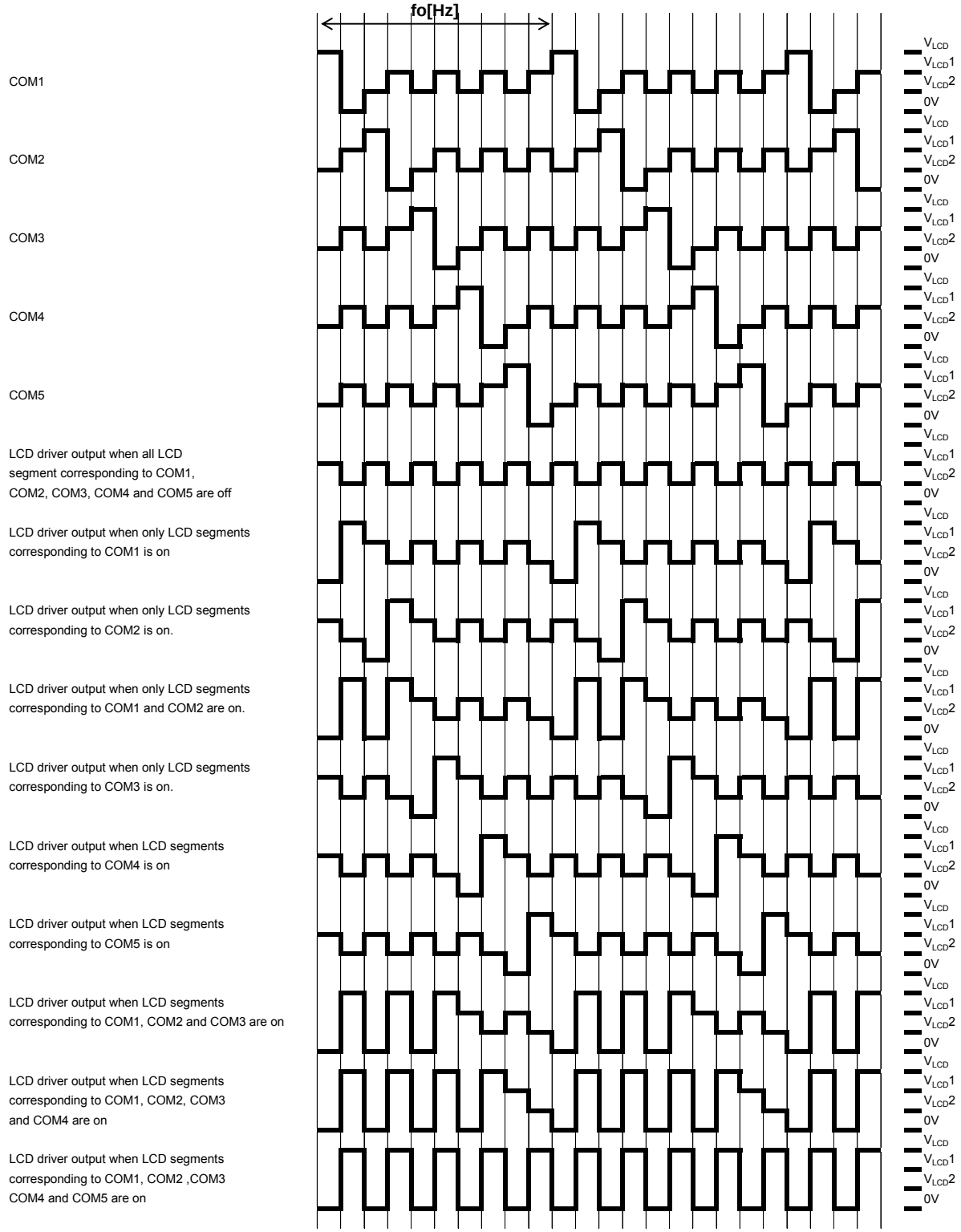


Figure 24. LCD Waveform (Line Inversion, 1/5 DUTY, 1/3 BIAS)

Output Waveform (Line Inversion 1/5 Duty 1/2 Bias Drive Scheme)

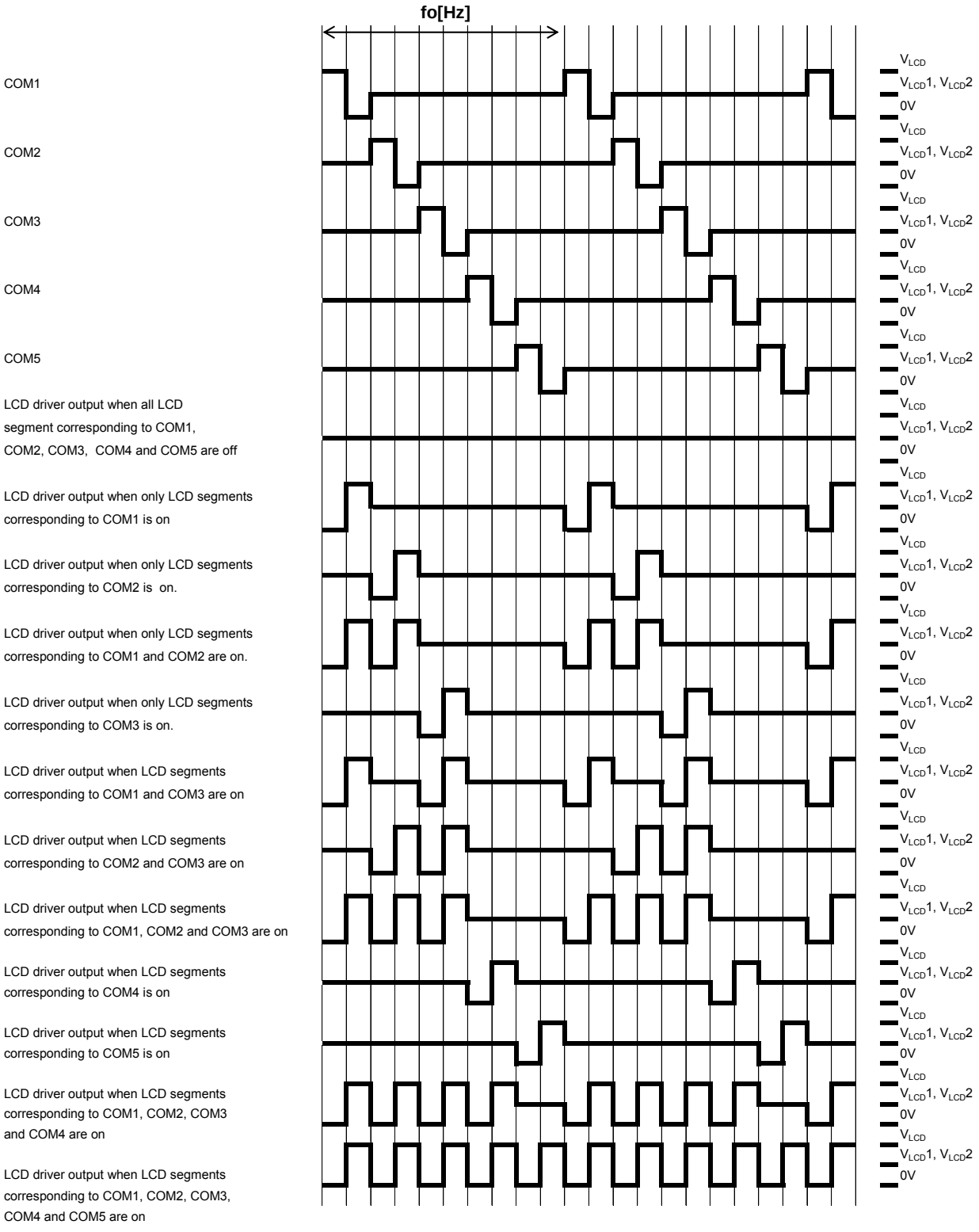


Figure 25. LCD Waveform (Line Inversion, 1/5 DUTY, 1/2 BIAS)

Output Waveform (Line Inversion 1/4 Duty 1/3 Bias Drive Scheme)

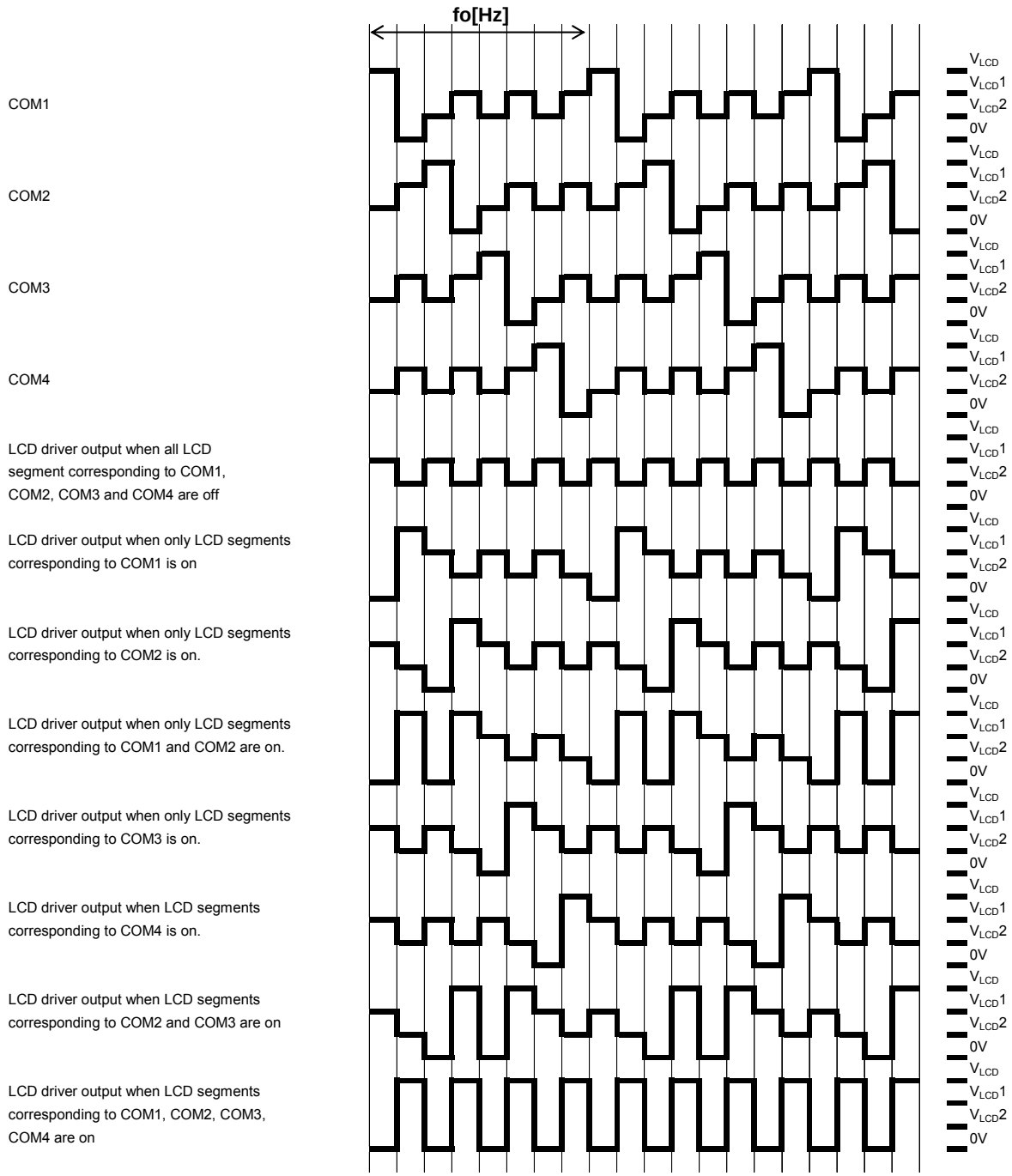


Figure 26. LCD Waveform (Line Inversion, 1/4 DUTY, 1/3 BIAS)

Output Waveform (Line Inversion 1/4 Duty 1/2 Bias Drive Scheme)

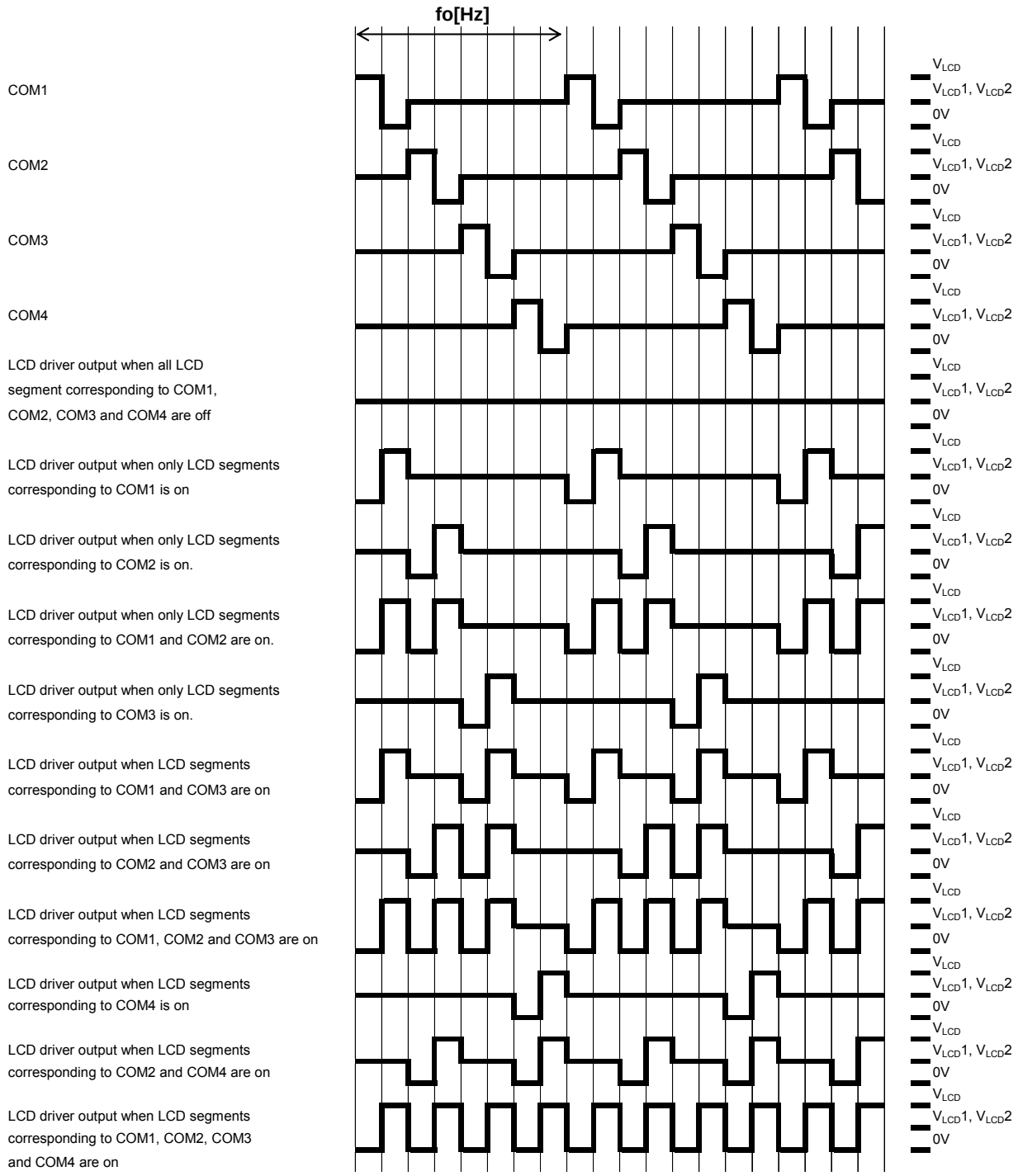


Figure 27. LCD Waveform (Line Inversion, 1/4 DUTY, 1/2 BIAS)

Output Waveform (Line Inversion 1/3 Duty 1/3 Bias Drive Scheme)

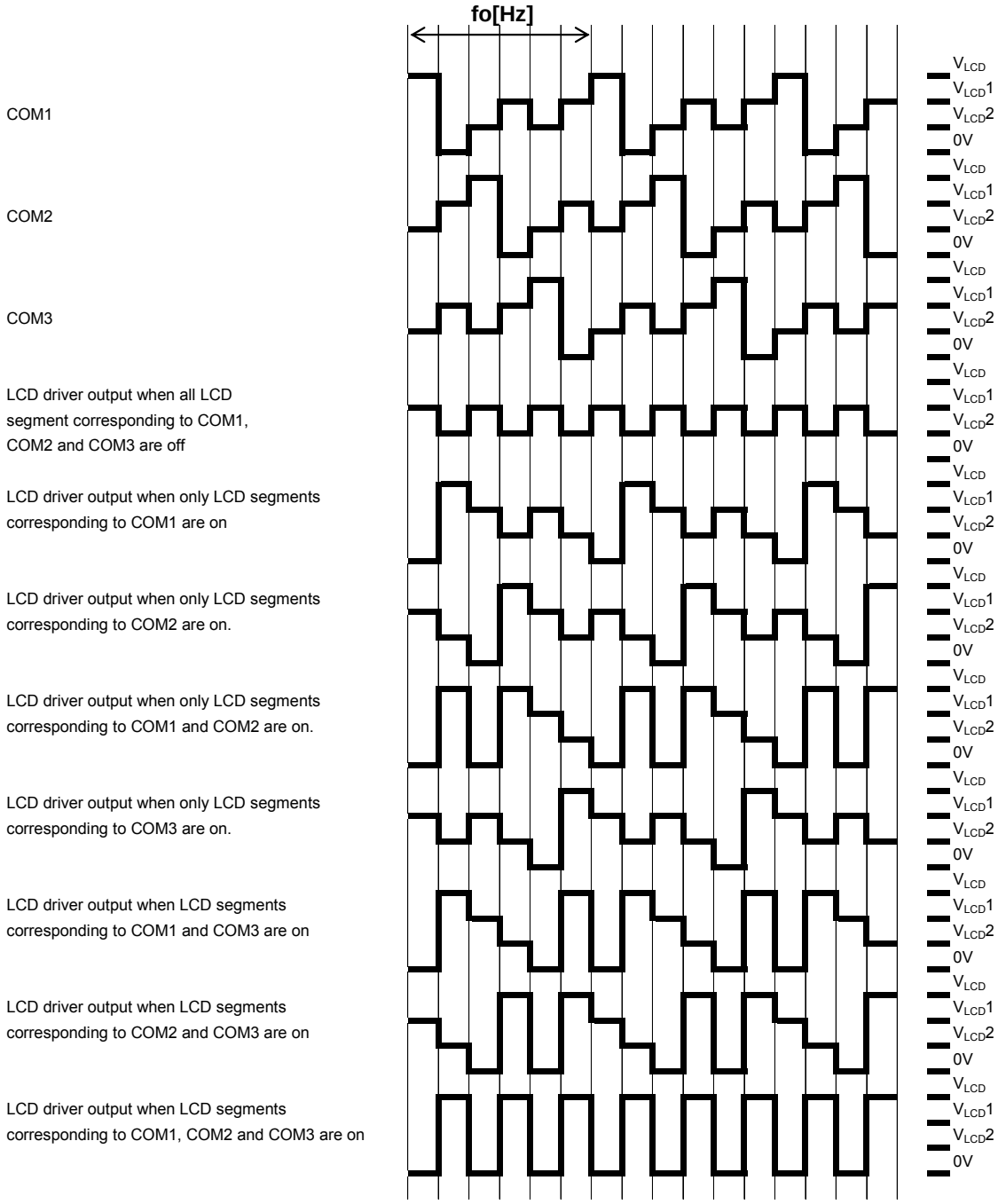


Figure 28. LCD Waveform (Line Inversion, 1/3 DUTY, 1/3 BIAS) (Note24)

(Note24) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Line Inversion 1/3 Duty 1/2 Bias Drive Scheme)

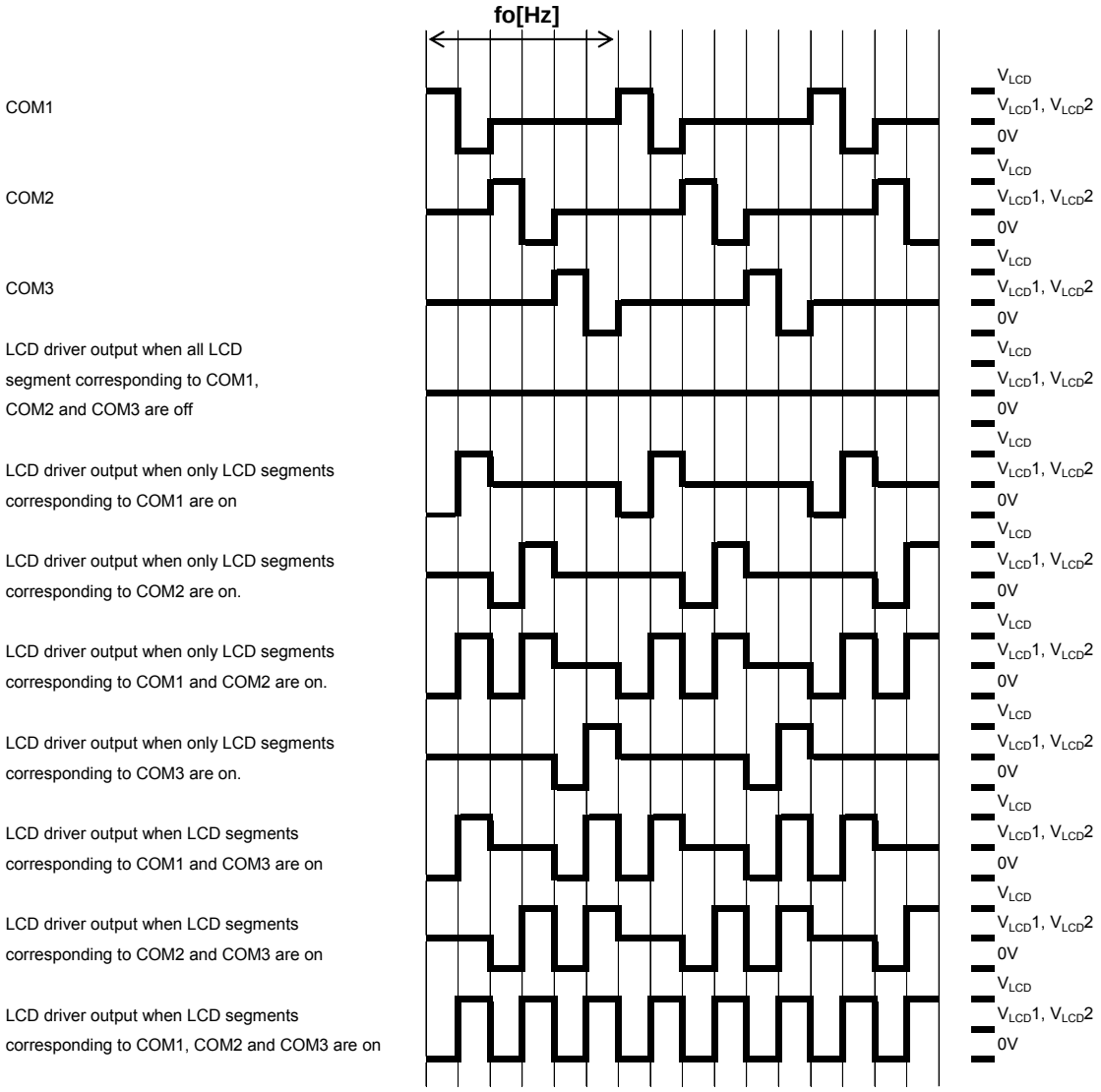


Figure 29. LCD Waveform (Line Inversion, 1/3 DUTY, 1/2BIAS) (Note25)

(Note25) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Line Inversion 1/1 Duty [Static] Drive Scheme)

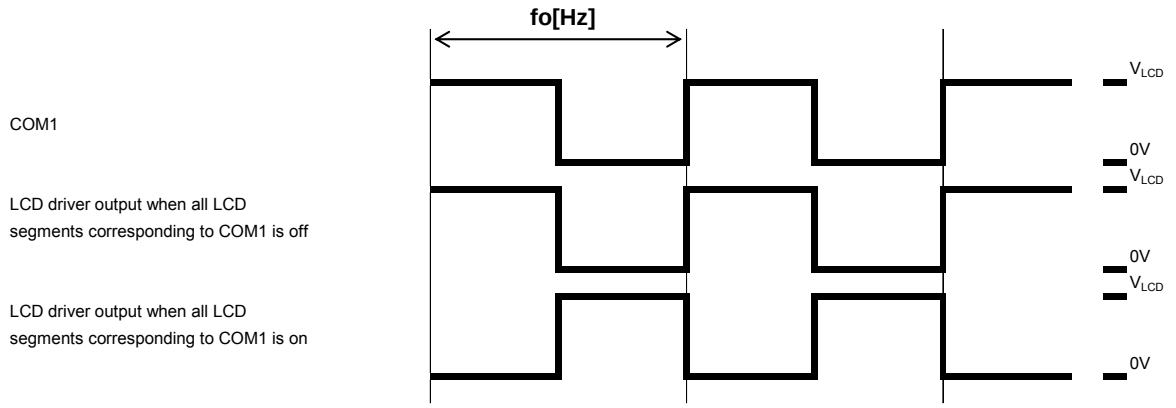


Figure 30. LCD Waveform (Line Inversion, 1/1 DUTY) (Note26)

(Note26) COM2, COM3 and COM4 function are same as COM1 at 1/1 duty.

Output Waveform (Frame Inversion 1/5 Duty 1/3 Bias Drive Scheme)

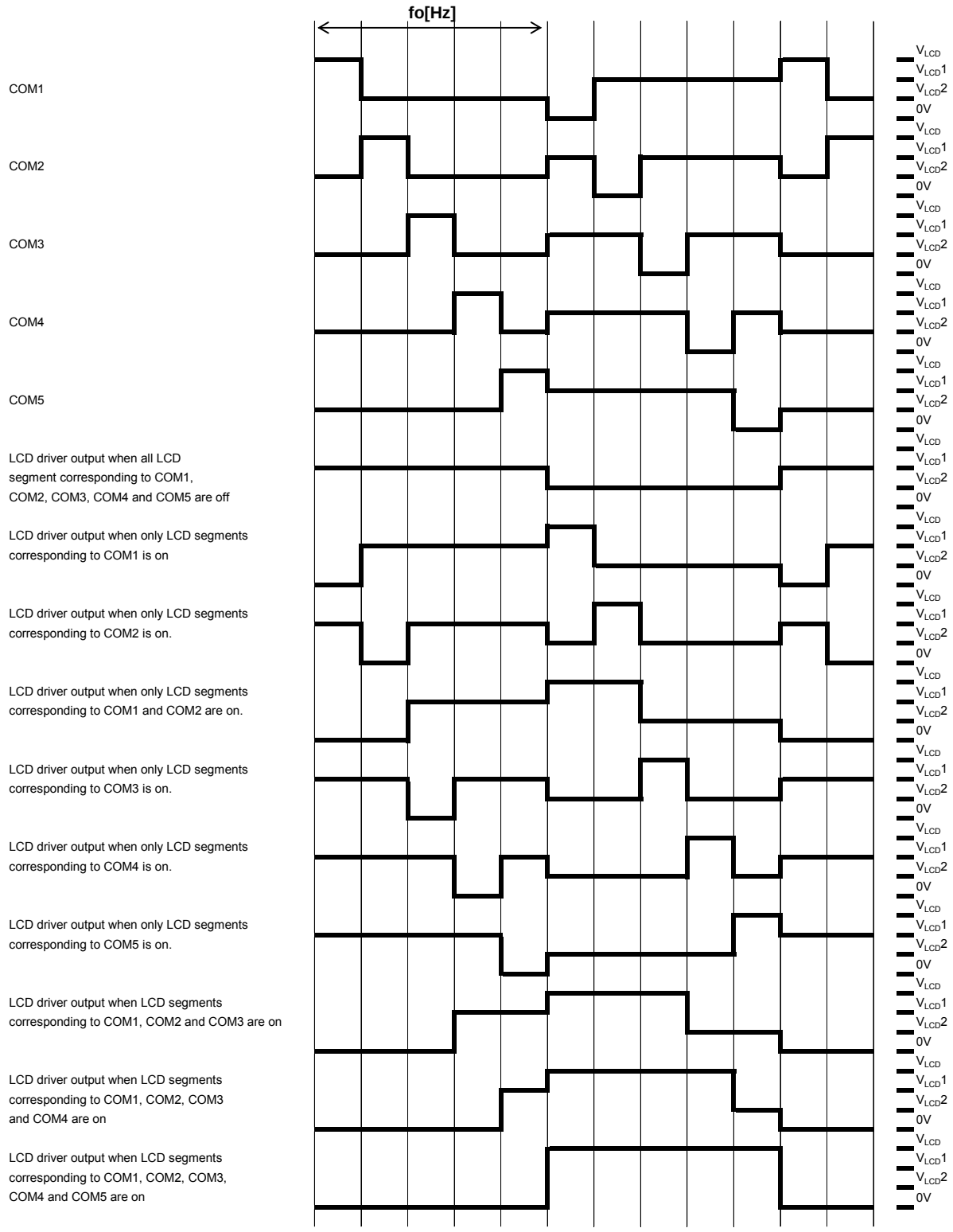


Figure 31. LCD Waveform (Frame Inversion, 1/5 DUTY, 1/3BIAS)

Output Waveform (Frame Inversion 1/5 Duty 1/2 Bias Drive Scheme)

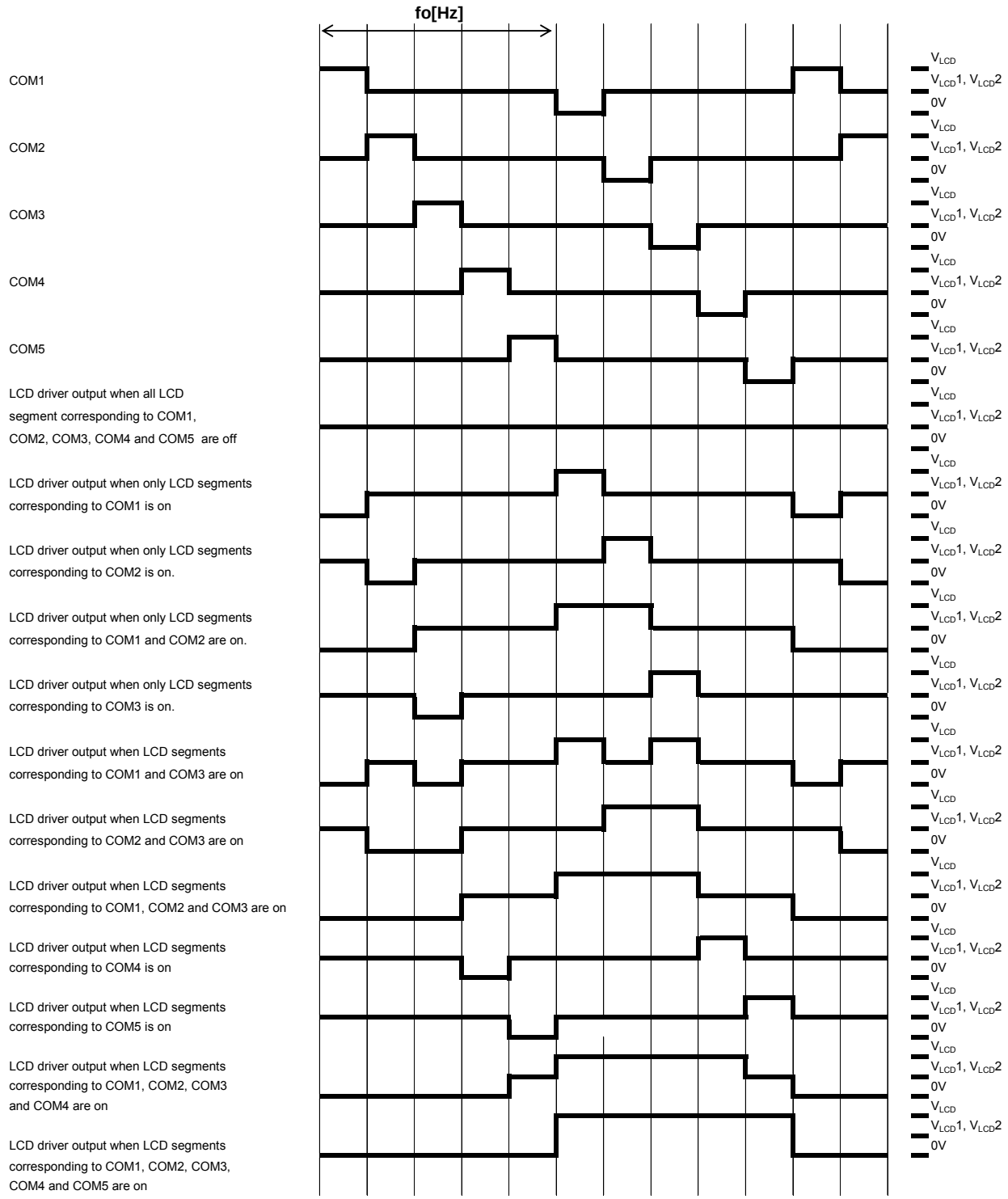


Figure 32. LCD Waveform (Frame Inversion, 1/5 DUTY, 1/2BIAS)

Output Waveform (Frame Inversion 1/4 Duty 1/3 Bias Drive Scheme)

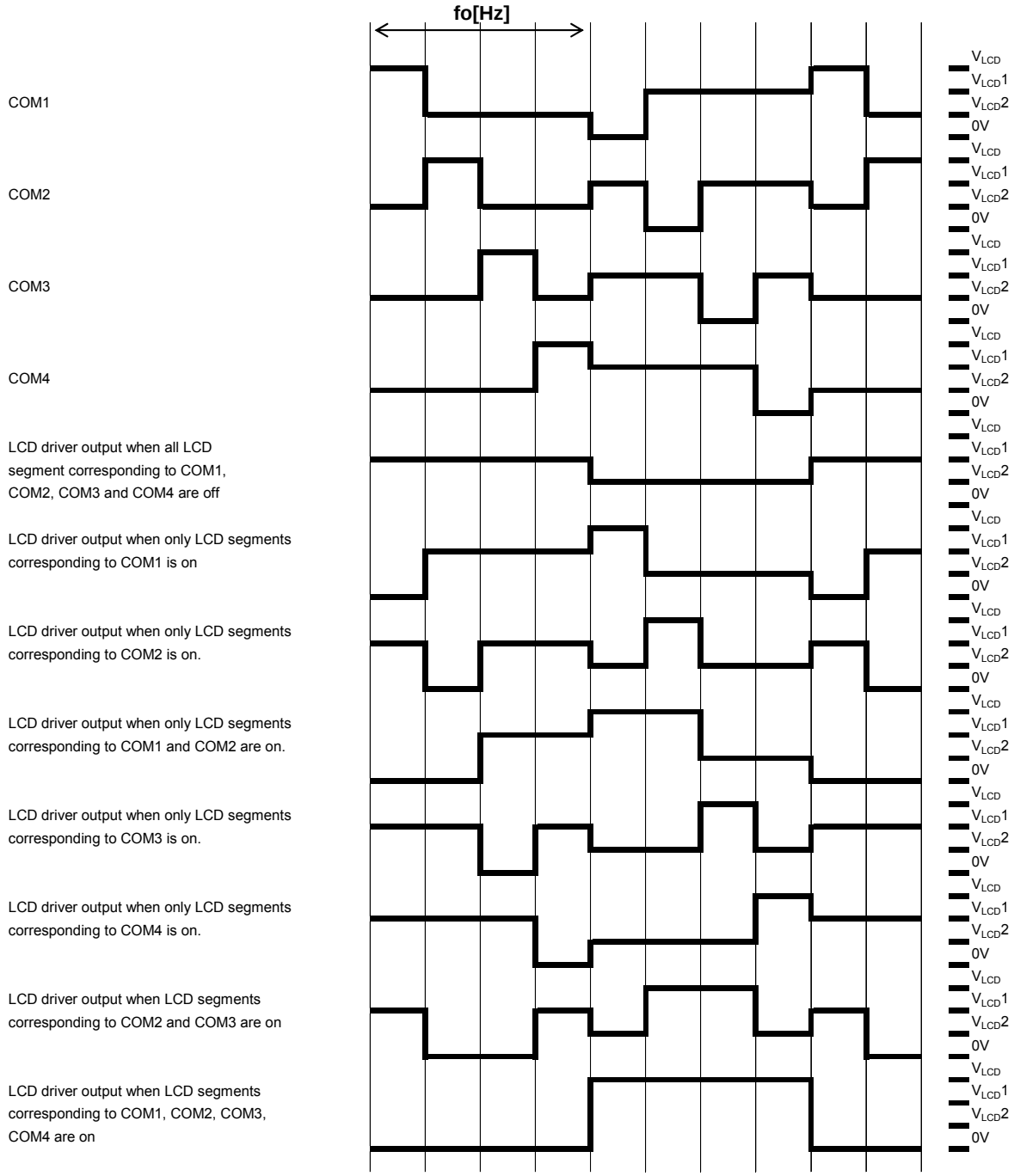


Figure 33. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/3BIAS)

Output Waveform (Frame Inversion 1/4 Duty 1/2 Bias Drive Scheme)

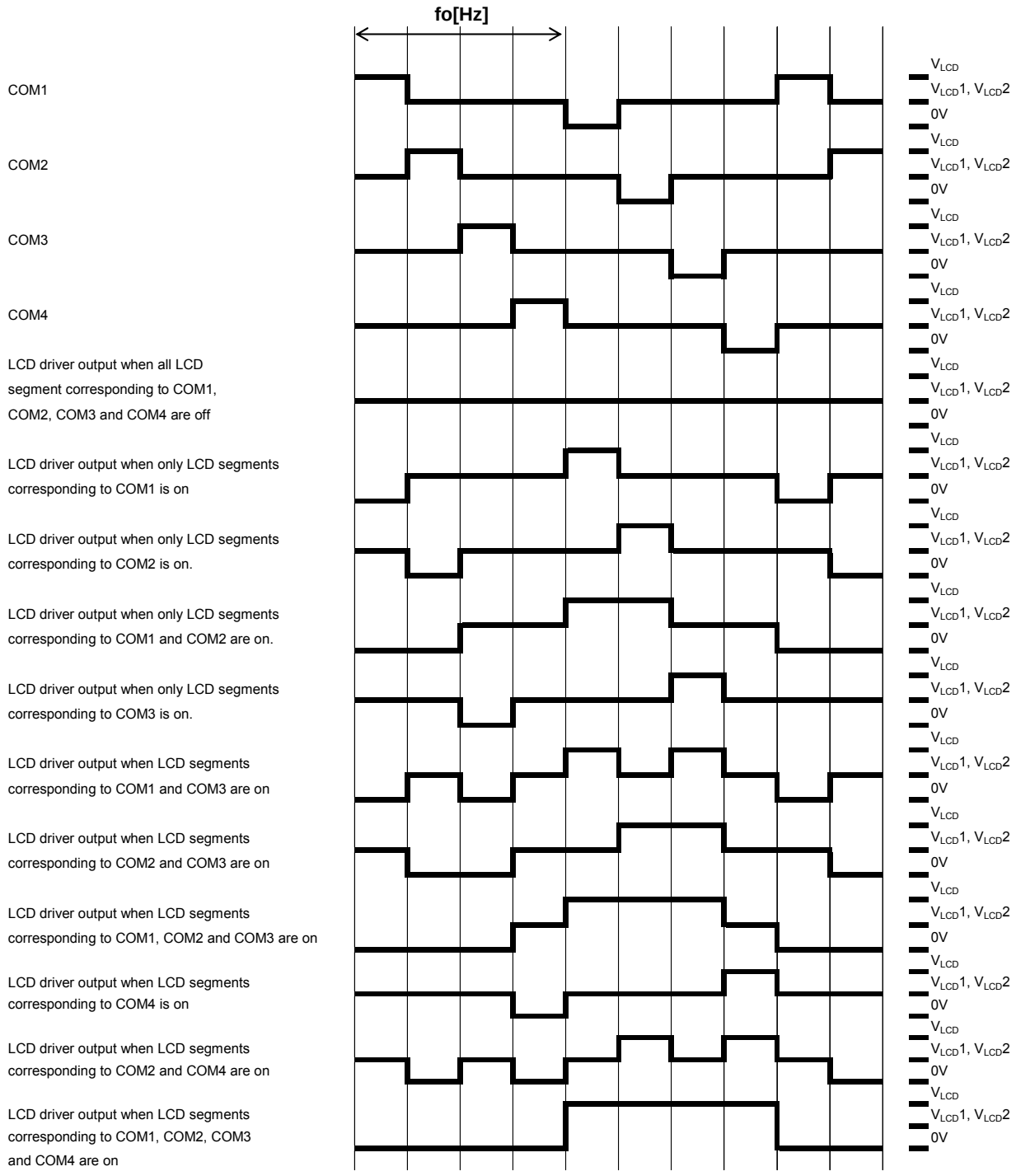


Figure 34. LCD Waveform (Frame Inversion, 1/4 DUTY, 1/2BIAS)

Output Waveform (Frame Inversion 1/3 Duty 1/3 Bias Drive Scheme)

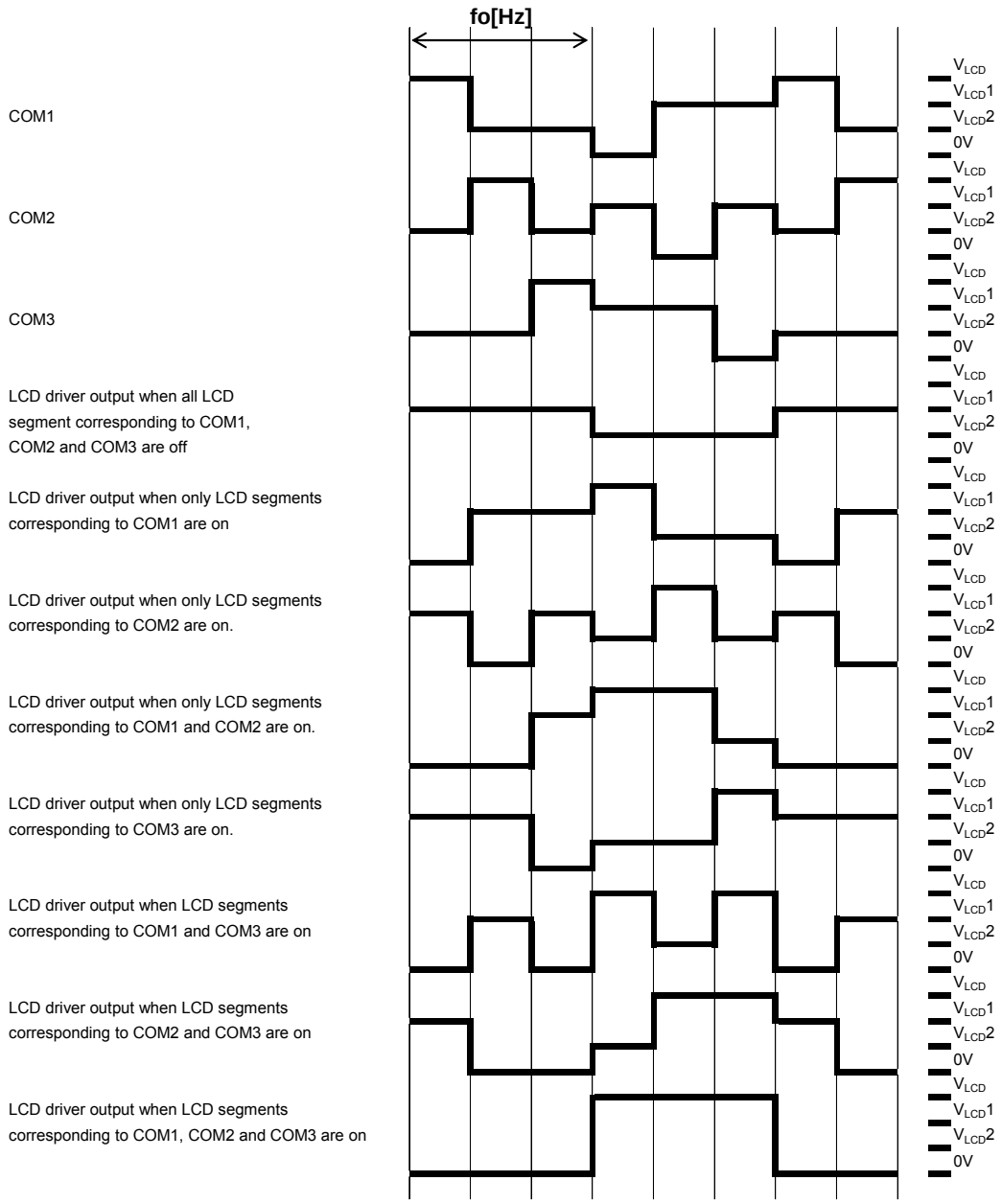


Figure 35. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/3BIAS) (Note27)

(Note27) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Frame Inversion 1/3 Duty 1/2 Bias Drive Scheme)

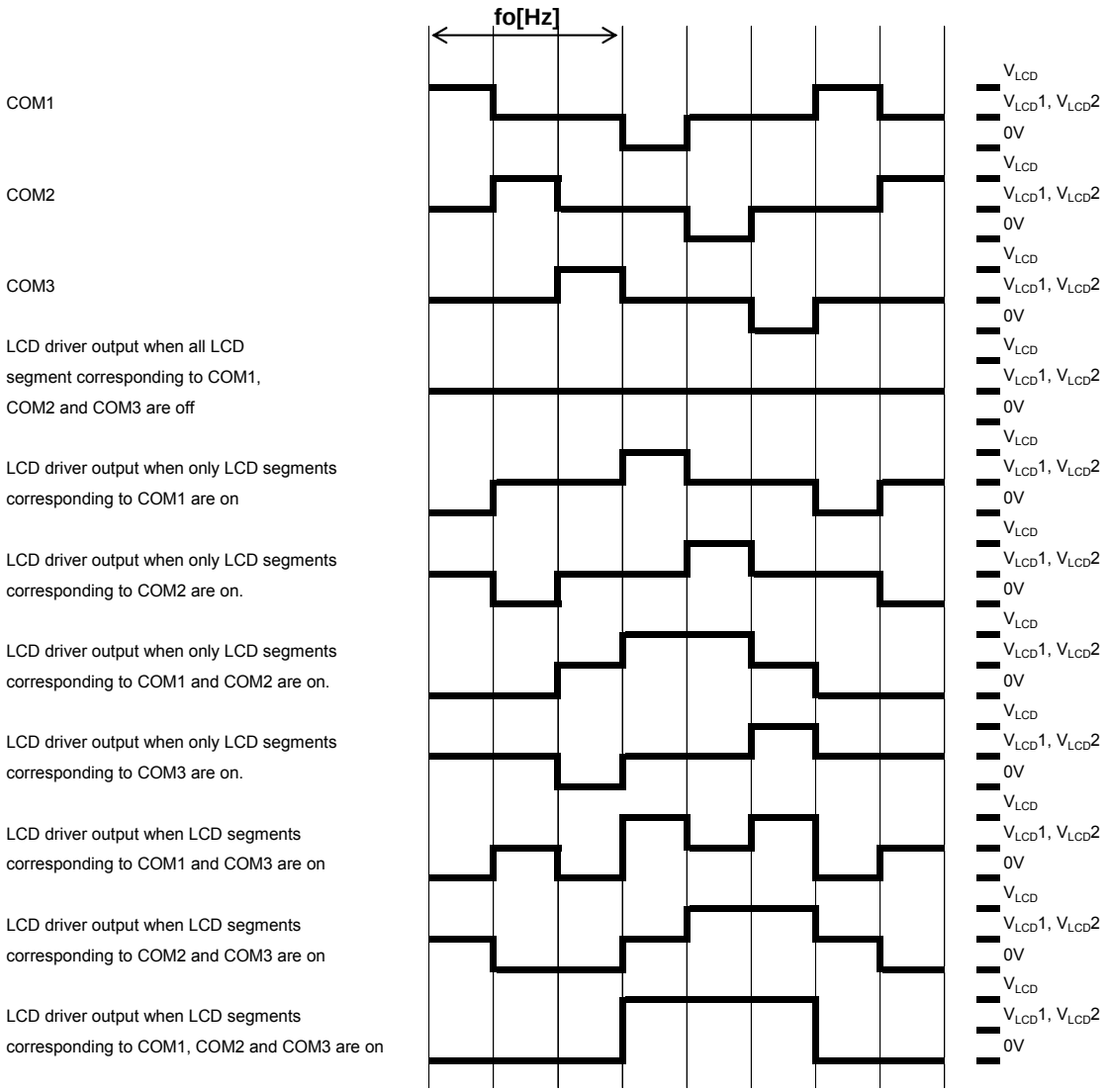


Figure 36. LCD Waveform (Frame Inversion, 1/3 DUTY, 1/2 BIAS) (Note28)

(Note28) COM4 function is same as COM1 at 1/3 duty.

Output Waveform (Frame Inversion 1/1 Duty [Static] Drive Scheme)

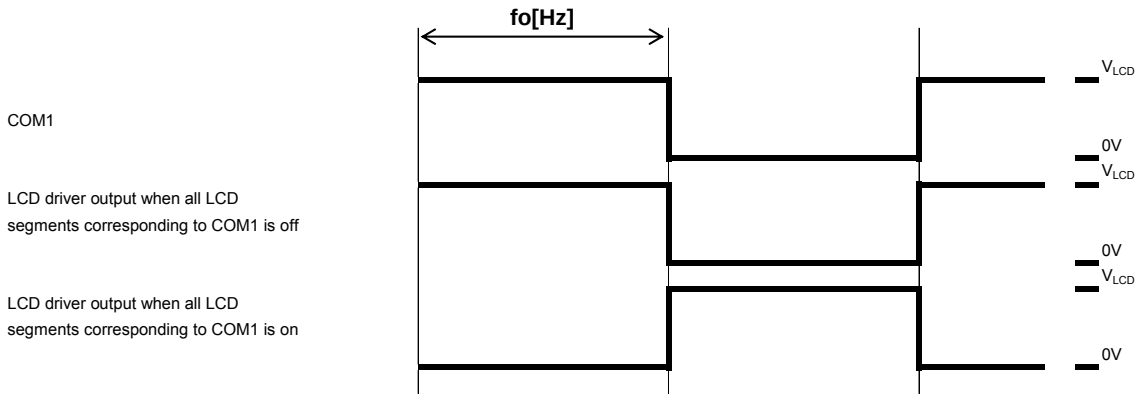


Figure 37. LCD Waveform (Frame Inversion, 1/1 DUTY) (Note29)

(Note29) COM2, COM3 and COM4 function are same as COM1 at 1/1 duty.

Oscillation Stabilization Time

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.

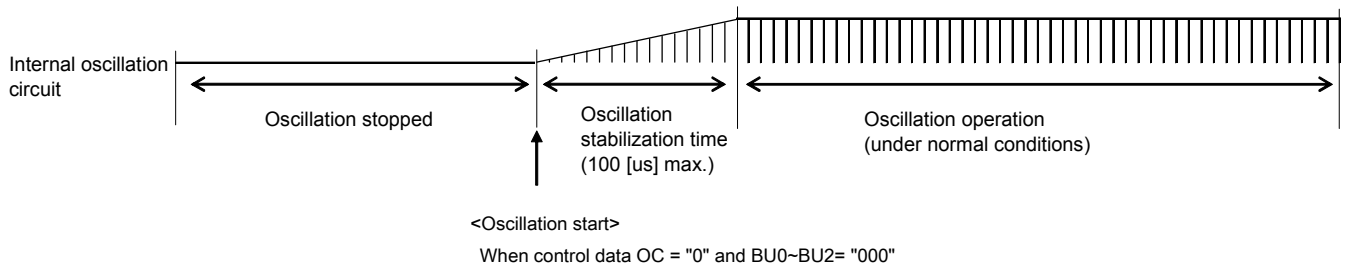


Figure 38. Oscillation Stabilization Time

Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal that resets the system when power is applied for the first time and when the power supply voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (VDET = 1.8V typ.). To ensure that this reset function works properly, it is recommended that a capacitor be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

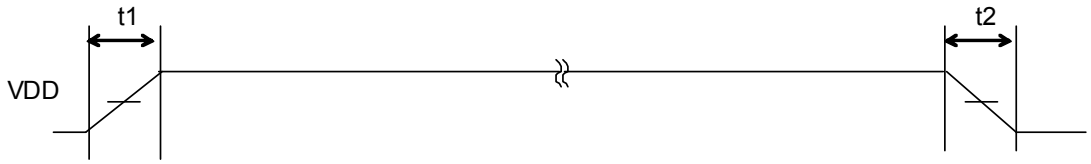


Figure 39. VDET Detection Timing

Power supply voltage VDD rise time: t1 > 1ms
Power supply voltage VDD fall time: t2 > 1ms

RESET CONDITION

When BU97530KVT-M is initialized, the internal status after power supply has been reset as the following table.

Instruction	At Reset Condition
Key Scan mode	[KM0,KM1,KM2]=[1,1,1]:Keyscan no use
S1/P1/G1 to S9/P9/G9 pin	[P0,P1,P2,P3]=[0,0,0,0]:all segment output
Inversion mode	FL=0:Line Inversion
LCD bias	DR=0:1/3 bias
LCD duty	[DT0,DT1]=[1,0]:1/4 duty
DISPLAY frequency	[FC0,FC1,FC2,FC3]=[0,0,0]:fosc/12288
Display clock mode	OC=0:Internal oscillator
LCD display	SC=1:OFF
Power mode	[BU0, BU1, BU2]=[1,1,1]:Power saving mode
PWM/GPO output	PGx=0:PWM output(x=1～9)
PWM frequency	[PF0,PF1,PF2,PF3]=[0,0,0,0]: fosc /4096
PWM duty	[Wn1～Wn8]=[0,0,0,0,0,0,0,0]:0/256)xTp (n=1～9,Tp=1/fp)
Display Contrast setting	[CT0,CT1,CT2,CT3]=[0,0,0,0]:VLCD Level is 1.00*VDD

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Data transmission

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

Ordering Information

B U 9 7 5 3 0 K V T - ME2

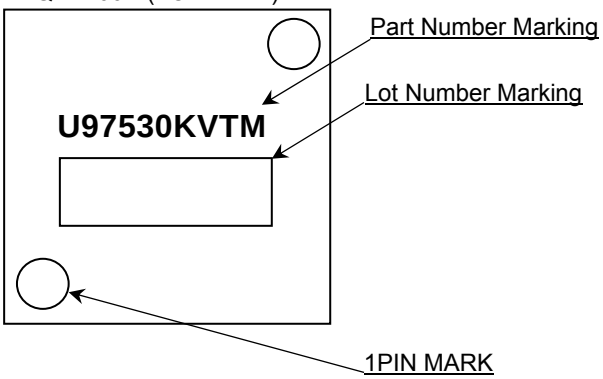
Part Number

Package
KVT : TQFP100V

Product Rank
M: for Automotive
Packaging Specification
E2: Embossed tape and reel
(TQFP100V)
None: Tray (TQFP100V)

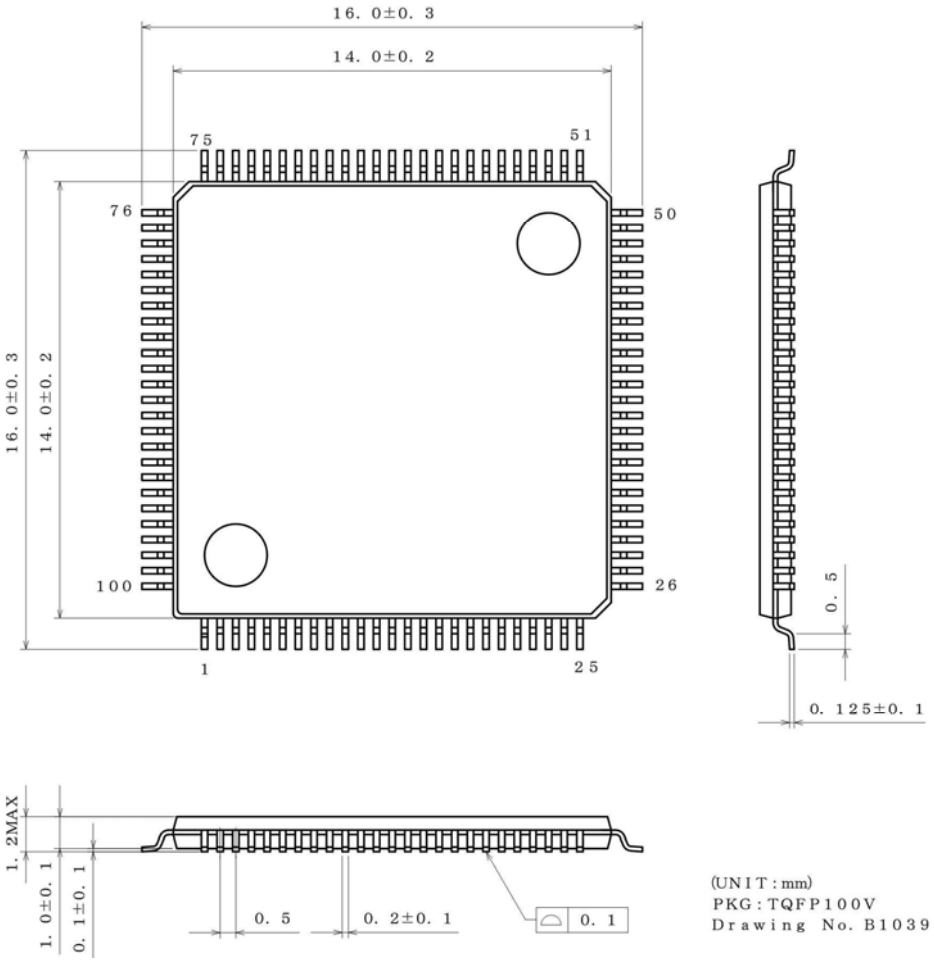
Marking Diagram

TQFP100V (TOP VIEW)



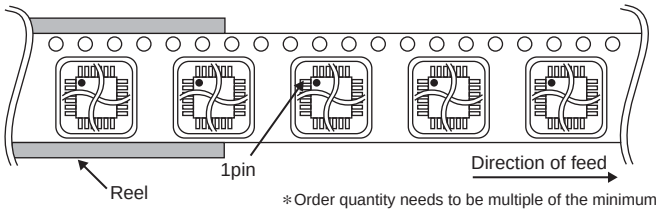
Physical Dimension, Tape and Reel Information

Package Name	TQFP100V



<Tape and Reel information>

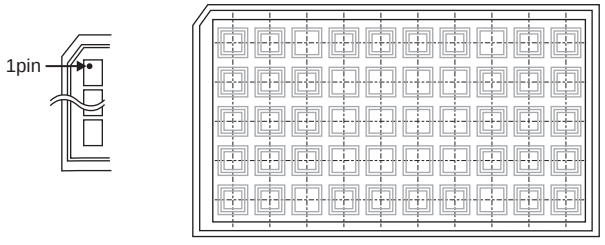
Tape	Embossed carrier tape (with dry pack)
Quantity	500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	500pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

Version / Revision History

Version	date	description
001	16. Mar. 2014	New Release
002	21. Oct. 2014	Page.8-15 Modify 3-SPI Data Transfer Format Wn0 delete(fix to 0) Page.40,41,47,48 Delete COM4 description Page.51 Delete Wn0 description in RESET CONDITION Table
003	2. Mar. 2015	Modify Note number. Page.1 Add Note on AEC-Q100 Qualified. Page.4 Add External Clock Duty. Page.5 Modify Data Setup Time Min limit. Page.5 Modify Data Hold Time Min limit. Page.5 Modify SCE Wait Time Min limit. Page.5 Modify SCE Setup Time Min limit. Page.5 Modify SCE Hold Time Min limit. Page.5 Modify High-level Clock Pulse Width Min limit. Page.5 Modify Low-level Clock Pulse Width (Write) Min limit. Page.5 Add Clock Cycle Time. Page.5 Add Low-Level Clock Pulse Width (Read). Page.5 Add RPU and CL explanation. Page.5 Add SDO signal, tccyc and tclwr on Figure5 Serial Interface Timing. Page.5 Modify tclww from tclw on Figure5 Serial Interface Timing. Page.5 Modify reference level of tchw to VIH1,VIH2 from 50% on Figure5 Serial Interface Timing. Page.5 Modify reference level of tclww to VIL1 from 50% on Figure5 Serial Interface Timing. Page.5 Delete tcp on Figure5 Serial Interface Timing (1.When SCL is stopped at the low level) . Page.5 Delete tcs on Figure5 Serial Interface Timing (2.When SCL is stopped at the high level). Page.54,55 Add packing specification for tray.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BU97530KVT-M - Web Page

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Distribution Inventory

Part Number	BU97530KVT-M
Package	TQFP100V
Unit Quantity	500
Minimum Package Quantity	500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes