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March 2015

FDD5614P

60V P-Channel PowerTrench® MOSFET

General Description

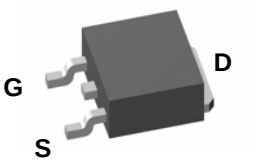
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

Applications

- DC/DC converter
- Power management
- Load switch

Features

- –15 A, –60 V. $R_{DS(ON)}$ = 100 mΩ @ V_{GS} = –10 V
  $R_{DS(ON)}$ = 130 mΩ @ V_{GS} = –4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



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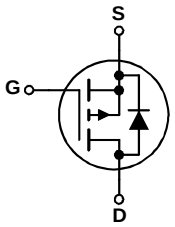


Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current – Continuous	(Note 3)	–15	A
	– Pulsed	(Note 1a)	–45	
P_D	Power Dissipation for Single Operation	(Note 1)	42	W
		(Note 1a)	3.8	
		(Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	3.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5614P	FDD5614P	13”	16mm	2500 units

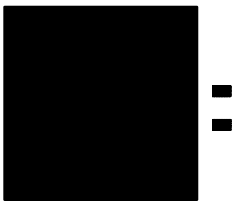
Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = –30 V, I_D = –4.5 A			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				–4.5	A
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		–49		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –48 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –10 V, I_D = –4.5 A V_{GS} = –4.5 V, I_D = –3.9 A V_{GS} = –10 V, I_D = –4.5 A, T_J=125°C		76 99 137	100 130 185	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = –10 V, V_{DS} = –5 V	–20			A
g_{FS}	Forward Transconductance	V_{DS} = –5 V, I_D = –3 A		8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = –30 V, V_{GS} = 0 V, f = 1.0 MHz		759		pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = –30 V, I_D = –1 A, V_{GS} = –10 V, R_{GEN} = 6 Ω		7	14	ns
t_r	Turn–On Rise Time			10	20	ns
$t_{d(off)}$	Turn–Off Delay Time			19	34	ns
t_f	Turn–Off Fall Time			12	22	ns
Q_g	Total Gate Charge	V_{DS} = –30V, I_D = –4.5 A, V_{GS} = –10 V		15	24	nC
Q_{gs}	Gate–Source Charge			2.5		nC
Q_{gd}	Gate–Drain Charge			3.0		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–3.2	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –3.2 A (Note 2)		–0.8	–1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$ = 40°C/W when mounted on a $1in^2$ pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$
where P_D is maximum power dissipation at T_C = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and V_{GS} = 10V. Package current limitation is 21A

Typical Characteristics

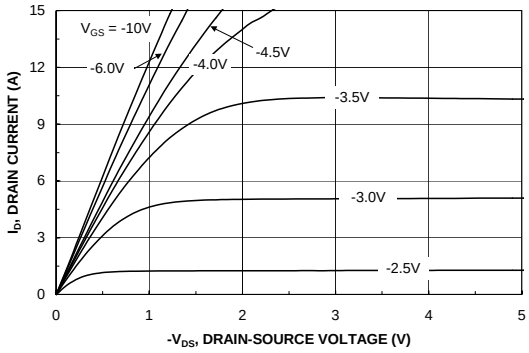


Figure 1. On-Region Characteristics.

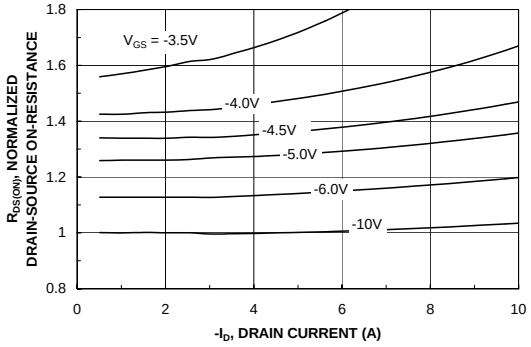


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

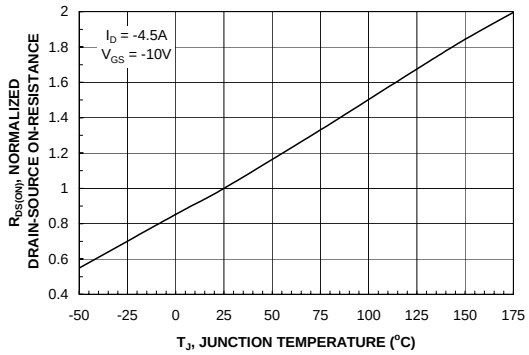


Figure 3. On-Resistance Variation with Temperature.

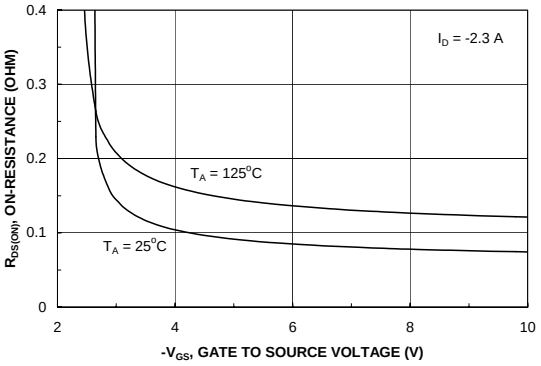


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

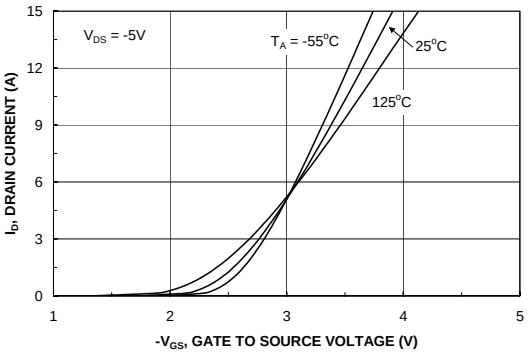


Figure 5. Transfer Characteristics.

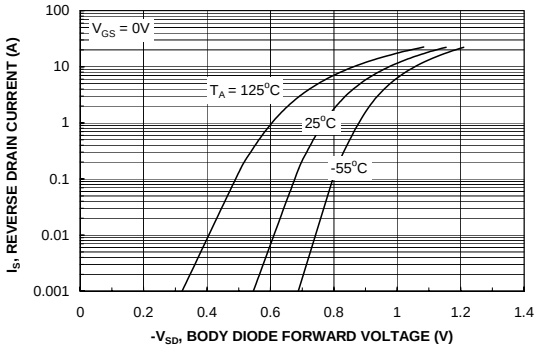


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

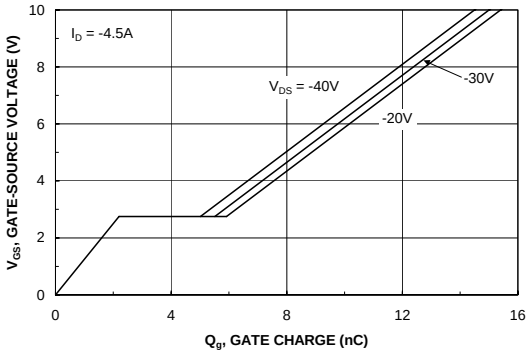


Figure 7. Gate Charge Characteristics.

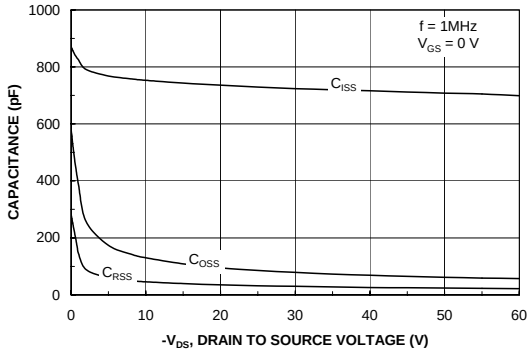


Figure 8. Capacitance Characteristics.

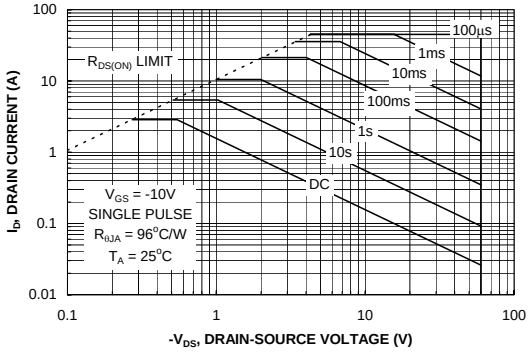


Figure 9. Maximum Safe Operating Area.

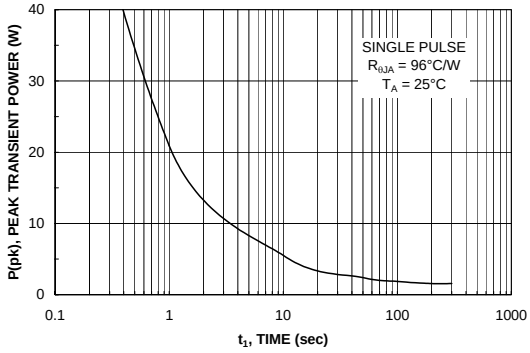


Figure 10. Single Pulse Maximum Power Dissipation.

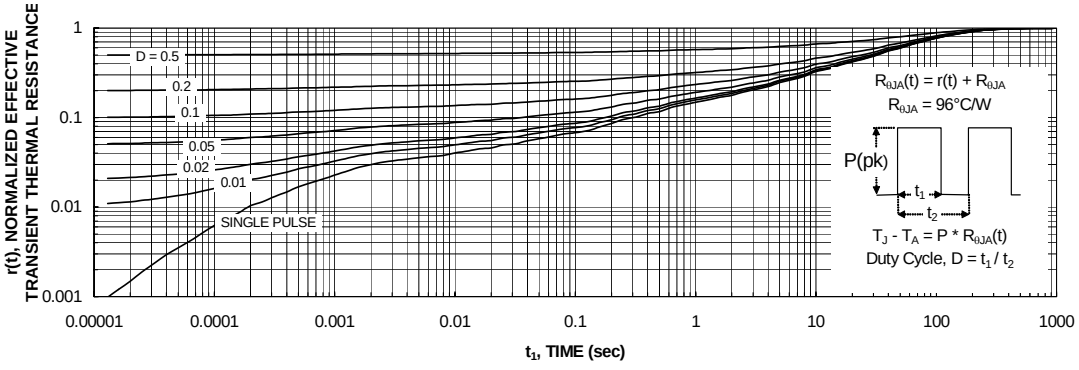
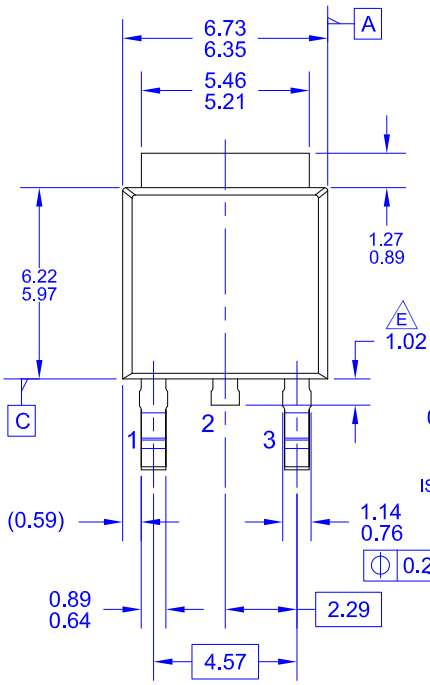
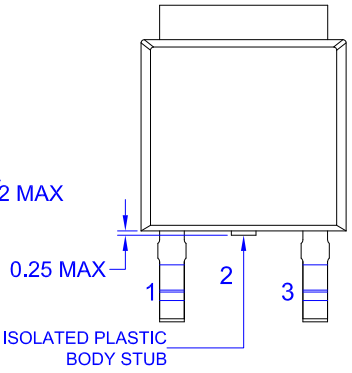


Figure 11. Transient Thermal Response Curve.

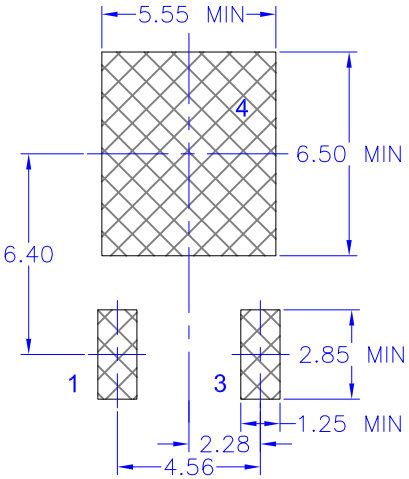
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



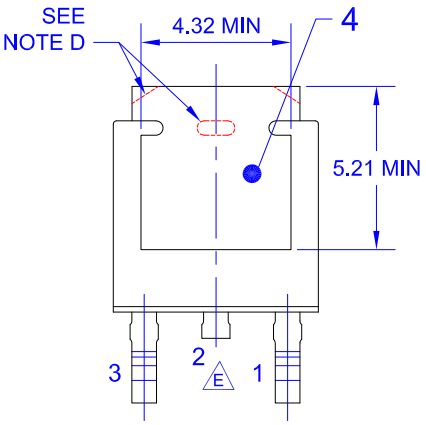
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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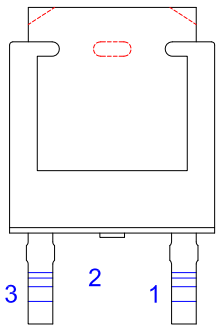

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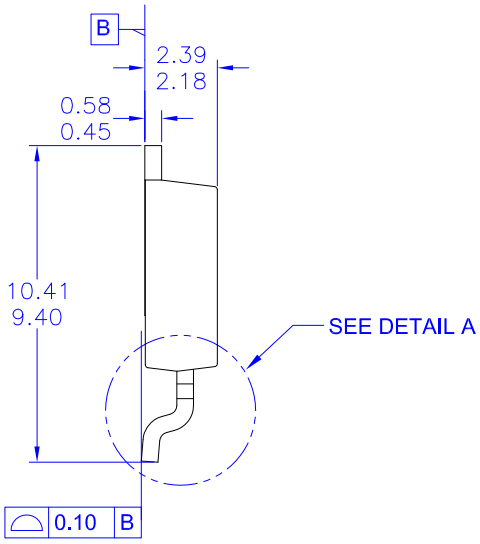

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C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
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E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
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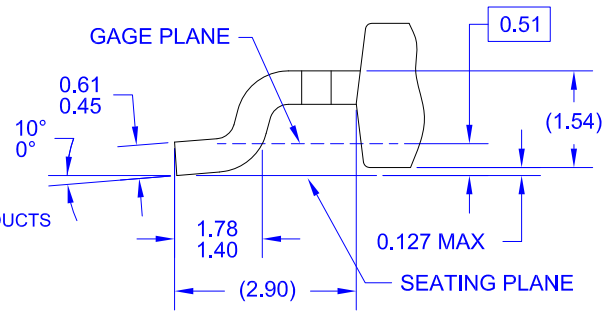

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