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January 1993
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74LVX4245
8-Bit Dual Supply Translating Transceiver with 3-STATE Outputs

General Description

The LVX4245 is a dual-supply, 8-bit translating transceiver that is designed to interface between a 5V bus and a 3V bus in a mixed 3V/5V supply environment. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance condition. The A Port interfaces with the 5V bus; the B Port interfaces with the 3V bus.

The LVX4245 is suitable for mixed voltage applications such as laptop computers using 3.3V CPU's and 5V LCD displays.

Features

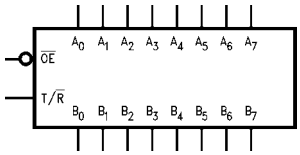
- Bidirectional interface between 5V and 3V buses
- Control inputs compatible with TTL level
- 5V data flow at A Port and 3V data flow at B Port
- Outputs source/sink 24 mA at 5V bus; 12 mA at 3V bus
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Implements patented EMI reduction circuitry
- Functionally compatible with the 74 series 245

Ordering Code:

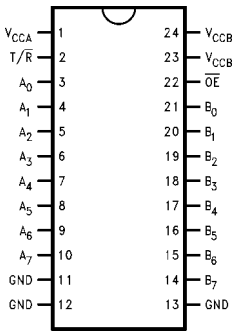
Order Number	Package Number	Package Description
74LVX4245WM	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX4245QSC	MQA24	24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
74LVX4245MTC	MTC24	24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

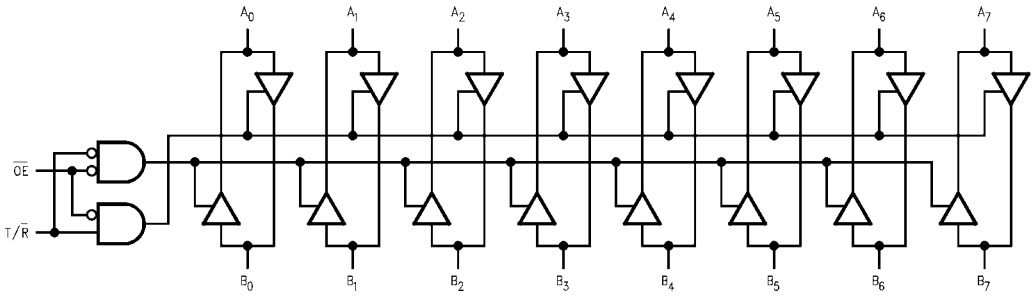
Pin Names	Description
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A Inputs or 3-STATE Outputs
B_0–B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CCA}, V_{CCB})	−0.5V to +7.0V
DC Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	−0.5V to V_{CCA} + 0.5V
DC Input/Output Voltage ($V_{I/O}$)	
@ A_n	−0.5V to V_{CCA} + 0.5V
@B_n	−0.5V to V_{CCB} + 0.5V
DC Input Diode Current (I_{IN})	
@ $\overline{OE}$, T/$\overline{R}$	±20 mA
DC Output Diode Current (I_{OK})	±50 mA
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
and Max Current @ I_{CCA}	±200 mA
@ I_{CCB}	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA

Recommended Operating Conditions (Note 2)

Supply Voltage	
V_{CCA}	4.5V to 5.5V
V_{CCB}	2.7V to 3.6V
Input Voltage (V_I) @ $\overline{OE}$, T/$\overline{R}$	0V to V_{CCA}
Input/Output Voltage ($V_{I/O}$)	
@ A_n	0V to V_{CCA}
@ B_n	0V to V_{CCB}
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (Δt/ΔV)	8 ns/V
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.0V, 4.5V, 5.5V	

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: Unused inputs must he held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter		V_{CCA} (V)	V_{CCB} (V)	T_A +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IHA}	Minimum HIGH Level Input Voltage	A_n, T/$\overline{R}$, $\overline{OE}$	5.5	3.3		2.0	2.0	V	V_{OUT} ≤ 0.1V or ≥ V_{CC} − 0.1V
			4.5	3.3		2.0	2.0		
V_{IHB}		B_n	5.0	3.6		2.0	2.0		
			5.0	2.7		2.0	2.0		
V_{ILA}	Maximum LOW Level Input Voltage	A_n, T/$\overline{R}$, $\overline{OE}$	5.5	3.3		0.8	0.8	V	V_{OUT} ≤ 0.1V or ≥ V_{CC} −0.1V
			4.5	3.3		0.8	0.8		
V_{ILB}		B_n	5.0	2.7		0.8	0.8		
			5.0	3.6		0.8	0.8		
V_{OHA}	Minimum HIGH Level Output Voltage		4.5	3.0	4.5	4.4	4.4	V	I_{OUT} = −100 µA
			4.5	3.0	4.25	3.86	3.76		I_{OH} = −24 mA
V_{OHB}			4.5	3.0	2.99	2.9	2.9	V	I_{OUT} = −100 µA
			4.5	3.0	2.8	2.4	2.4		I_{OH} = −12 mA
			4.5	2.7	2.5	2.4	2.4		I_{OL} = −8 mA
V_{OLA}	Maximum LOW Level Output Voltage		4.5	3.0	0.002	0.1	0.1	V	I_{OUT} =100 µA
			4.5	3.0	0.18	0.36	0.44		I_{OL} = 24 mA
V_{OLB}			4.5	3.0	0.002	0.1	0.1	V	I_{OUT} = 100 µA
			4.5	3.0	0.1	0.31	0.4		I_{OL} = 12 mA
			4.5	2.7	0.1	0.31	0.4		I_{OL} = 8 mA
I_{IN}	Maximum Input Leakage Current @ $\overline{OE}$, T/$\overline{R}$		5.5	3.6		±0.1	±1.0	µA	V_I = V_{CCA}, GND
I_{OZA}	Maximum 3-STATE Output Leakage @ A_n		5.5	3.6		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} $\overline{OE}$ = V_{CCA} V_O = V_{CCA}, GND
I_{OZB}	Maximum 3-STATE Output Leakage @ B_n		5.5	3.6		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} $\overline{OE}$ = V_{CCA} V_O = V_{CCB}, GND
ΔI_{CC}	Maximum I_{CCT}/Input @ A_n, T/$\overline{R}$, $\overline{OE}$		5.5	3.6	1.0	1.35	1.5	mA	V_I = V_{CCA} − 2.1V
	Input @ B_n		5.5	3.6		0.35	0.5	mA	V_I = V_{CCB} − 0.6V

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CCA} (V)	V_{CCB} (V)	T_A +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
I_{CCA}	Quiescent V_{CCA} Supply Current	5.5	3.6		8	80	µA	A_n = V_{CCA} or GND B_n = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = GND
I_{CCB}	Quiescent V_{CCB} Supply Current	5.5	3.6		5	50	µA	A_n = V_{CCA} or GND B_n = V_{CCB} or GND, $\overline{OE}$ = GND T/$\overline{R}$ = V_{CCA}
V_{OLPA}	Quiet Output Maximum	5.0	3.3		1.5		V	(Note 4)(Note 5)
V_{OLPB}	Dynamic V_{OL}	5.0	3.3		0.8			
V_{OLVA}	Quiet Output Minimum	5.0	3.3		−1.2		V	(Note 4)(Note 5)
V_{OLVB}	Dynamic V_{OL}	5.0	3.3		−0.8			
V_{IHDA}	Minimum HIGH Level	5.0	3.3		2.0		V	(Note 4)(Note 6)
V_{IHDB}	Dynamic Input Voltage	5.0	3.3		2.0			
V_{ILDA}	Maximum LOW Level	5.0	3.3		0.8		V	(Note 4)(Note 6)
V_{ILDB}	Dynamic Input Voltage	5.0	3.3		0.8			

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Worst case package.

Note 5: Max number of outputs defined as (n). Data inputs are driven 0V to V_{CC} level; one output at GND.

Note 6: Max number of Data Inputs (n) switching. (n–1) inputs switching 0V to V_{CC} level. Input-under-test switching: V_{CC} level to threshold (V_{IHD}), OV to threshold (V_{ILD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameters	T_A = +25°C, C_L = 50 pF, V_{CCA} = 5V (Note 7), V_{CCB} = 3.3V (Note 8)			T_A = −40°C to +85°C, C_L = 50 pF, V_{CCA} = 5V (Note 7), V_{CCB} = 3.3V (Note 8)		T_A = −40°C to +85°C, C_L = 50 pF, V_{CCA} = 5V (Note 7), V_{CCB} = 2.7V		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	5.1	8.5	1.0	9.0	1.0	10.0	ns
t_{PLH}	A to B	1.0	5.3	8.5	1.0	9.0	1.0	10.0	
t_{PHL}	Propagation Delay	1.0	5.4	8.5	1.0	9.0	1.0	10.0	ns
t_{PLH}	B to A	1.0	5.5	8.5	1.0	9.0	1.0	10.0	
t_{PZL}	Output Enable Time	1.0	6.5	10.0	1.0	10.5	1.0	11.5	ns
t_{PZH}	$\overline{OE}$ to B	1.0	6.7	10.0	1.0	10.5	1.0	11.5	
t_{PZL}	Output Enable Time	1.0	5.2	9.0	1.0	9.5	1.0	10.0	ns
t_{PZH}	$\overline{OE}$ to A	1.0	5.8	9.0	1.0	9.5	1.0	10.0	
t_{PHZ}	Output Disable Time	1.0	6.0	9.5	1.0	10.0	1.0	10.0	ns
t_{PLZ}	$\overline{OE}$ to B	1.0	3.3	6.5	1.0	7.0	1.0	7.5	
t_{PHZ}	Output Disable Time	1.0	3.9	7.0	1.0	7.5	1.0	7.5	ns
t_{PLZ}	$\overline{OE}$ to A	1.0	2.9	6.5	1.0	7.0	1.0	7.5	
t_{OSHL}	Output to Output								
t_{OSLH}	Skew (Note 9)		1.0	1.5		1.5		1.5	ns
	Data to Output								

Note 7: Voltage Range 5.0V is 5.0V ± 0.5V.

Note 8: Voltage Range 3.3V is 3.3V ± 0.3V.

Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}). Parameter guaranteed by design.

Capacitance

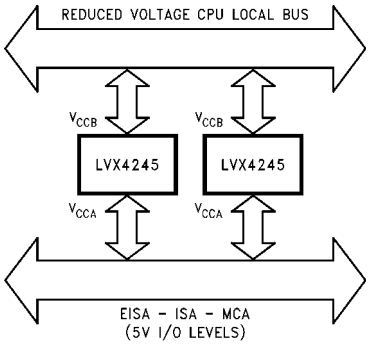
Symbol	Parameter		Typ	Units	Conditions
C_{IN}	Input Capacitance		4.5	pF	V_{CC} = Open
$C_{I/O}$	Input/Output Capacitance		15	pF	V_{CCA} = 5.0V V_{CCB} = 3.3V
C_{PD}	Power Dissipation Capacitance (Note 10)	B→A	55	pF	V_{CCA} = 5.0V V_{CCB} = 3.3V
		A→B	40	pF	

Note 10: C_{PD} is measured at 10 MHz

8-Bit Dual Supply Translating Transceiver

The LVX4245 is a dual supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low voltage CPU local bus with memory and a standard bus defined by 5V I/O levels. The device control inputs can be controlled by either the low voltage CPU and core logic or a bus arbitrator with 5V I/O levels.

Manufactured on a sub-micron CMOS process, the LVX4245 is ideal for mixed voltage applications such as notebook computers using 3.3V CPU's and 5V peripheral devices.



Power Up Considerations

To insure the system does not experience unnecessary I_{CC} current draw, bus contention, or oscillations during power up, the following guidelines should be adhered to (refer to Table 1):

- Power up the control side of the device first. This is the V_{CCA}.
- $\overline{OE}$ should ramp with or ahead of V_{CCA}. This will help guard against bus contention.
- The Transmit/Receive control pin (T/$\overline{R}$) should ramp with or ahead of V_{CCA}, this will ensure that the A Port data pins are configured as inputs. With V_{CCA} receiving power first, the A I/O Port should be configured as inputs to help guard against bus contention and oscillations.
- A side data inputs should be driven to a valid logic level. This will prevent excessive current draw.

The above steps will ensure that no bus contention or oscillations, and therefore no excessive current draw occurs during the power up cycling of these devices. These steps will help prevent possible damage to the translator devices and potential damage to other system components.

TABLE 1. Low Voltage Translator Power Up Sequencing Table

Device Type	V_{CCA}	V_{CCB}	T/$\overline{R}$	$\overline{OE}$	A Side I/O	B Side I/O	Floatable Pin Allowed
74LVX4245	5V (power up 1st)	3V (power up 2nd)	ramp with V_{CCA}	ramp with V_{CCA}	logic 0V or V_{CCA}	outputs	No

Please reference Application Note AN-5001 for more detailed information on using Fairchild's LVX Low Voltage Dual Supply CMOS Translating Transceivers.

Applications: Mixed Mode Dual Supply Interface Solution

LVX4245 is designed to solve 3V/5V interfacing issues when CMOS devices cannot tolerate I/O levels above their applied V_{CC}. If an I/O pin of 3V ICs is driven by 5V ICs, the P-Channel transistor in 3V ICs will conduct causing current flow from I/O bus to the 3V power supply. The resulting high current flow can cause destruction of 3V ICs through latchup effects. To prevent this problem, a current limiting resistor is used typically under direct connection of 3V ICs and 5V ICs, but it causes speed degradation.

In a better solution, the LVX4245 configures two different output levels to handle the dual supply interface issues. The “A” port is a dedicated 5V port to interface 5V ICs. The “B” port is a dedicated port to interface 3V ICs. *Figure 2* shows how LVX4245 fits into a system with 3V subsystem and 5V subsystem.

This device is also configured as an 8-bit 245 transceiver, giving the designer 3-STATE capabilities and the ability to select either bidirectional or unidirectional modes. Since the center 20 pins are also pin compatible to 74 series 245, as shown in *Figure 1*, the designer could use this device in either a 3V system or a 5V system without any further work to re-layout the board.

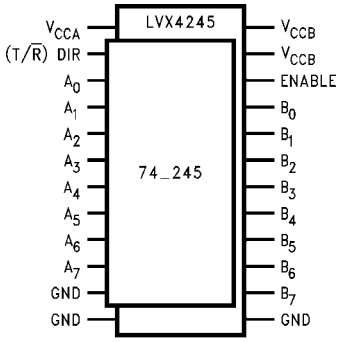


FIGURE 1. LVX4245 Pin Arrangement is Compatible to 20-Pin 74 Series 245

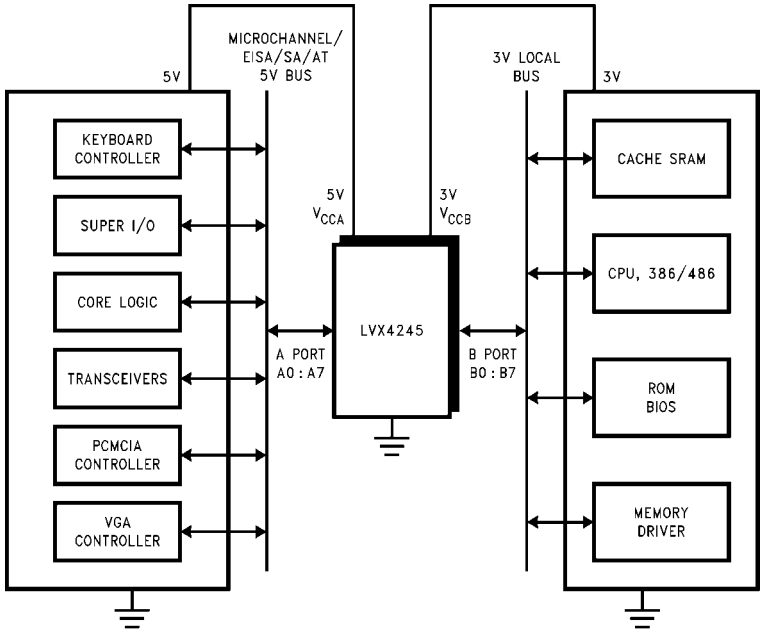
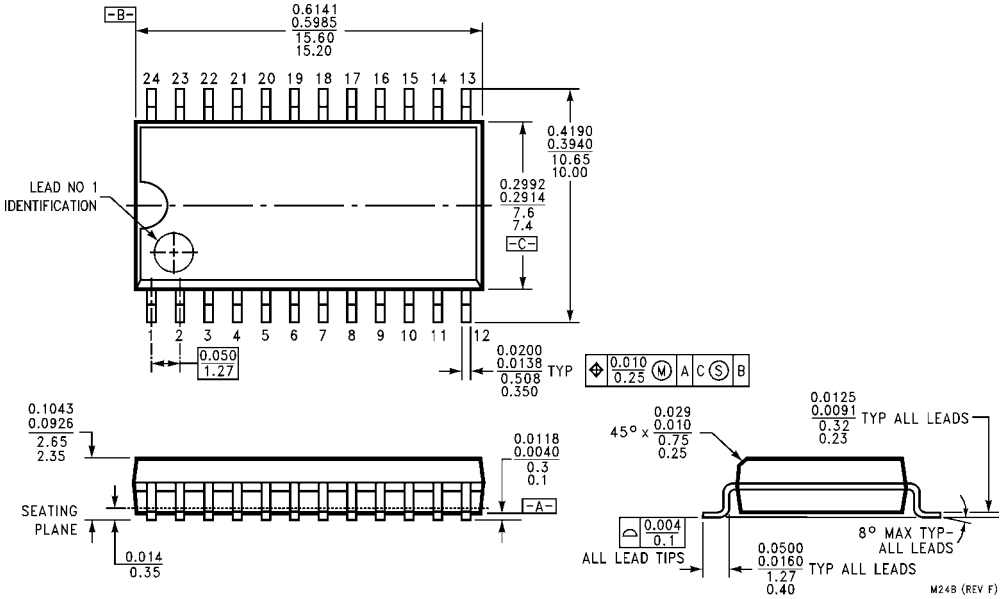
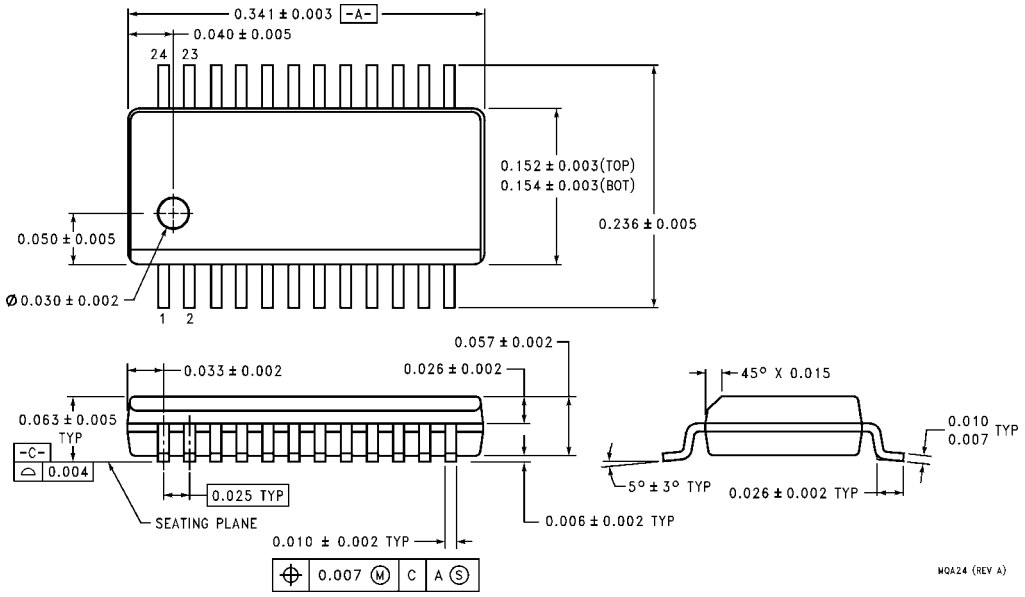


FIGURE 2. LVX4245 Fits into a System with 3V Subsystem and 5V Subsystem

Physical Dimensions inches (millimeters) unless otherwise noted

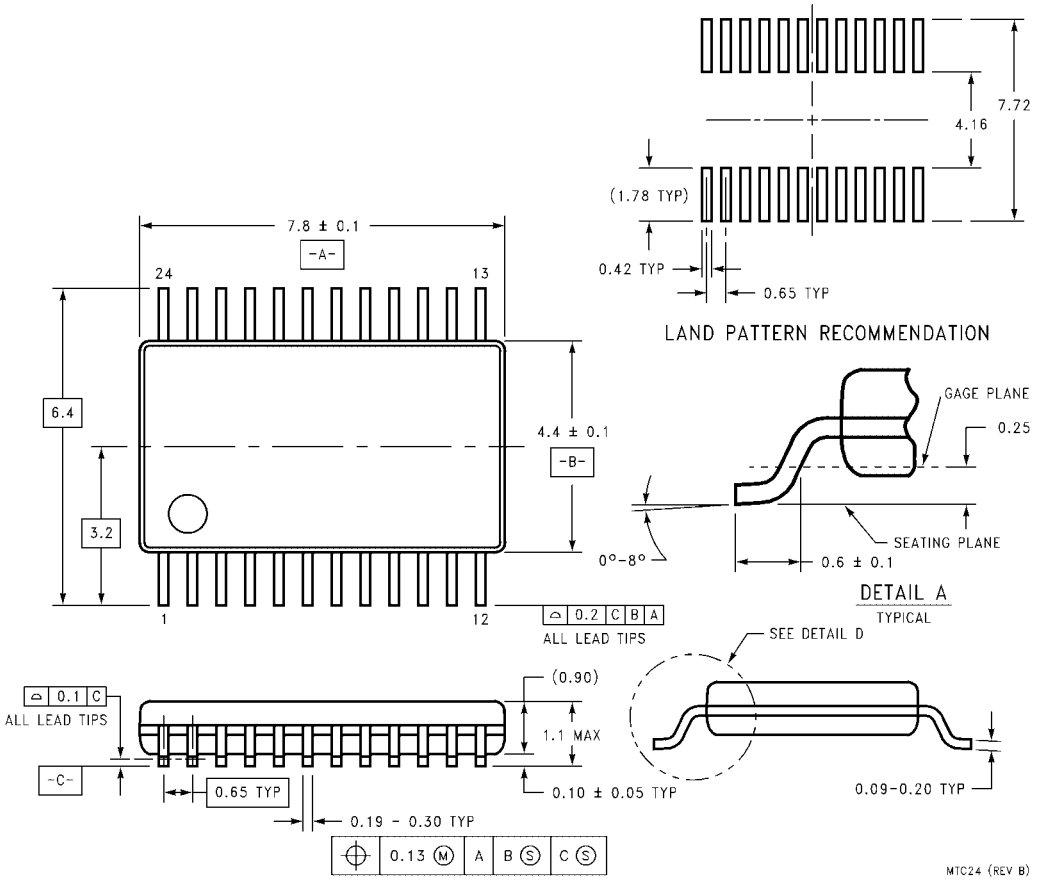


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M24B



24-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide
Package Number MQA24

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC24

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