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January 2016

# FDMD8240L

## Dual N-Channel Power Trench<sup>®</sup> MOSFET 40 V, 98 A, 2.6 mΩ

### Features

- Max  $r_{DS(on)}$  = 2.6 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 23\text{ A}$
- Max  $r_{DS(on)}$  = 3.95 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 19\text{ A}$
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- Termination is Lead-free and RoHS Compliant

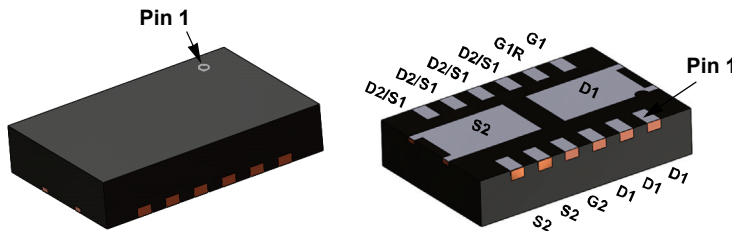


### General Description

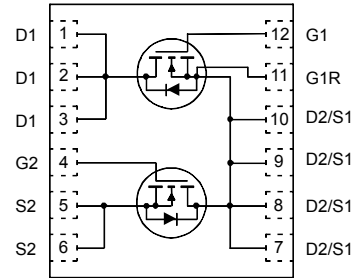
This device includes two 40V N-Channel MOSFETs in a dual Power (3.3 mm X 5 mm) package. HS source and LS Drain are internally connected for half/full bridge, low source inductance package, low  $r_{DS(on)}$ /Qg FOM silicon.

### Applications

- Synchronous Buck : Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge : Primary Switch of Half / Full bridge Converter for BLDC Motor
- MV POL: Synchronous Buck Switch



Power 3.3 x 5



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	40	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	$T_C = 25\text{ °C}$ (Note 5)	98
	-Continuous	$T_C = 100\text{ °C}$ (Note 5)	62
	-Continuous	$T_A = 25\text{ °C}$ (Note 1a)	23
	-Pulsed	(Note 4)	464
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	216
$P_D$	Power Dissipation	$T_C = 25\text{ °C}$	42
	Power Dissipation	$T_A = 25\text{ °C}$ (Note 1a)	2.1
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	60	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
8240L	FDMD8240L	Power 3.3 x 5	13 "	12 mm	3000 units

FDMD8240L Dual N-Channel PowerTrench<sup>®</sup> MOSFET

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		23		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 23\text{ A}$		2.0	2.6	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 19\text{ A}$		3.2	3.95	
		$V_{GS} = 10\text{ V}$ , $I_D = 23\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		3.0	3.9	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 23\text{ A}$		107		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$		3020	4230	pF
$C_{oss}$	Output Capacitance			876	1230	
$C_{rss}$	Reverse Transfer Capacitance			33	52	
$R_g$	Gate Resistance		0.1	2.8	6	

### Switching Characteristics

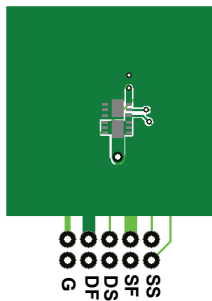
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\text{ V}$ , $I_D = 23\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		12	22	ns
$t_r$	Rise Time			8	16	
$t_{d(off)}$	Turn-Off Delay Time			36	58	
$t_f$	Fall Time			9	18	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$		40	
	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	$V_{DD} = 20\text{ V}$ $I_D = 23\text{ A}$	21	30	
$Q_{gs}$	Gate to Source Charge			9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			5		nC

### Drain-Source Diode Characteristics

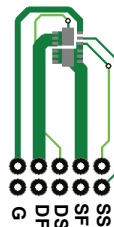
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 23\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}$ , $I_S = 1.6\text{ A}$ (Note 2)		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 23\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		41	65	ns
$Q_{rr}$	Reverse Recovery Charge			21	32	

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



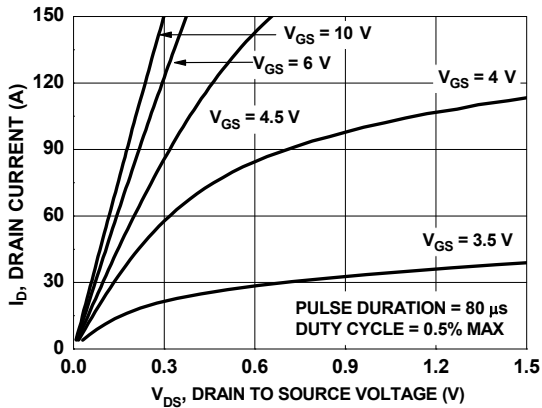
a. 60 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



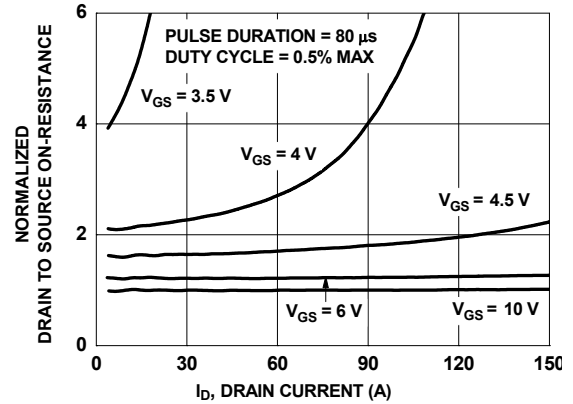
b. 130 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.
- $E_{AS}$  of 216 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 12\text{ A}$ ,  $V_{DD} = 40\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 37\text{ A}$ .
- Pulsed Id please refer to Fig 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

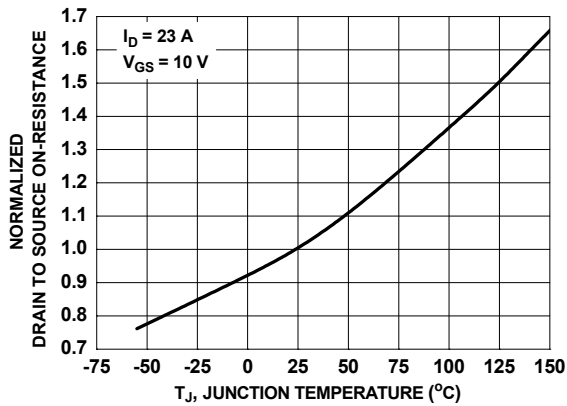
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



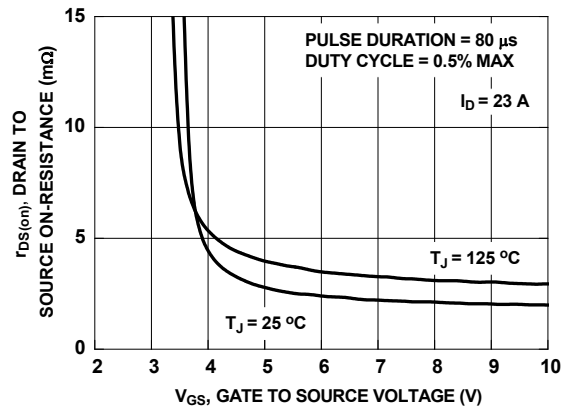
**Figure 1. On-Region Characteristics**



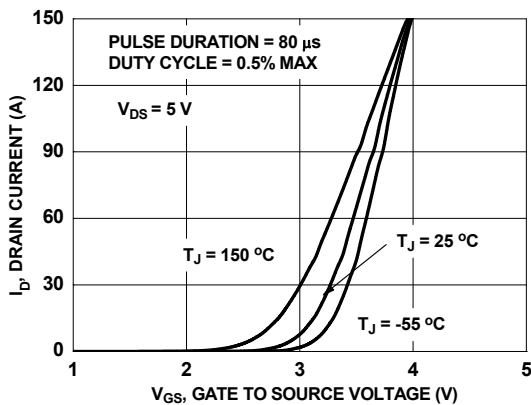
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



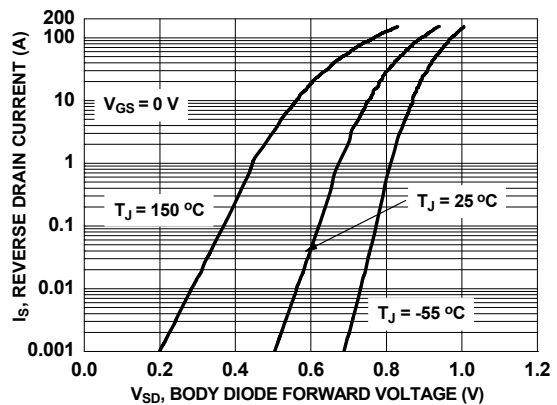
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On Resistance vs. Gate to Source Voltage**

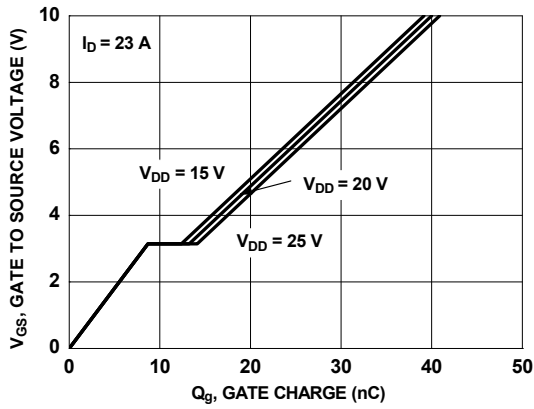


**Figure 5. Transfer Characteristics**

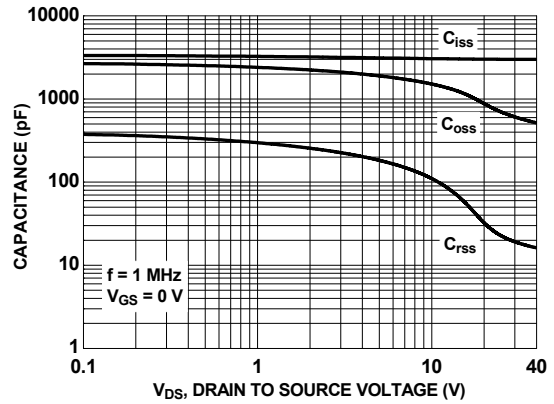


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

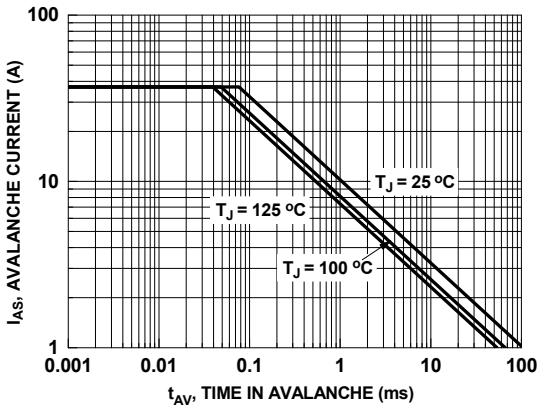
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.



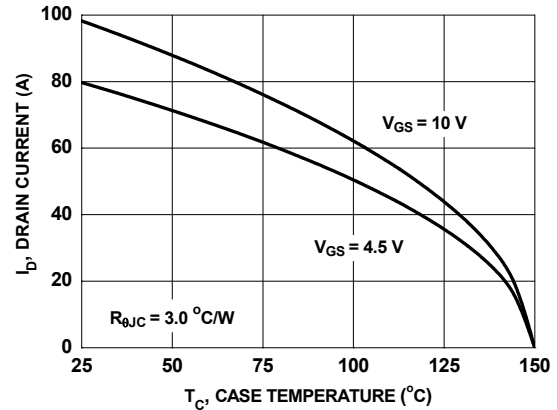
**Figure 7. Gate Charge Characteristics**



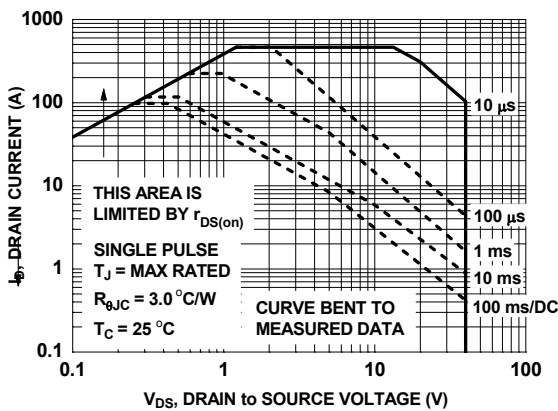
**Figure 8. Capacitance vs. Drain to Source Voltage**



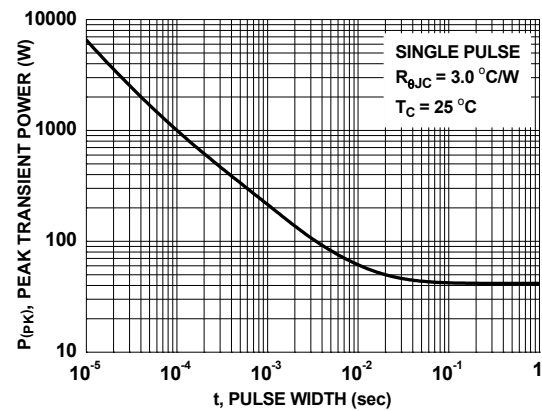
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

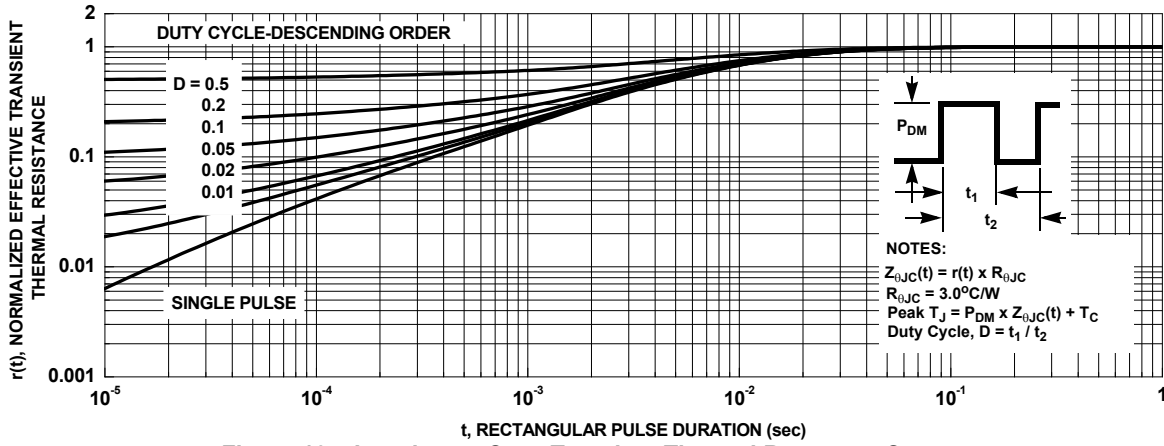


**Figure 11. Forward Bias Safe Operating Area**

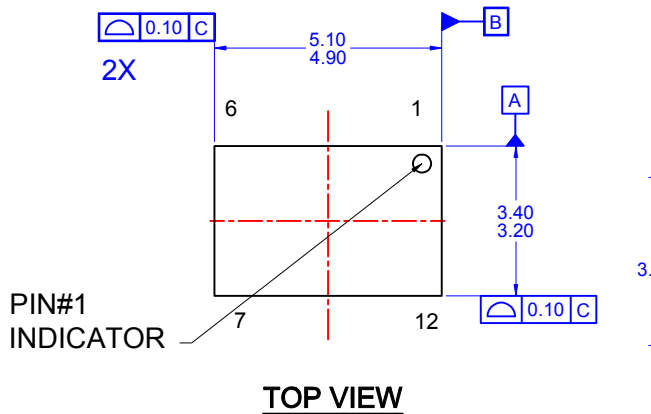


**Figure 12. Single Pulse Maximum Power Dissipation**

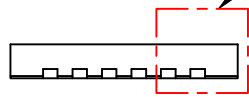
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

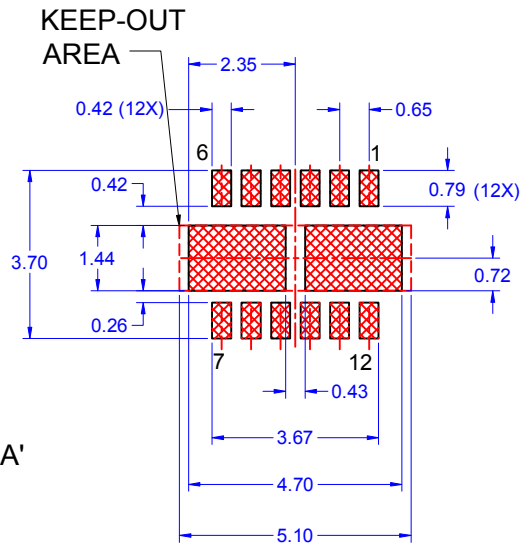


**TOP VIEW**

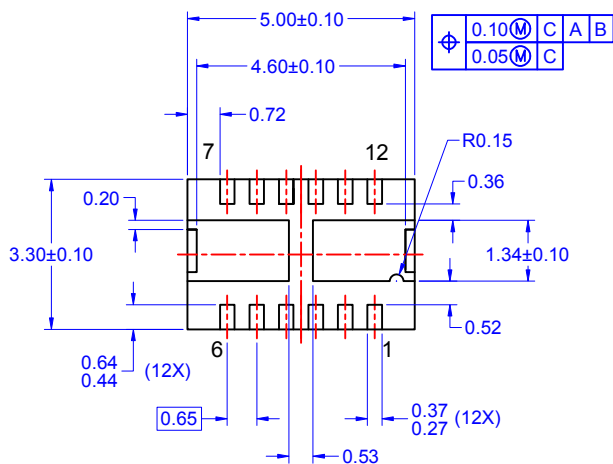


**FRONT VIEW**

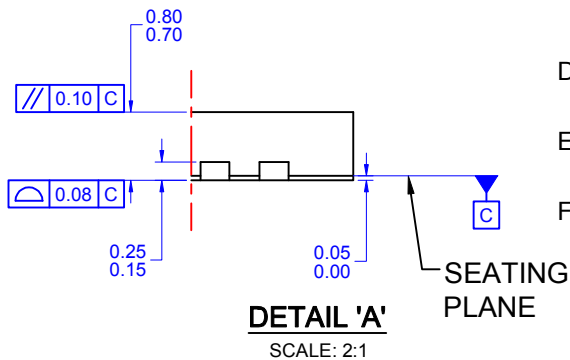
SEE  
DETAIL 'A'



**LAND PATTERN  
RECOMMENDATION**



**BOTTOM VIEW**



**DETAIL 'A'**

SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

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- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
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