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December 2010

BSS138W

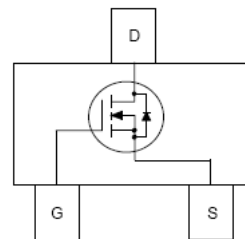
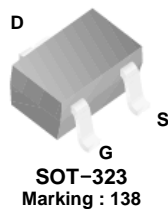
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode field effect transistor. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- $R_{DS(ON)} = 3.5\Omega @ V_{GS} = 10V, I_D = 0.22A$
 $R_{DS(ON)} = 6.0\Omega @ V_{GS} = 4.5V, I_D = 0.22A$
- High density cell design for extremely low $R_{DS(ON)}$
- Rugged and Reliable
- Compact industry standard SOT-323 surface mount package



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{DSS}	Drain-Source Voltage	50	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current - Continuous (Note1)	0.21	A
	- Pulsed	0.84	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Maximum Power Dissipation (Note1)	340	mW
	Derate Above 25°C	2.72	$\text{mW}/^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note1)	367	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
138	BSS138W	7"	8mm	3000 units

BSS138W — N-Channel Logic Level Enhancement Mode Field Effect Transistor

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C		71		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50V, V_{GS} = 0V$ $V_{DS} = 50V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ $V_{DS} = 30V, V_{GS} = 0V$			0.5 5 100	μA μA nA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
On Characteristics (Note2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1\text{mA}$, Referenced to 25°C		-3.9		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 0.22\text{A}$ $V_{GS} = 4.5V, I_D = 0.22\text{A}$ $V_{GS} = 10V, I_D = 0.22\text{A}, T_J = 125^\circ\text{C}$		1.17 1.36 2.16	3.5 6.0 5.8	Ω Ω Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10V, V_{DS} = 5V$	0.2			A
g_{FS}	Forward Transconductance	$V_{DS} = 10V, I_D = 0.22\text{A}$	0.12			S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{MHz}$		38		pF
C_{oss}	Output Capacitance			5.9		pF
C_{rss}	Reverse Transfer Capacitance			3.5		pF
R_G	Gate Resistance	$V_{GS} = 15\text{mV}, f = 1.0\text{MHz}$		11		Ω
Switching Characteristics (Note2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30V, I_D = 0.29\text{A},$ $V_{GS} = 10V, R_{GEN} = 6\Omega$		2.3	5	ns
t_r	Turn-On Rise Time			1.9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			6.7	36	ns
t_f	Turn-Off Fall Time			6.5	14	ns
Q_g	Total Gate Change	$V_{DS} = 25V, I_D = 0.22\text{A},$ $V_{GS} = 10V$		1.1		nC
Q_{gs}	Gate-Source Change			0.12		nC
Q_{gd}	Gate-Drain Change			0.22		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.22	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 0.44\text{A}$ (Note2)			1.4	V

Notes:

- 367°C/W when mounted on a minimum pad.
- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Performance Characteristics

Figure 1. On-Region Characteristics.

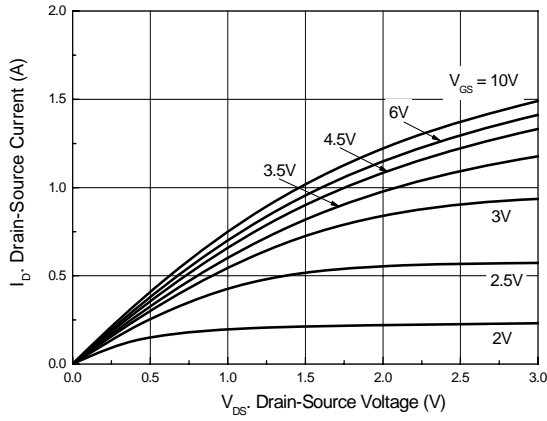


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

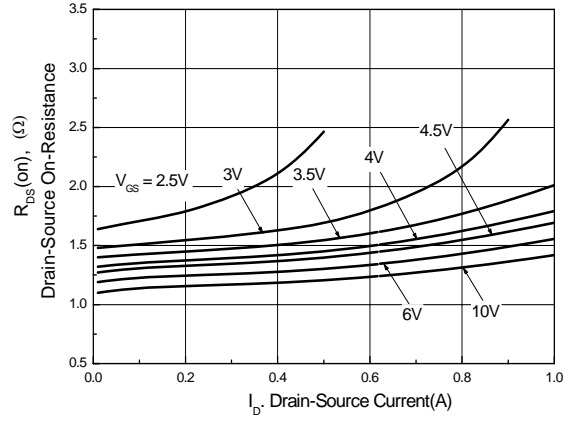


Figure 3. On-Resistance Variation with Temperature.

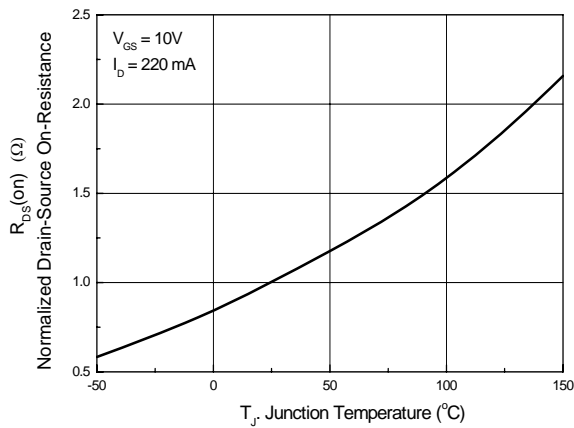


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

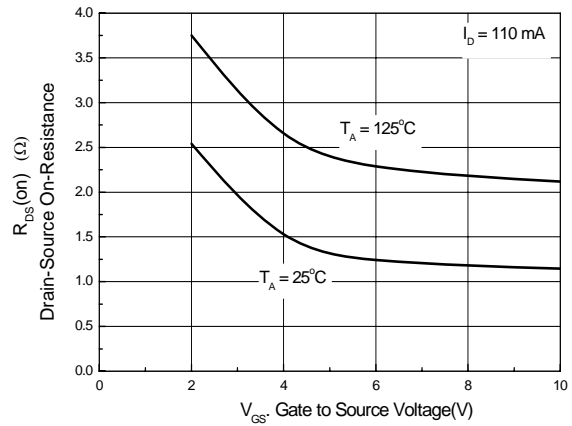


Figure 5. Drain-Source On Voltage with Temperature.

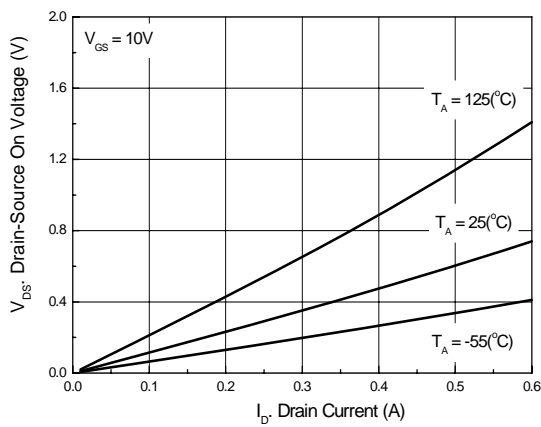
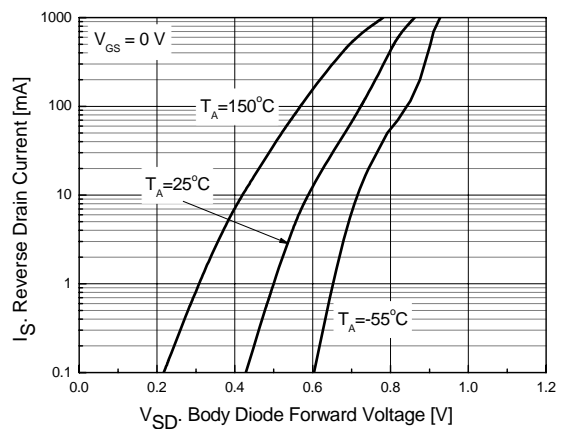


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



Typical Performance Characteristics (Continued)

Figure 7. Gate Charge Characteristics.

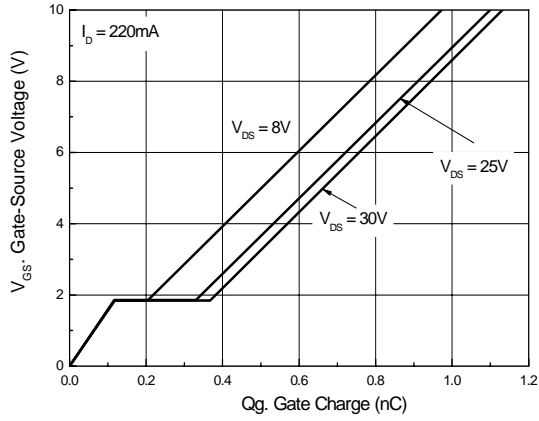


Figure 8. Capacitance Characteristics.

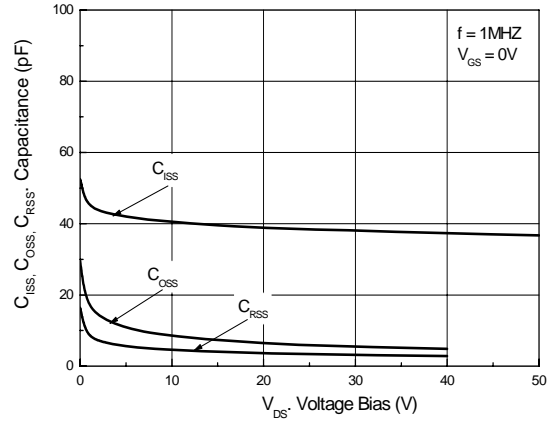


Figure 9. Maximum Safe Operating Area.

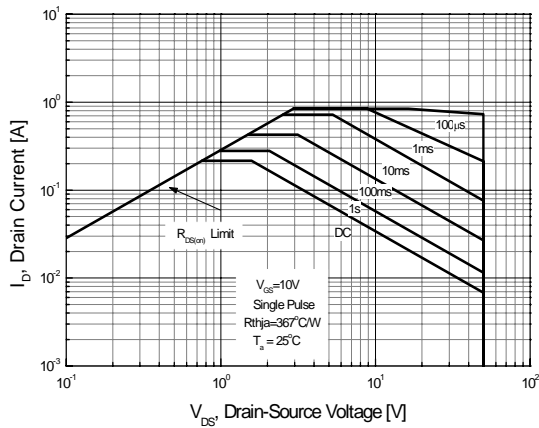


Figure 10. Single Pulse Maximum Power Dissipation.

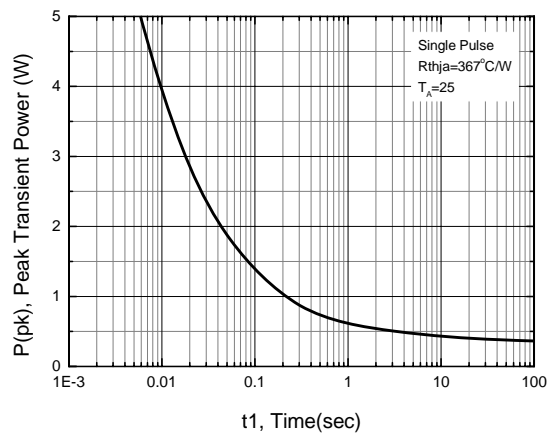
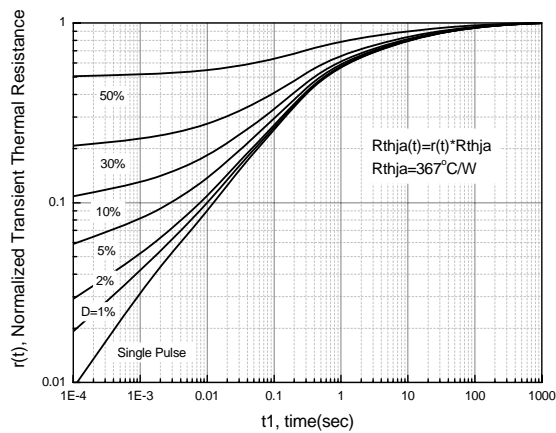
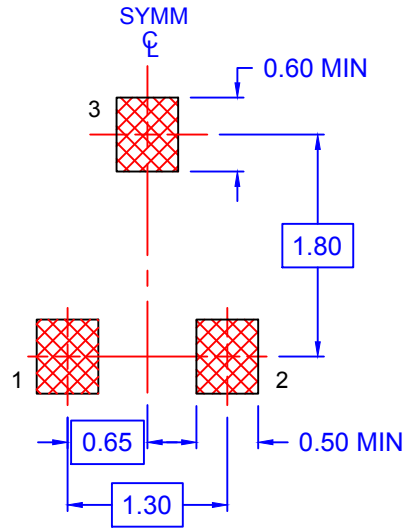
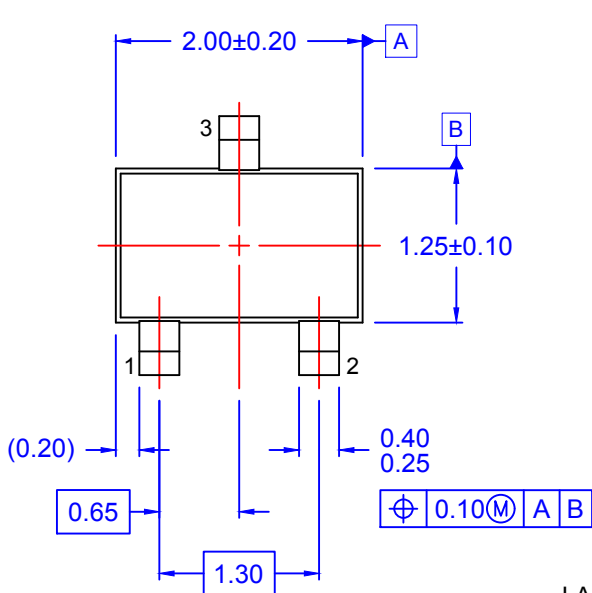
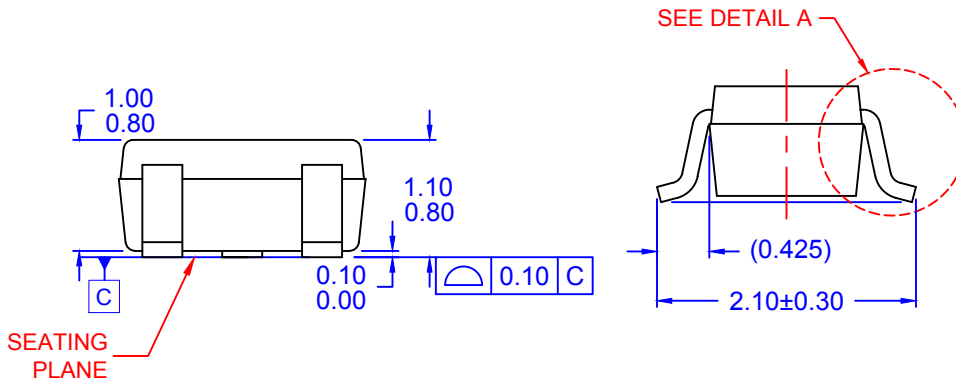


Figure 11. Transient Thermal Response Curve.



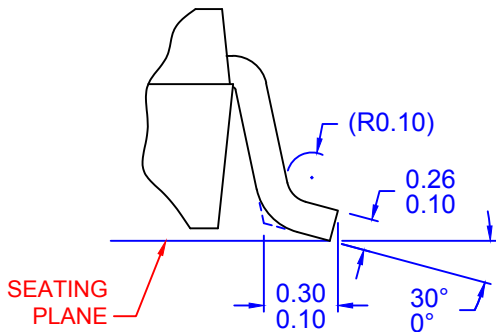


LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-70.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E) DRAWING FILE NAME: MKT-MAA03AREV2



DETAIL A
SCALE: 2X



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