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FQPF9N50CF

N-Channel QFET® FRFET® MOSFET

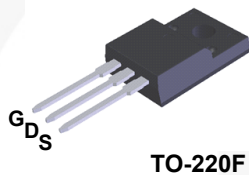
500 V, 9 A, 850 mΩ

Description

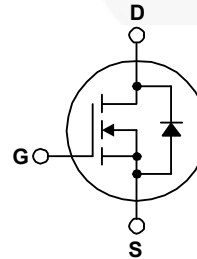
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 9 A, 500 V, $R_{DS(on)}$ = 850 mΩ (Max.) @ $V_{GS} = 10$ V, $I_D = 4.5$ A
- Low Gate Charge (Typ. 28 nC)
- Low Crss (Typ. 24 pF)
- 100% Avalanche Tested
- Fast Recovery Body Diode (Typ. 100 ns)



TO-220F



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQPF9N50CF	Unit
V_{DSS}	Drain-Source Voltage	500	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	9*	A
	Drain Current - Continuous ($T_C = 100^\circ\text{C}$)	5.4*	A
I_{DM}	Drain Current - Pulsed (Note 1)	36*	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	360	mJ
I_{AR}	Avalanche Current (Note 1)	9	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	4.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	44	W
	- Derate above 25°C	0.35	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	$^\circ\text{C}$

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FQPF9N50CF	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.86	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQPF9N50CF	FQPF9N50CF	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	--	0.57	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$	--	--	10 100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	--	4.0	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 4.5 \text{ A}$	--	0.70	0.85	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_D = 4.5 \text{ A}$	--	6.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$	--	790	1030	pF
C_{oss}	Output Capacitance		--	130	170	pF
C_{riss}	Reverse Transfer Capacitance		--	24	30	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 9 \text{ A},$ $R_G = 25 \Omega$	--	18	45	ns
t_r	Turn-On Rise Time		--	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		--	93	195	ns
t_f	Turn-Off Fall Time		(Note 4)	--	64	125
Q_g	Total Gate Charge	$V_{DS} = 400 \text{ V}, I_D = 9 \text{ A},$ $V_{GS} = 10 \text{ V}$	--	28	35	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	15	--
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9*	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	36*	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 9 \text{ A}$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 9 \text{ A},$ $di_F / dt = 100 \text{ A}/\mu\text{s}$	--	100	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.3	--	μC

NOTES:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 8 \text{ mH}, I_{AS} = 9 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 11 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

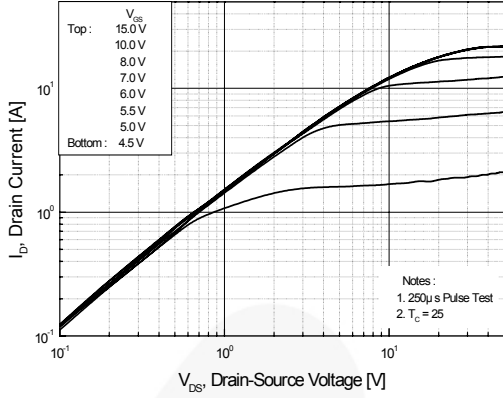


Figure 2. Transfer Characteristics

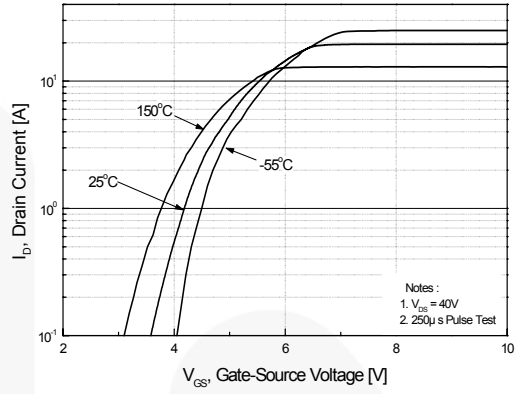


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

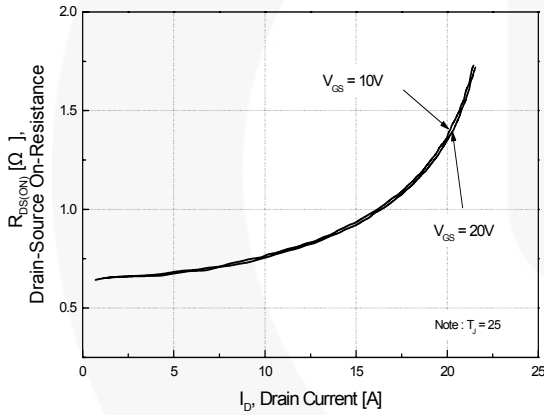


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

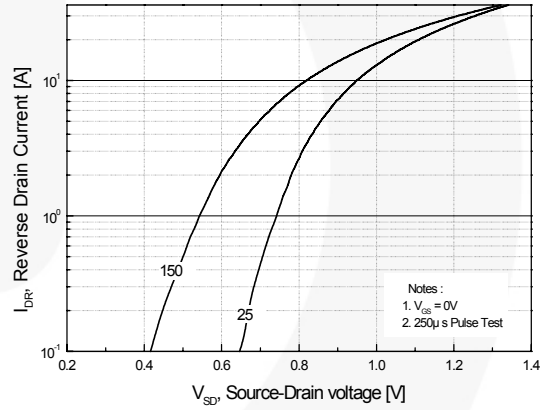


Figure 5. Capacitance Characteristics

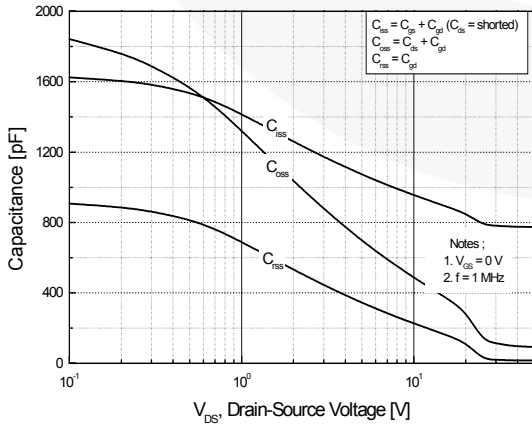
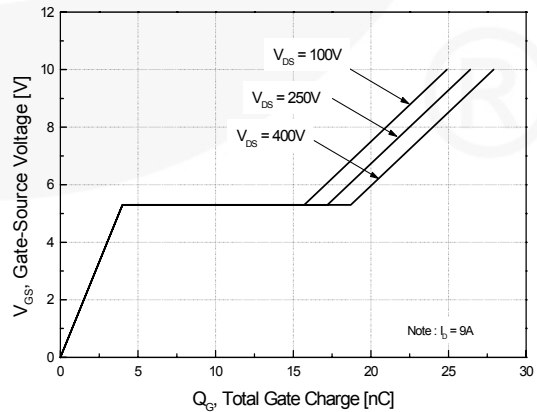


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

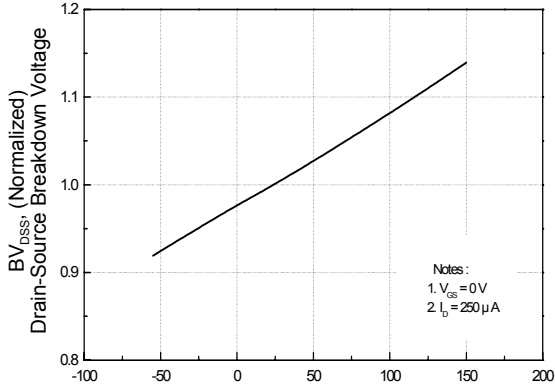


Figure 8. On-Resistance Variation vs. Temperature

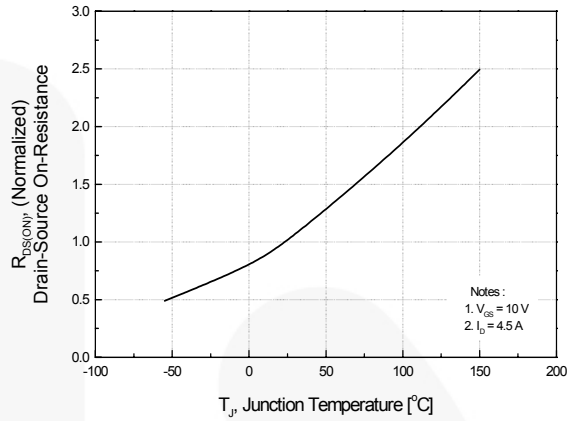


Figure 9. Maximum Safe Operating Area

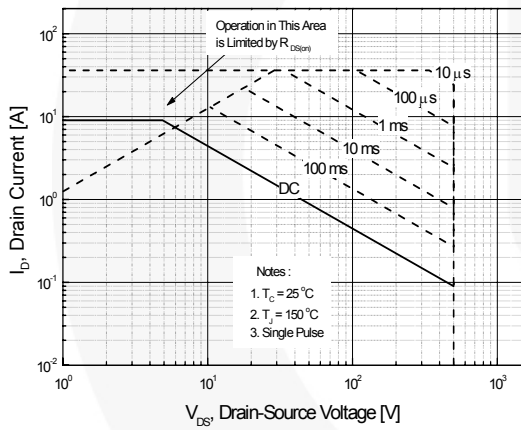


Figure 10. Maximum Drain Current vs. Case Temperature

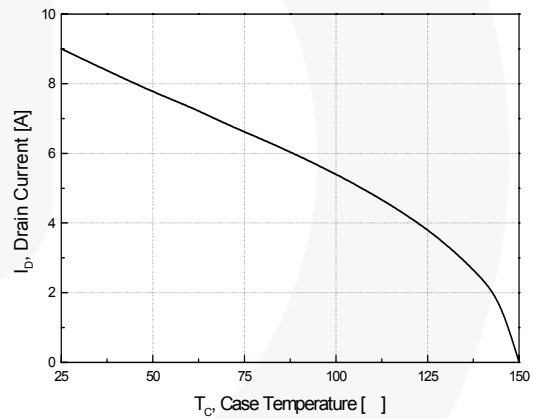
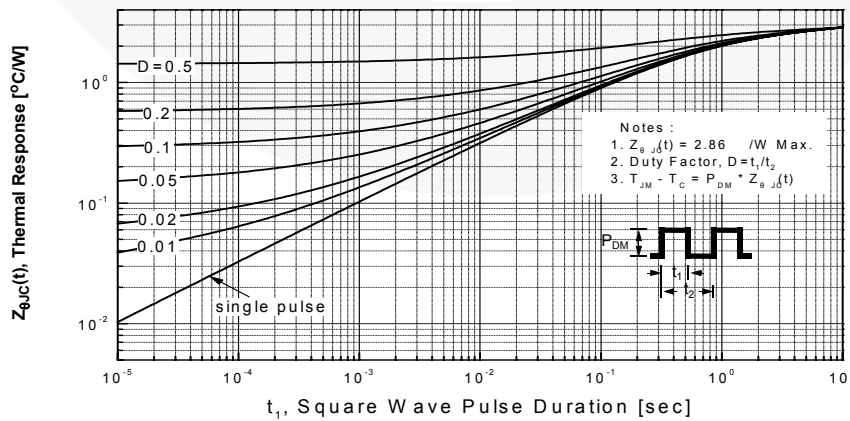


Figure 11. Transient Thermal Response Curve



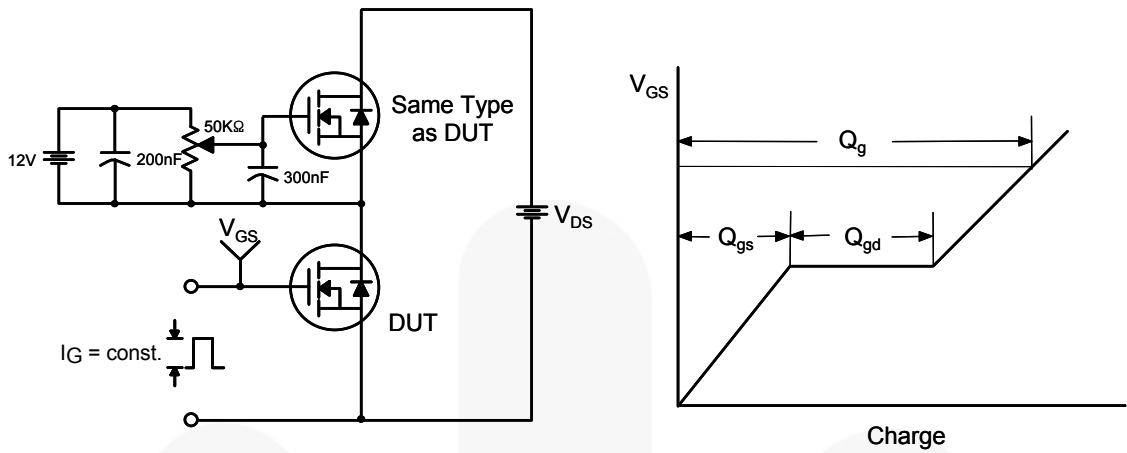


Figure 12. Gate Charge Test Circuit & Waveform

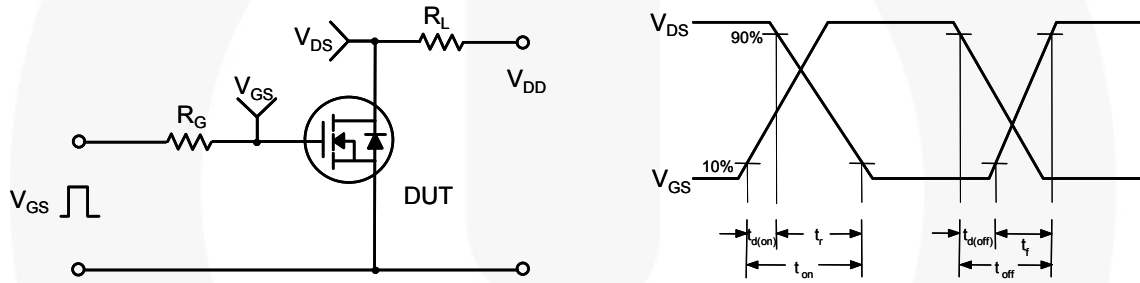


Figure 13. Resistive Switching Test Circuit & Waveforms

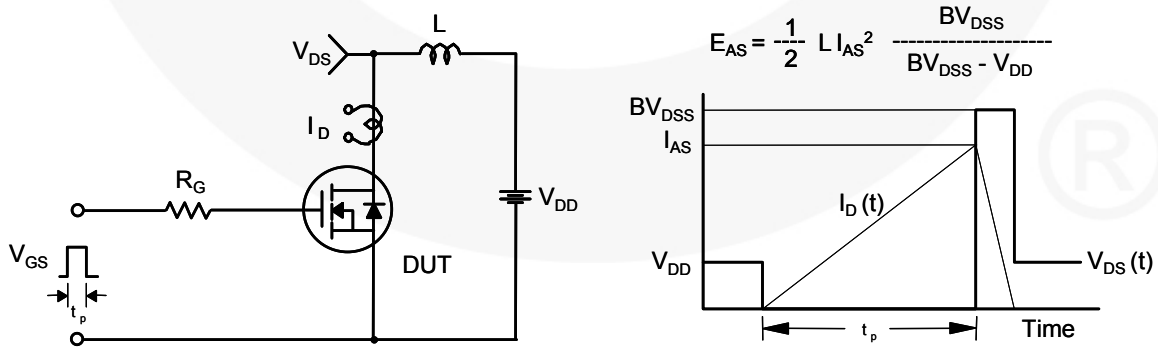


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

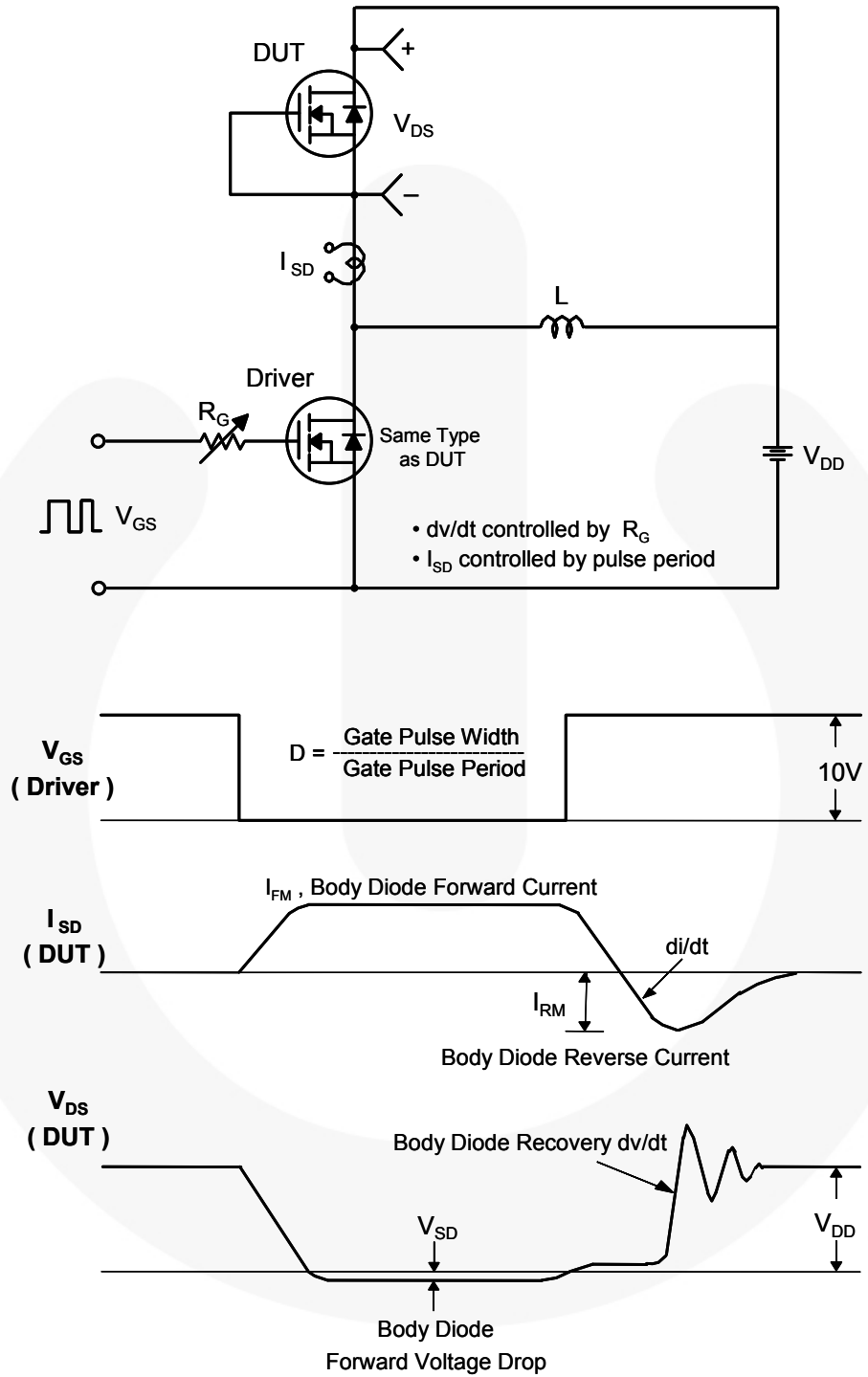


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

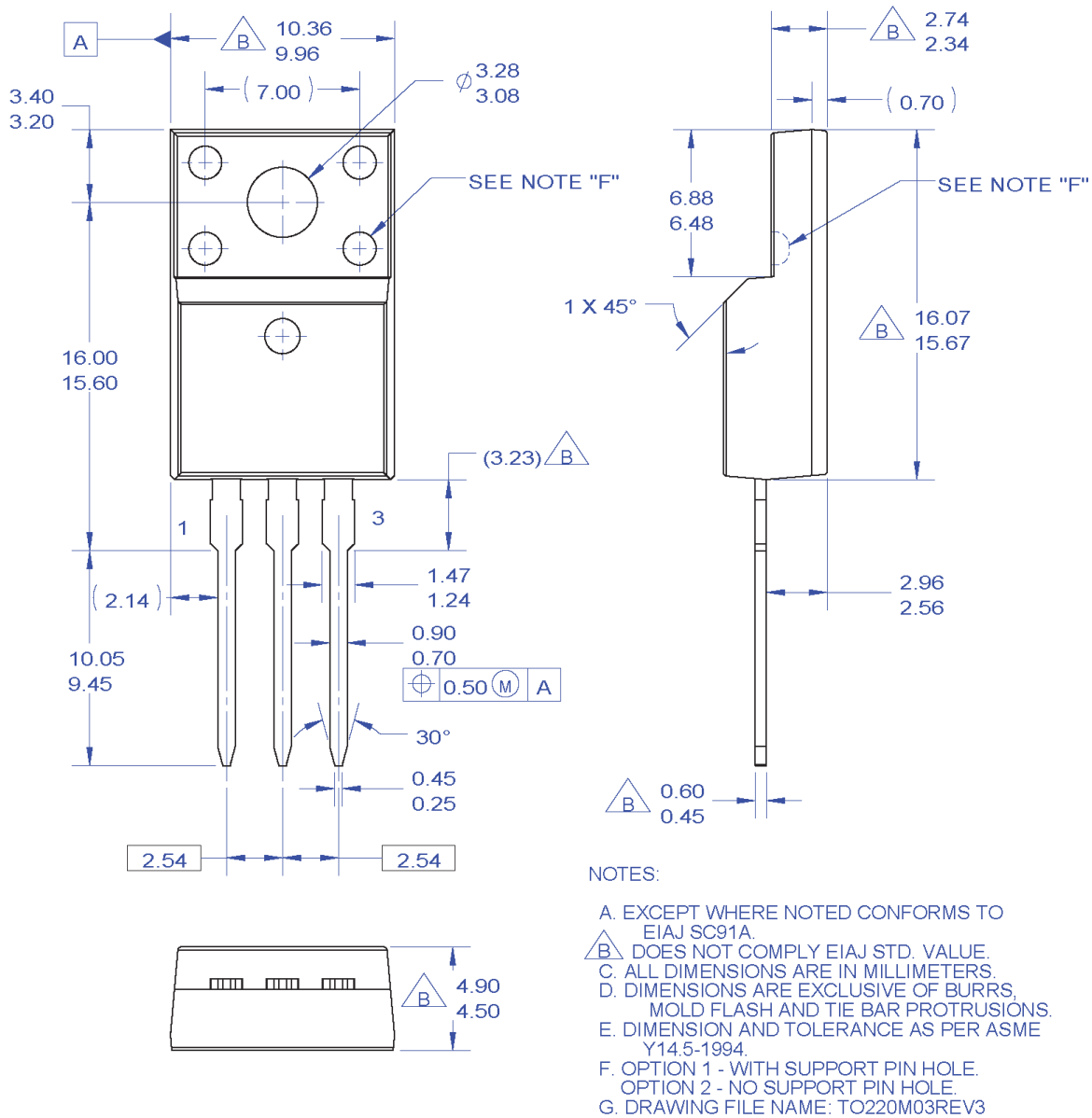


Figure 16. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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