



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

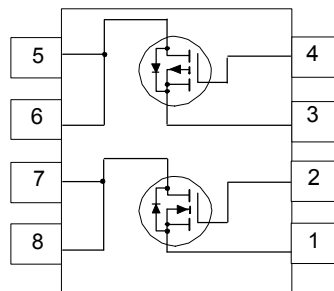
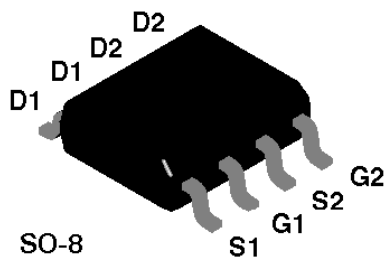
## NDS9952A Dual N & P-Channel Enhancement Mode Field Effect Transistor

### General Description

These dual N- and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- N-Channel 3.7A, 30V,  $R_{DS(ON)}=0.08\Omega @ V_{GS}=10V$ .  
P-Channel -2.9A, -30V,  $R_{DS(ON)}=0.13\Omega @ V_{GS}=-10V$ .
- High density cell design or extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DSS}$	Drain-Source Voltage	30	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current - Continuous (Note 1a)	$\pm 3.7$	$\pm 2.9$	A
	- Pulsed	$\pm 15$	$\pm 10$	
$P_D$	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>								
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	30			V	
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-30			V	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			2	$\mu\text{A}$	
				$T_J = 55^\circ\text{C}$			25	$\mu\text{A}$
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-2	$\mu\text{A}$	
				$T_J = 55^\circ\text{C}$			-25	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA	
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA	
<b>ON CHARACTERISTICS</b> (Note 2)								
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	1	1.7	2.8	V	
				$T_J = 125^\circ\text{C}$	0.7	1.2		2.2
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-1	-1.6	-2.8		
				$T_J = 125^\circ\text{C}$	-0.85	-1.25		-2.5
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	N-Ch		0.06	0.08	$\Omega$	
				$T_J = 125^\circ\text{C}$		0.08		0.13
		$V_{GS} = 4.5\text{ V}, I_D = 0.5\text{ A}$	N-Ch		0.08	0.11		
				$T_J = 125^\circ\text{C}$		0.11		0.18
		$V_{GS} = -10\text{ V}, I_D = -1.0\text{ A}$	P-Ch		0.11	0.13		
				$T_J = 125^\circ\text{C}$		0.15		0.21
$V_{GS} = -4.5\text{ V}, I_D = -0.5\text{ A}$		0.17	0.2					
		$T_J = 125^\circ\text{C}$		0.24	0.32			
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	15			A	
		$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-10				
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 3.7\text{ A}$	N-Ch		6		S	
		$V_{DS} = -15\text{ V}, I_D = -2.9\text{ A}$	P-Ch		4			
<b>DYNAMIC CHARACTERISTICS</b>								
$C_{iss}$	Input Capacitance	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		320		pF	
			P-Ch		350			
$C_{oss}$	Output Capacitance		P-Channel $V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		225		pF
				P-Ch		260		
$C_{rss}$	Reverse Transfer Capacitance			N-Ch		85		pF
				P-Ch		100		

### Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
<b>SWITCHING CHARACTERISTICS</b> (Note 2)							
t <sub>D(on)</sub>	Turn - On Delay Time	N-Channel V <sub>DD</sub> = 10 V, I <sub>D</sub> = 1 A, V <sub>GEN</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t <sub>r</sub>	Turn - On Rise Time	P-Channel V <sub>DD</sub> = -10 V, I <sub>D</sub> = -1 A, V <sub>GEN</sub> = -10 V, R <sub>GEN</sub> = 6 Ω	N-Ch		13	20	ns
			P-Ch		21	40	
t <sub>D(off)</sub>	Turn - Off Delay Time		N-Ch		21	50	ns
				P-Ch		21	
t <sub>f</sub>	Turn - Off Fall Time	N-Ch		5	50	ns	
			P-Ch		8		50
Q <sub>g</sub>	Total Gate Charge	N-Channel V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.7 A, V <sub>GS</sub> = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q <sub>gs</sub>	Gate-Source Charge	P-Channel V <sub>DS</sub> = -10 V, I <sub>D</sub> = -2.9 A, V <sub>GS</sub> = -10 V	N-Ch		1.5		nC
			P-Ch		1.6		
Q <sub>gd</sub>	Gate-Drain Charge	N-Ch		3.3		nC	
			P-Ch		3.4		

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.2	A
			P-Ch			-1.2	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -1.25 A (Note 2)	P-Ch		-0.8	-1.3	
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>F</sub> = 1.25 A, dI <sub>F</sub> /dt = 100 A/μs	N-Ch			75	ns
		V <sub>GS</sub> = 0 V, I <sub>F</sub> = -1.25 A, dI <sub>F</sub> /dt = 100 A/μs	P-Ch			100	

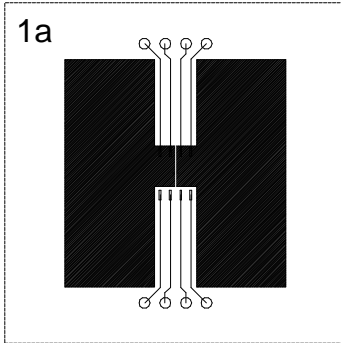
Notes:

- R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

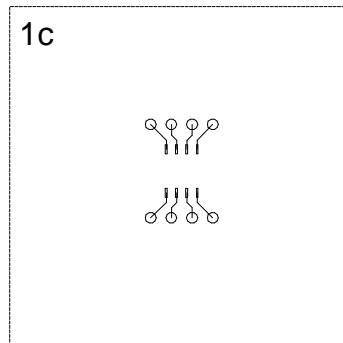
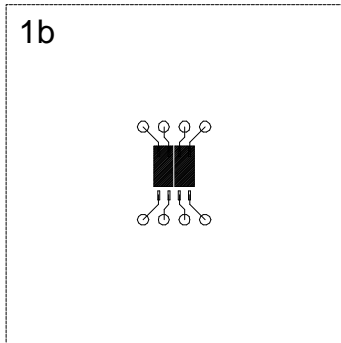
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J} \lambda(t)} = \frac{T_J - T_A}{R_{\theta J} \lambda + R_{\theta CA} \lambda(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical R<sub>θJA</sub> for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 78°C/W when mounted on a 0.5 in<sup>2</sup> pad of 2oz copper.
- 125°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- 135°C/W when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics: N-Channel

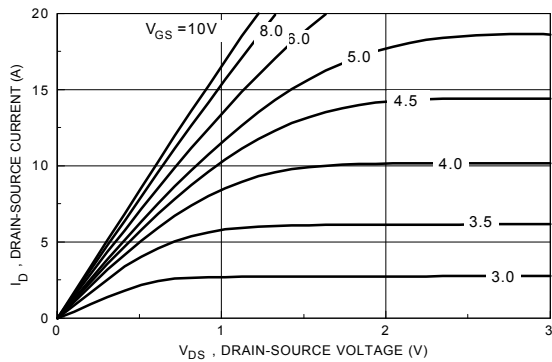


Figure 1. N-Channel On-Region Characteristics.

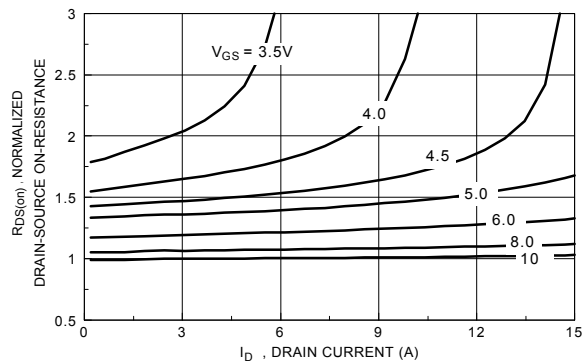


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

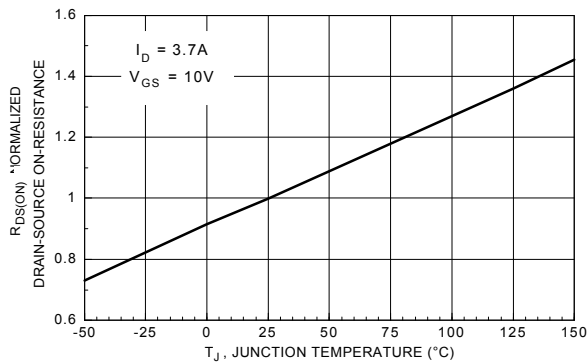


Figure 3. N-Channel On-Resistance Variation with Temperature.

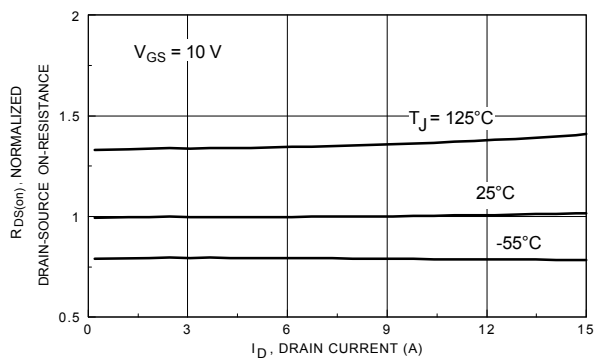


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

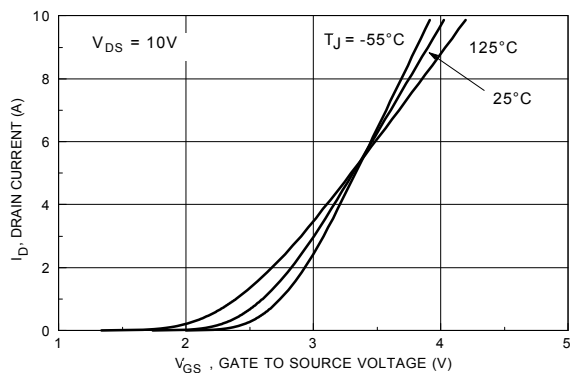


Figure 5. N-Channel Transfer Characteristics.

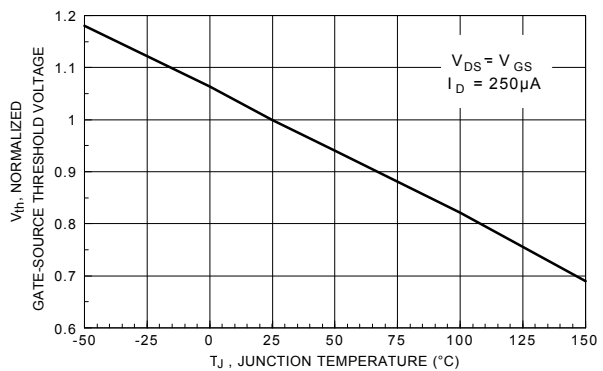
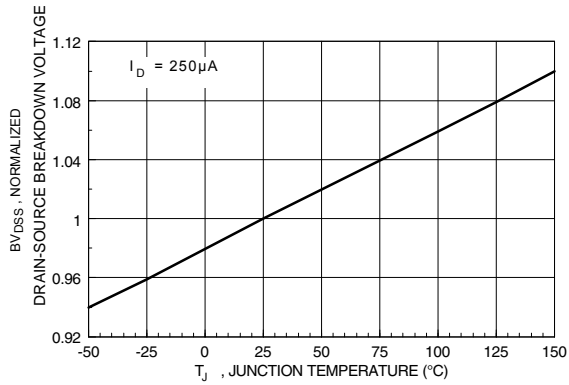
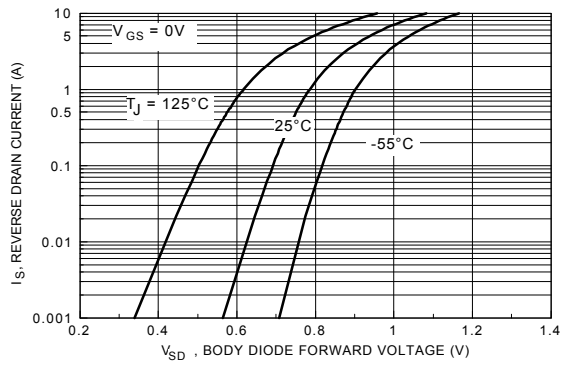


Figure 6. N-Channel Gate Threshold Variation with Temperature.

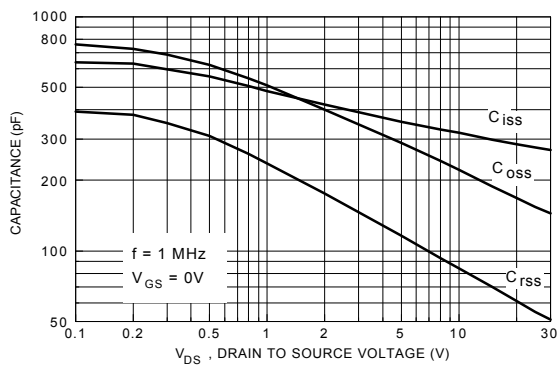
## Typical Electrical Characteristics: N-Channel (continued)



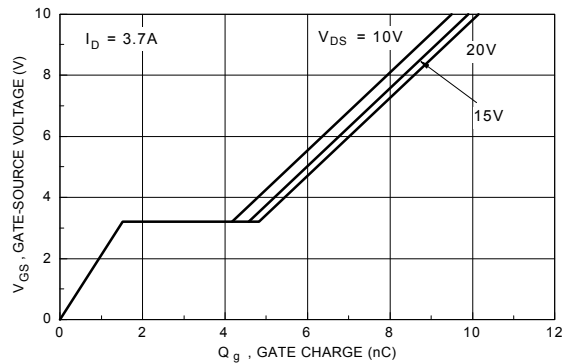
**Figure 7. N-Channel Breakdown Voltage Variation with Temperature.**



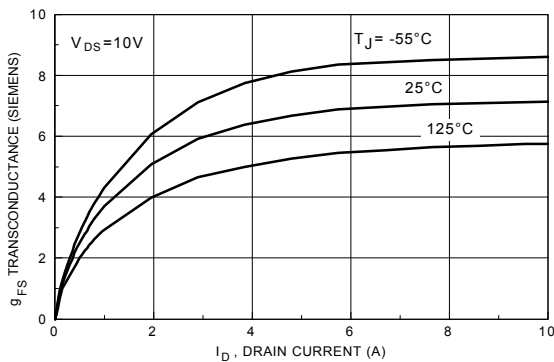
**Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.**



**Figure 9. N-Channel Capacitance Characteristics.**



**Figure 10. N-Channel Gate Charge Characteristics.**



**Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.**

## Typical Electrical Characteristics: P-Channel (continued)

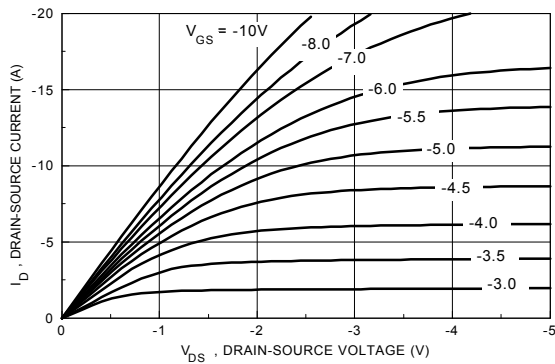


Figure 12. P-Channel On-Region Characteristics.

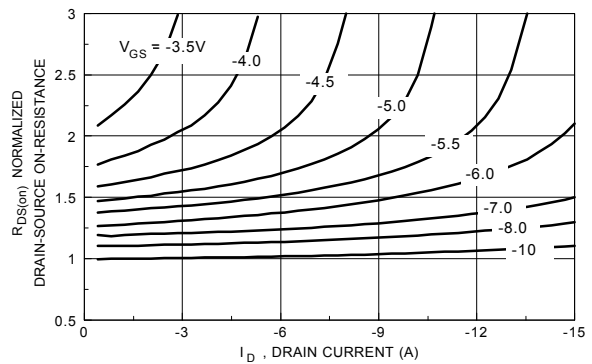


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

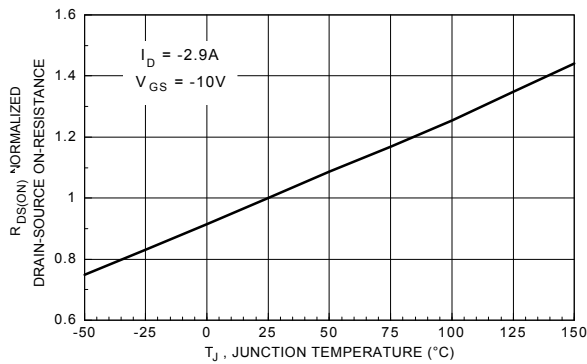


Figure 14. P-Channel On-Resistance Variation with Temperature.

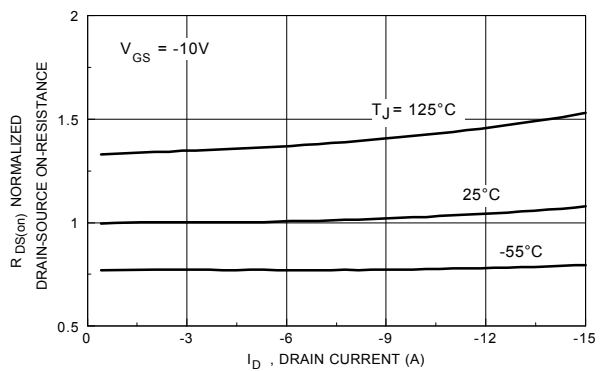


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

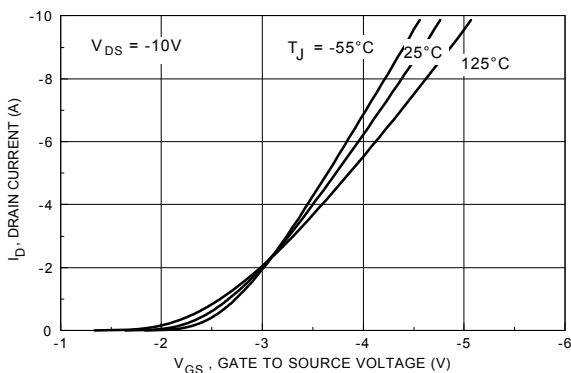


Figure 16. P-Channel Transfer Characteristics.

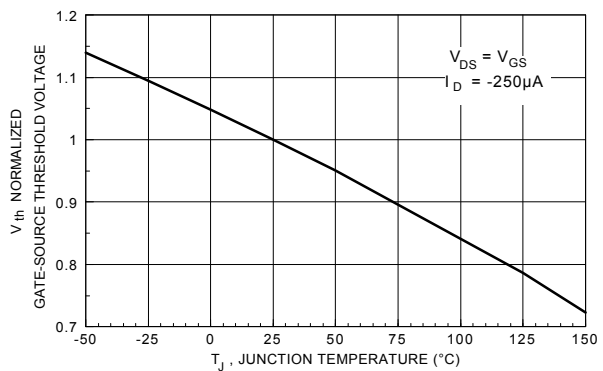


Figure 17. P-Channel Gate Threshold Variation with Temperature.

## Typical Electrical Characteristics: P-Channel (continued)

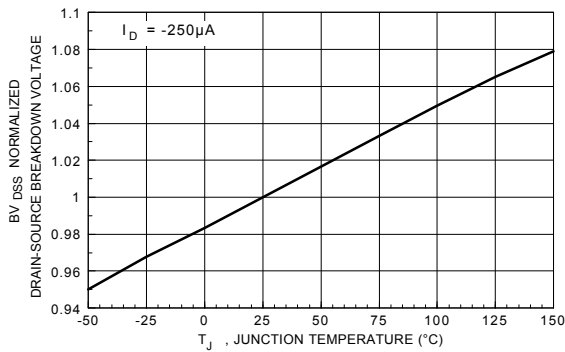


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

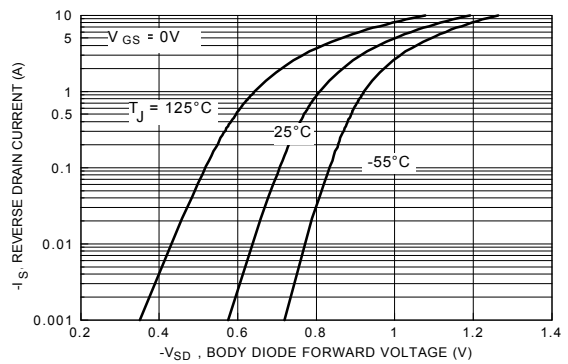


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

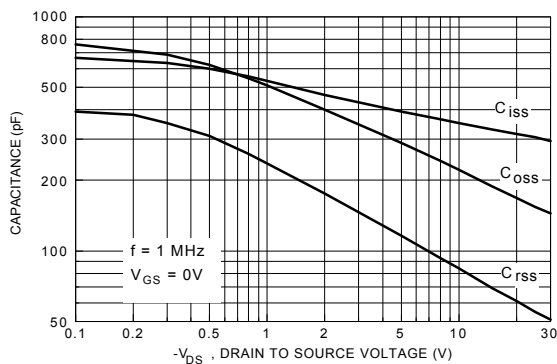


Figure 20. P-Channel Capacitance Characteristics.

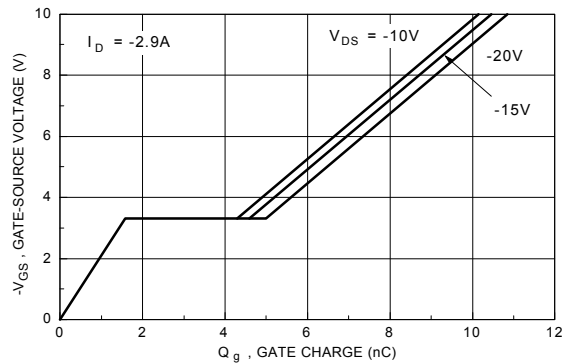


Figure 21. P-Channel Gate Charge Characteristics.

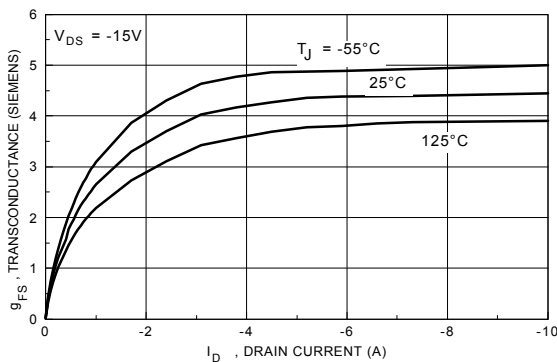
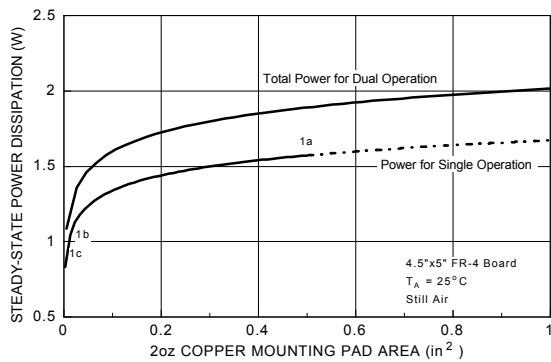


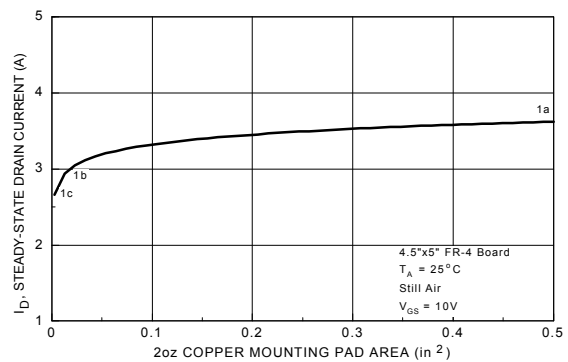
Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.



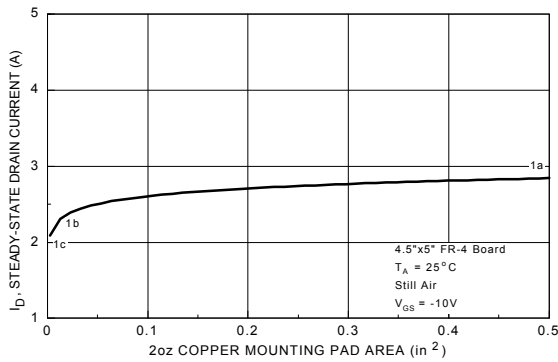
## Typical Thermal Characteristics: N & P-Channel



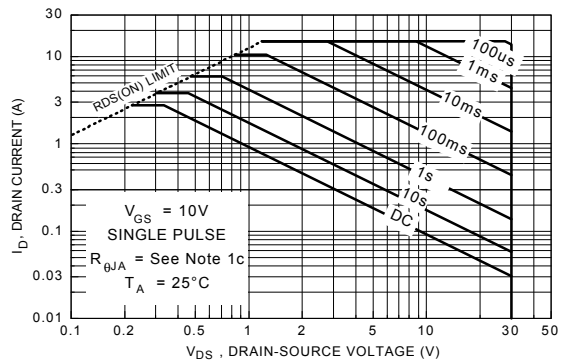
**Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



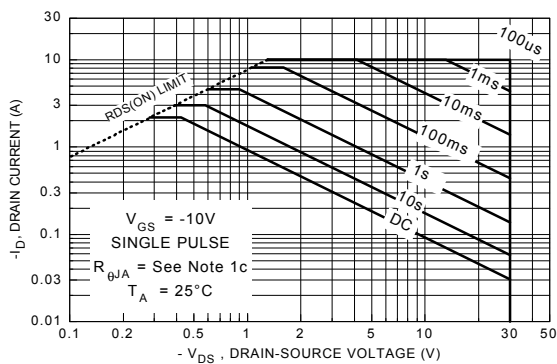
**Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**

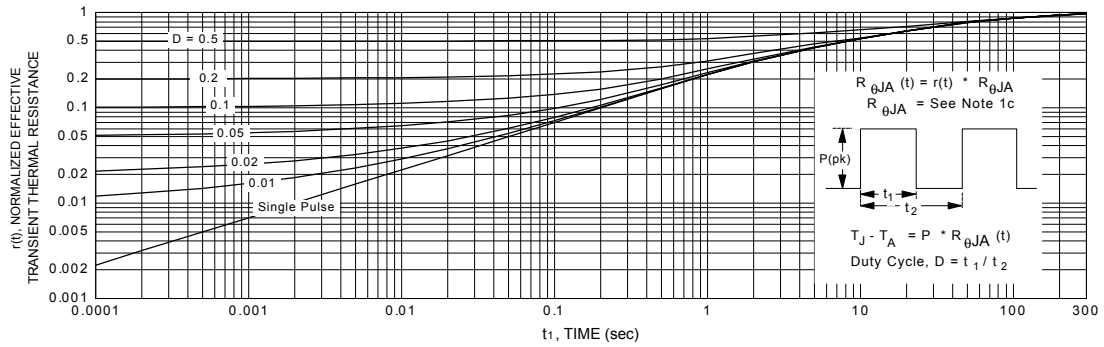


**Figure 26. N-Channel Maximum Safe Operating Area.**



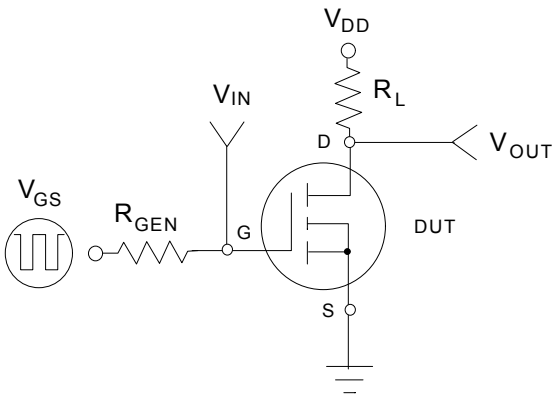
**Figure 27. P-Channel Maximum Safe Operating Area.**

## Typical Thermal Characteristics: N & P-Channel

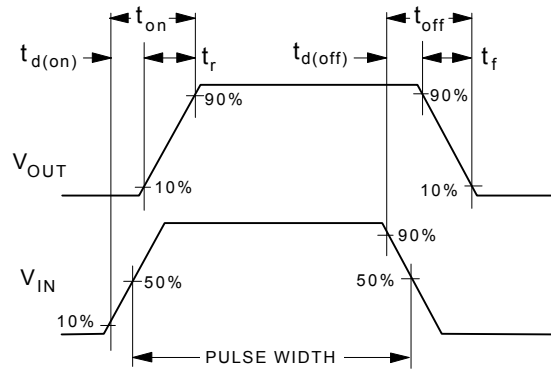


**Figure 28. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.



**Figure 29. N or P-Channel Switching Test Circuit.**



**Figure 30. N or P-Channel Switching Waveforms.**

## TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	HiSeC™	SuperSOT™-8
Bottomless™	ISOPLANAR™	SyncFET™
CoolFET™	MICROWIRE™	TinyLogic™
CROSSVOLT™	POP™	UHC™
E <sup>2</sup> CMOS™	PowerTrench®	VCX™
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local  
Sales Representative