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March 2016

FCH041N65EF

N-Channel SuperFET[®] II FRFET[®] MOSFET

650 V, 76 A, 41 mΩ

Features

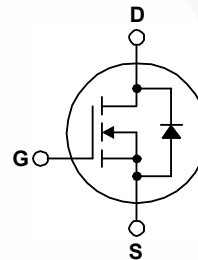
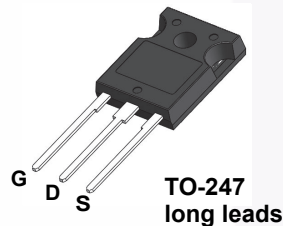
- 700 V @ T_J = 150°C
- Typ. R_{DS(on)} = 36 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 229 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 631 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- LCD / LED / PDP TV
- Telecom / Server Power Supplies
- Solar Inverter
- AC - DC Power Supply

Description

SuperFET[®] II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET[®] MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FCH041N65EF_F155	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	- DC	±20
		- AC (f > 1 Hz)	±30
I _D	Drain Current	- Continuous (T _C = 25°C)	76
		- Continuous (T _C = 100°C)	48.1
I _{DM}	Drain Current	- Pulsed (Note 1)	228
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	2025	mJ
I _{AR}	Avalanche Current (Note 1)	15	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	5.95	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P _D	Power Dissipation (T _C = 25°C)	595	W
		- Derate Above 25°C	4.76
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FCH041N65EF_F155	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.21	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max.	40	

FCH041N65EF — N-Channel SuperFET[®] II FRFET[®] MOSFET

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N65EF_F155	FCH041N65EF	TO-247 G03	Tube	N/A	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}, T_J = 150^\circ\text{C}$	700	-	-	
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, Referenced to 25°C	-	0.72	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	μA
		$V_{DS} = 520\text{ V}, T_C = 125^\circ\text{C}$	-	145	-	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 7.6\text{ mA}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 38\text{ A}$	-	36	41	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 38\text{ A}$	-	71.7	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	9446	12560	pF
C_{oss}	Output Capacitance		-	366	490	pF
C_{riss}	Reverse Transfer Capacitance		-	35	-	pF
C_{oss}	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	197	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	631	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 38\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	229	298	nC
Q_{gs}	Gate to Source Gate Charge		-	50	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	90	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.6	-	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 38\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$ (Note 4)	-	55	120	ns
t_r	Turn-On Rise Time		-	65	140	ns
$t_{d(off)}$	Turn-Off Delay Time		-	175	360	ns
t_f	Turn-Off Fall Time		-	48	106	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	76	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	228	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 38\text{ A}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 38\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	207	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.5	-	μC

Notes:

1. Repetitive rating: pulse width limited by maximum junction temperature.
2. $I_{AS} = 15\text{ A}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 38\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

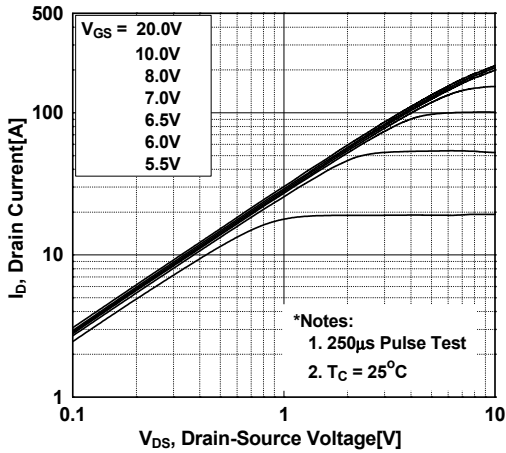


Figure 2. Transfer Characteristics

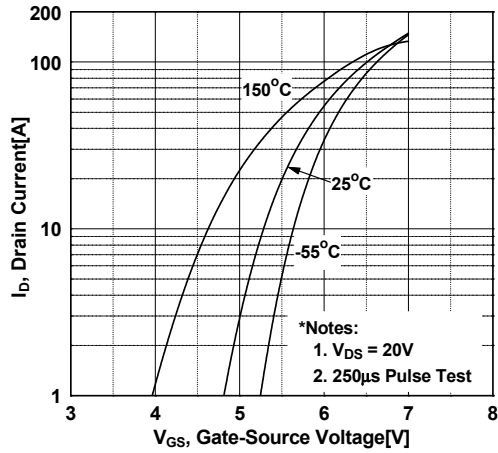


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

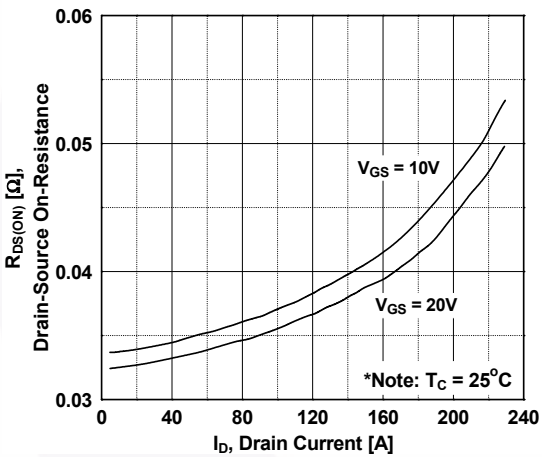


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

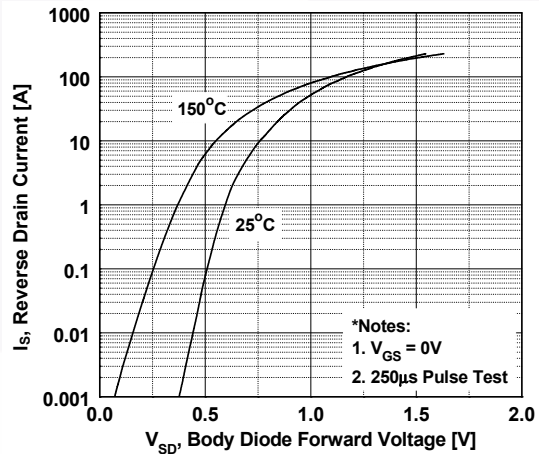


Figure 5. Capacitance Characteristics

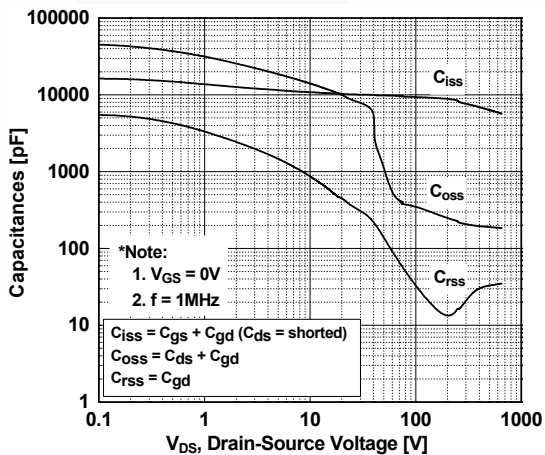
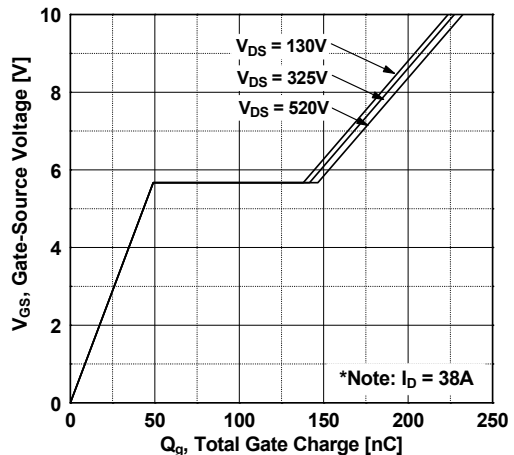


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

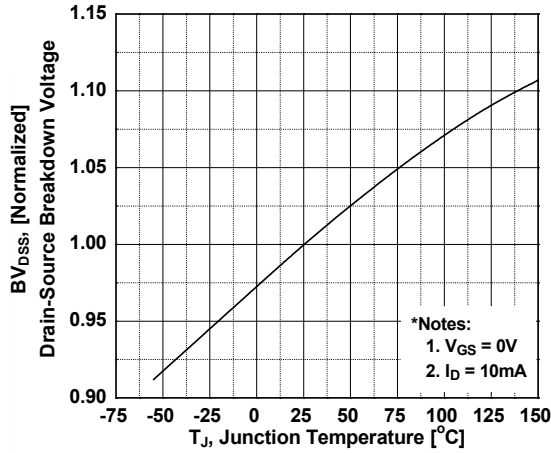


Figure 8. On-Resistance Variation vs. Temperature

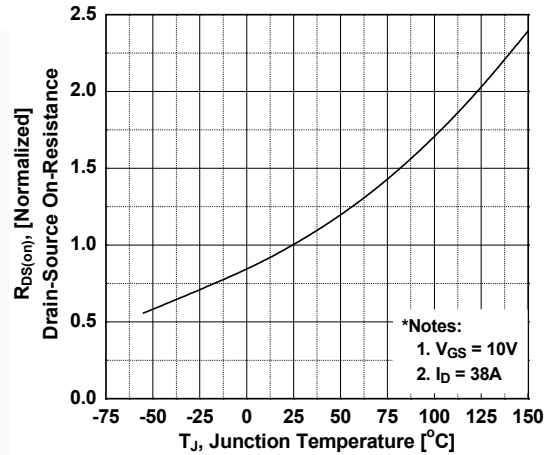


Figure 9. Maximum Safe Operating Area

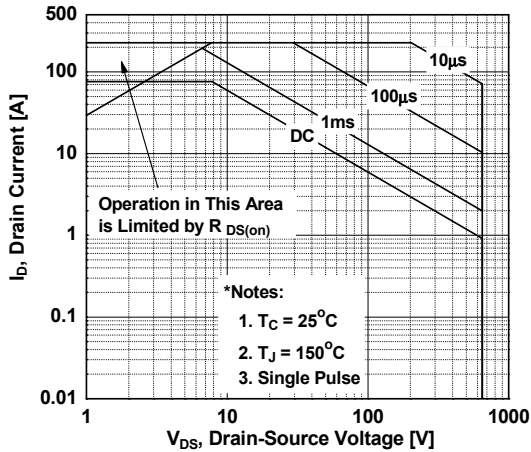


Figure 10. Maximum Drain Current vs. Case Temperature

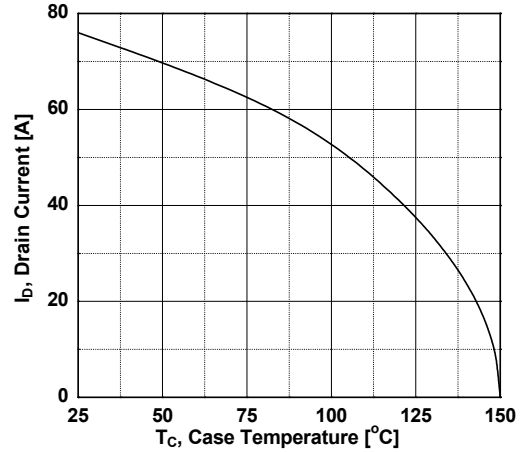
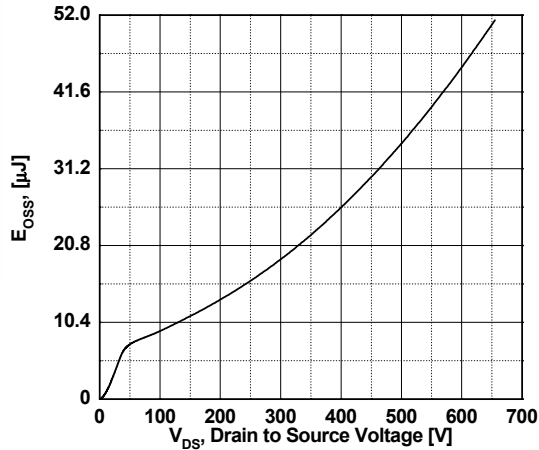
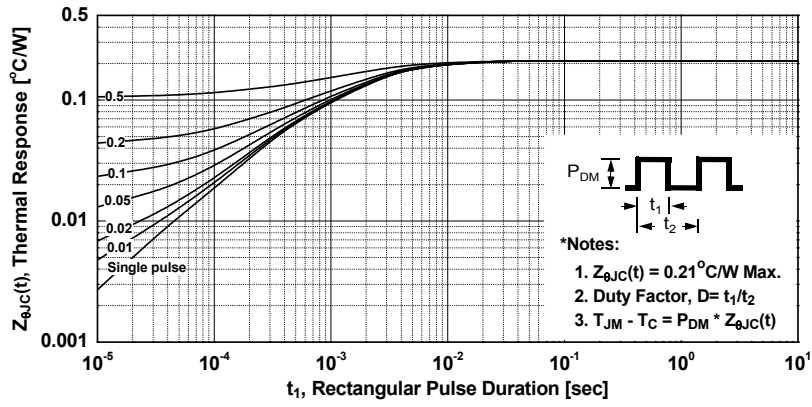


Figure 11. Eoss vs. Drain to Source Voltage



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



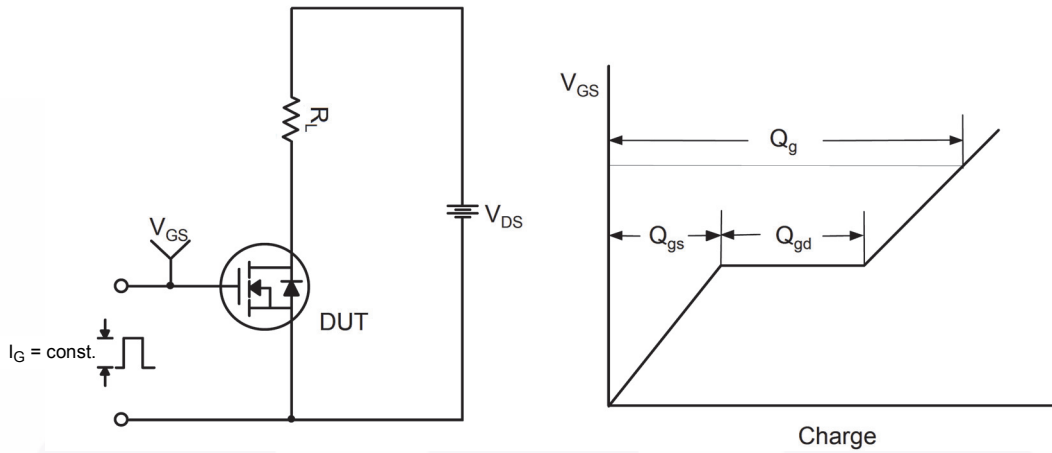


Figure 15. Gate Charge Test Circuit & Waveform



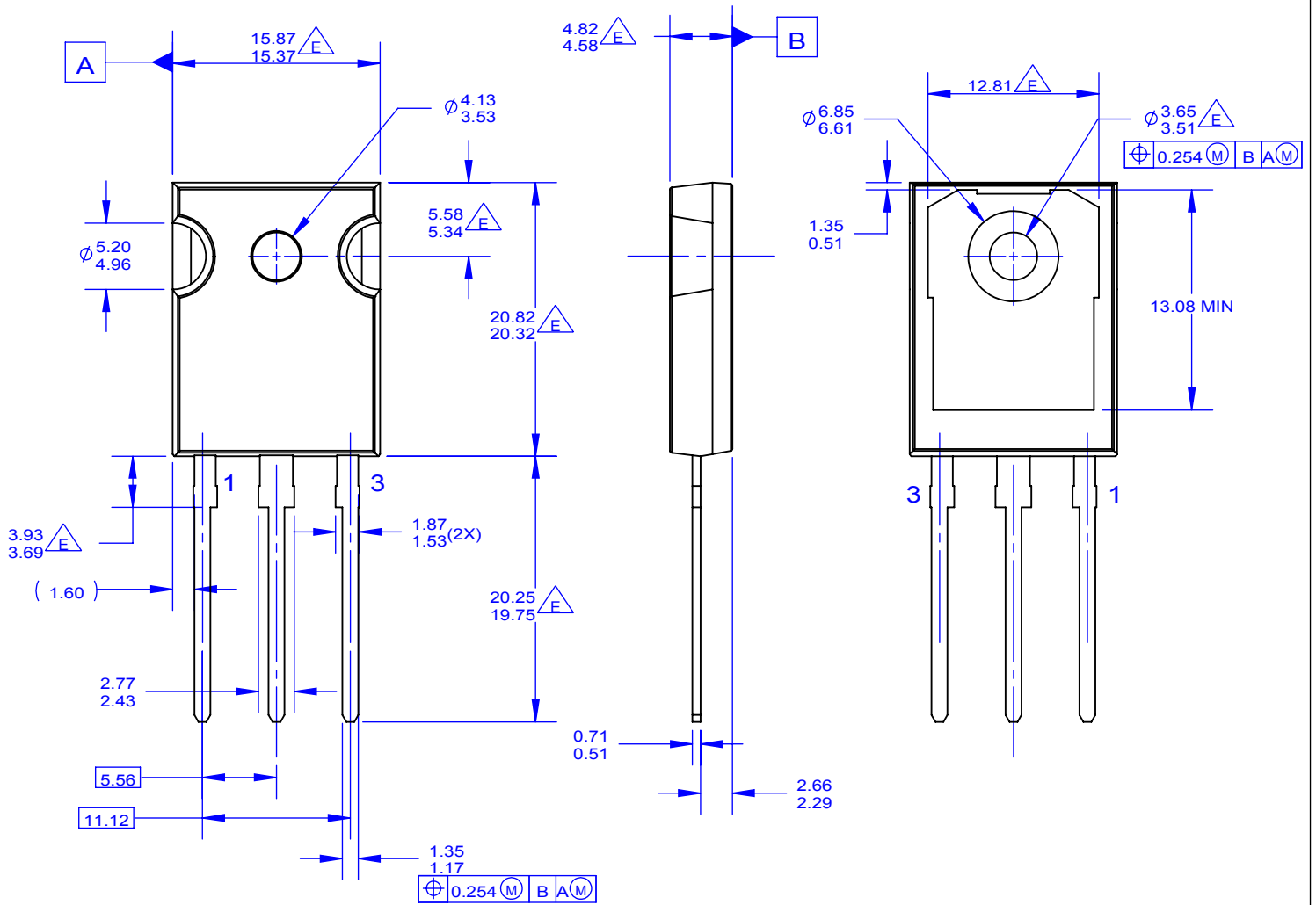
Figure 16. Resistive Switching Test Circuit & Waveforms



Figure 17. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 18. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED.

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