

# RQK0605JGDQA

Silicon N Channel MOS FET  
Power Switching

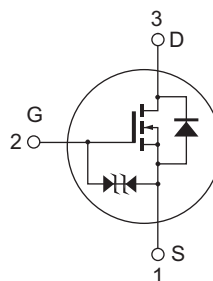
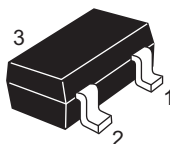
R07DS0309EJ0600  
Rev.6.00  
Jan 10, 2014

## Features

- Low on-resistance  
 $R_{DS(on)} = 82 \text{ m}\Omega \text{ typ}$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 1.5 \text{ A}$ )
- Low drive current
- High speed switching
- 4.5 V gate drive

## Outline

RENESAS Package code: PLSP0003ZB-A  
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Note: Marking is "JG".

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	3.1	A
Drain peak current	$I_{D(Pulse)}$ <sup>Note1</sup>	4.5	A
Body - drain diode reverse drain current	$I_{DR}$	3.1	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	0.8	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$

2. When using the glass epoxy board (FR-4:  $40 \times 40 \times 1 \text{ mm}$ )

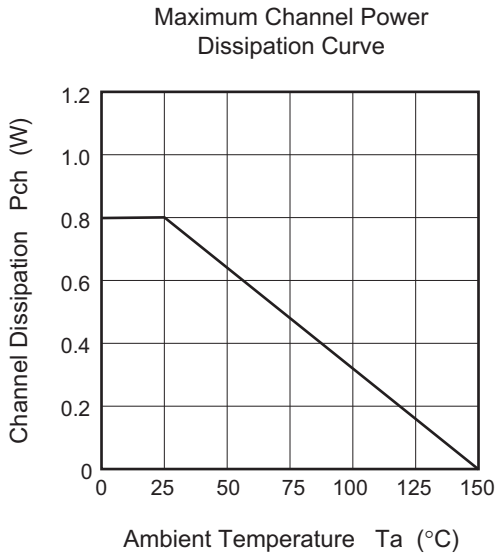
## Electrical Characteristics

(Ta = 25°C)

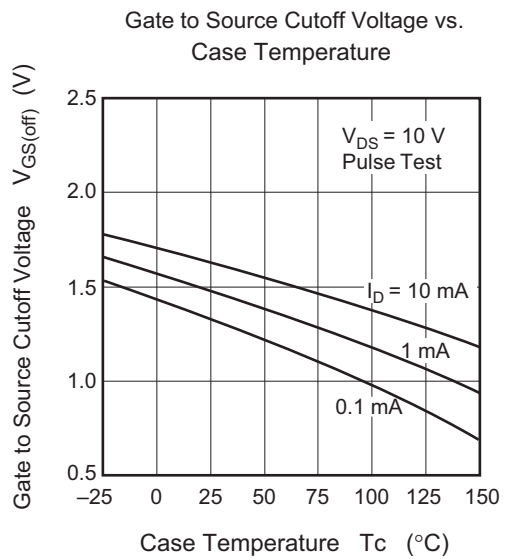
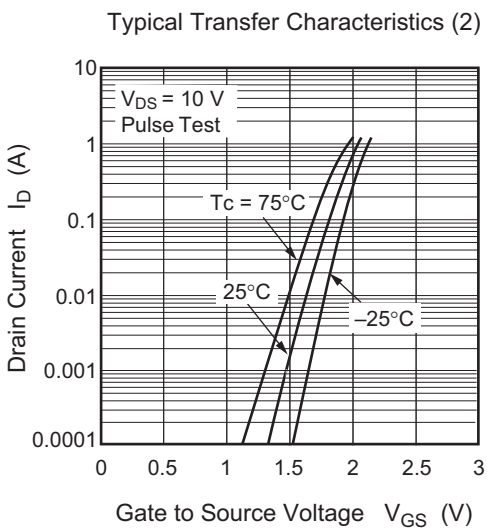
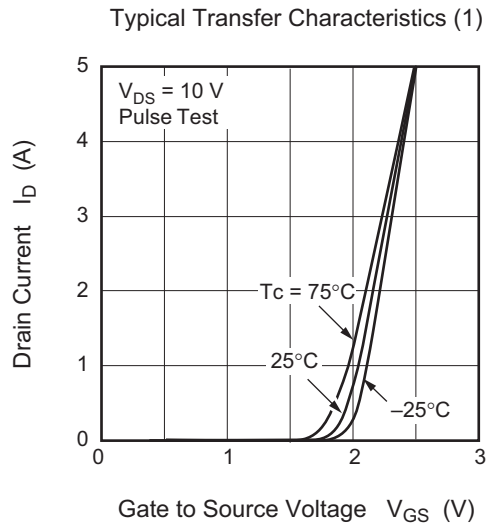
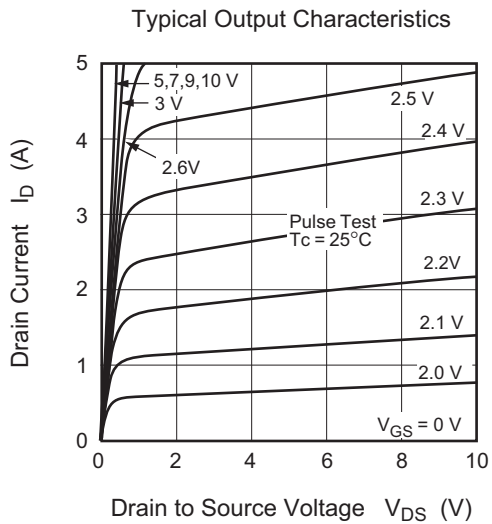
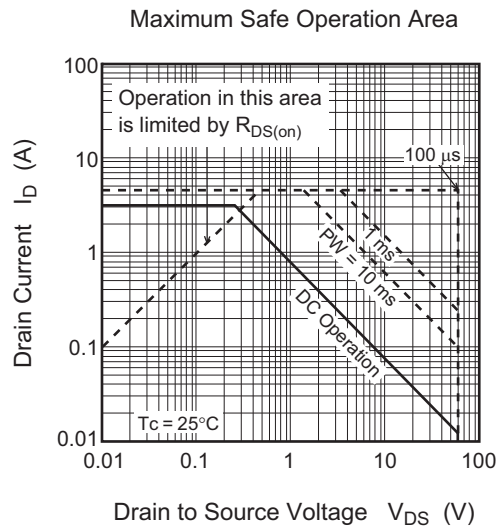
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Drain to source leak current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	82	103	$\text{m}\Omega$	$I_D = 1.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note3</sup>
	$R_{DS(on)}$	—	93	131	$\text{m}\Omega$	$I_D = 1.5 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	3.6	6	—	S	$I_D = 1.5 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	405	—	pF	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	58	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	23	—	pF	
Turn - on delay time	$t_{d(on)}$	—	14	—	ns	$I_D = 1 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_L = 10 \Omega$ , $R_g = 4.7 \Omega$
Rise time	$t_r$	—	43	—	ns	
Turn - off delay time	$t_{d(off)}$	—	43	—	ns	
Fall time	$t_f$	—	3.7	—	ns	
Total gate charge	$Q_g$	—	6.9	—	nC	$V_{DD} = 10 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 3.1 \text{ A}$
Gate to source charge	$Q_{gs}$	—	0.9	—	nC	
Gate to drain charge	$Q_{gd}$	—	0.8	—	nC	
Body - drain diode forward voltage	$V_{DF}$	—	0.8	—	V	$I_F = 1.5 \text{ A}$ , $V_{GS} = 0$ <sup>Note3</sup>

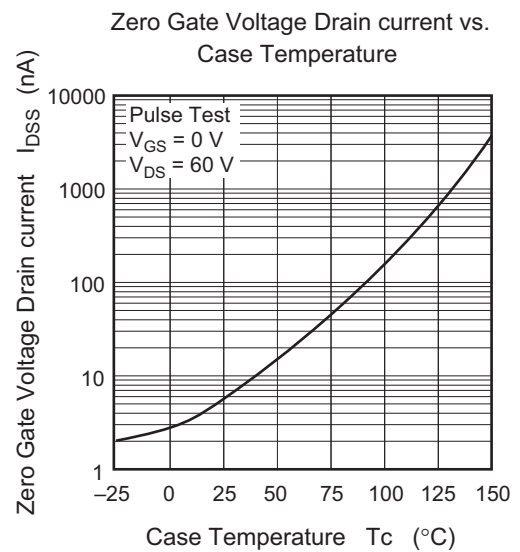
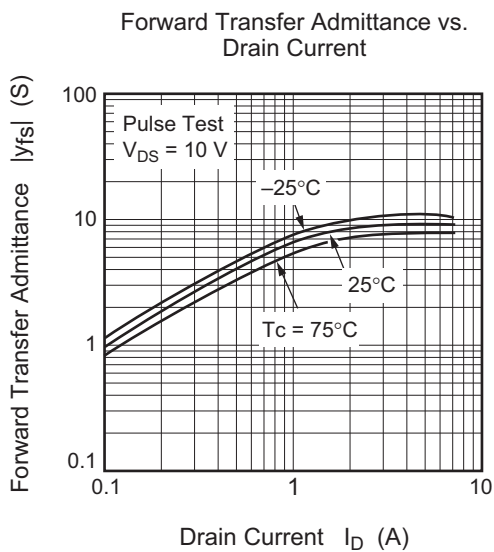
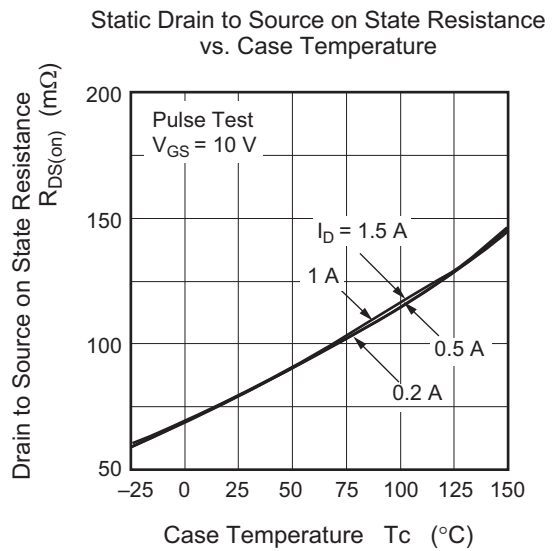
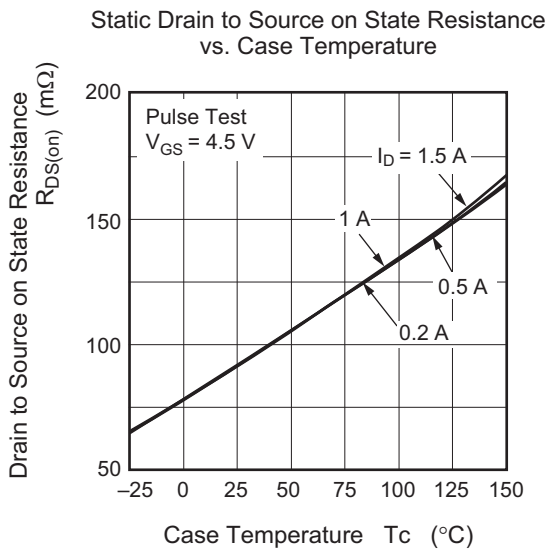
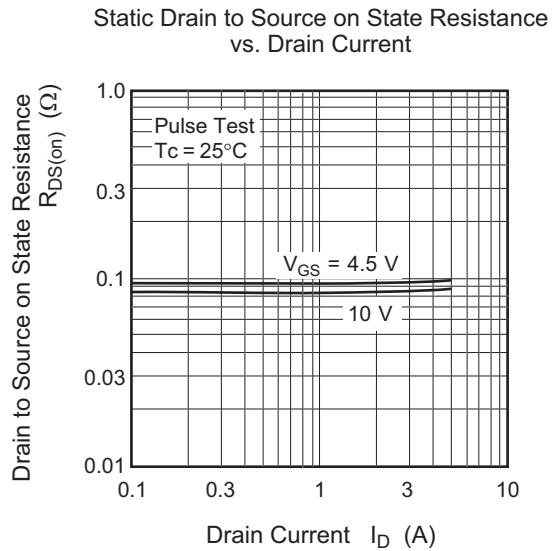
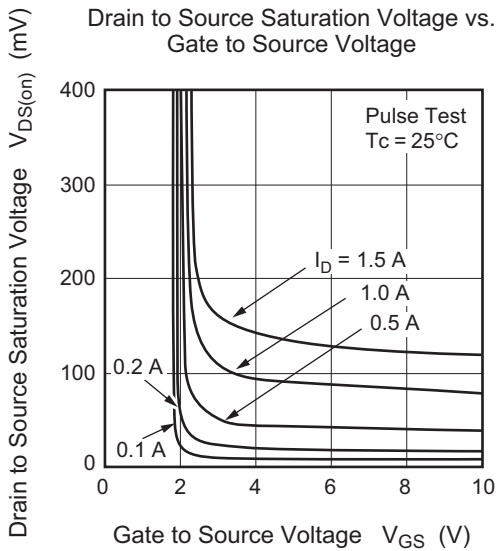
Notes: 3. Pulse test

### Main Characteristics

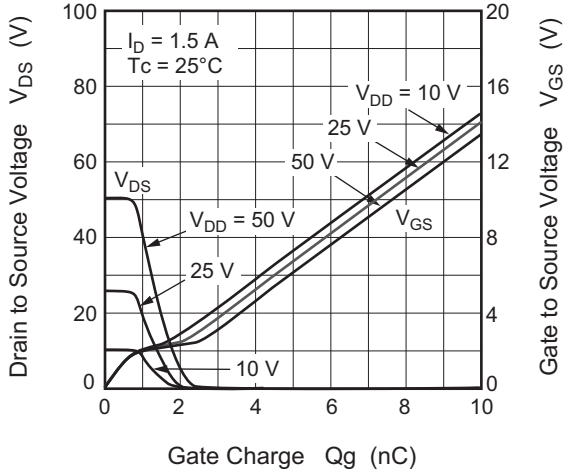


\*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

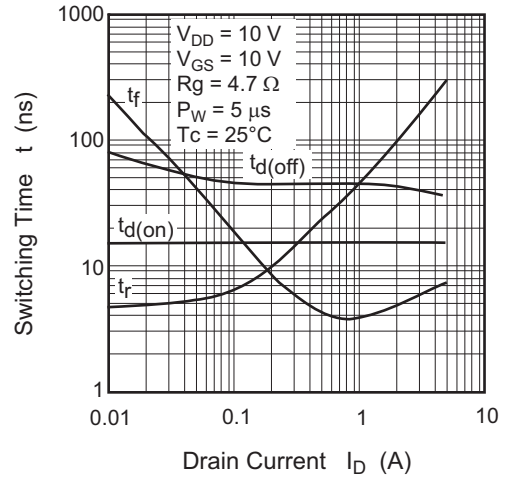




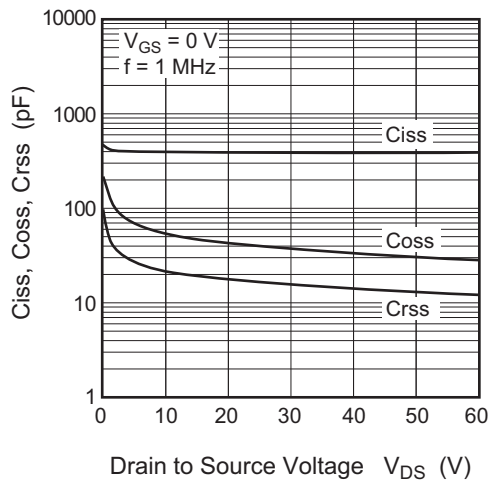
Dynamic Input Characteristics



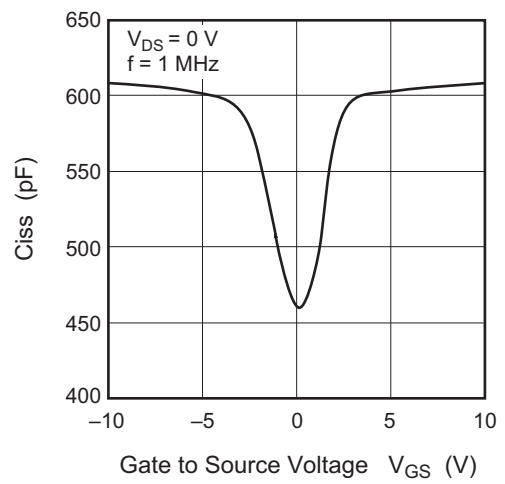
Switching Characteristics



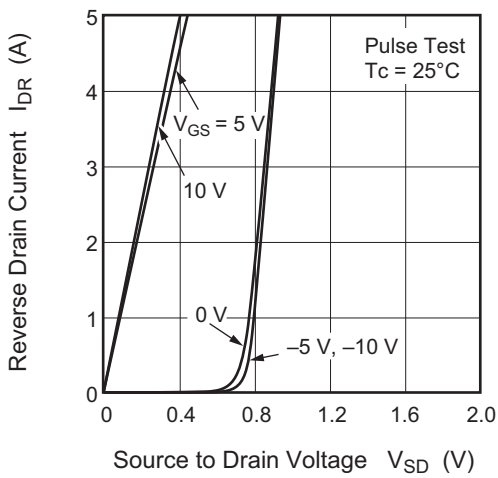
Typical Capacitance vs. Drain to Source Voltage



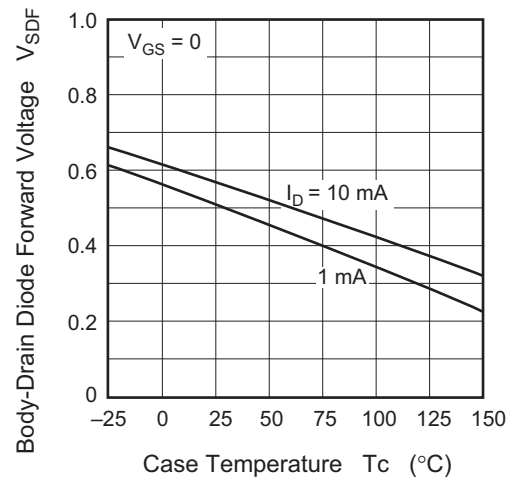
Input Capacitance vs. Gate to Source Voltage



Reverse Drain Current vs. Source to Drain Voltage

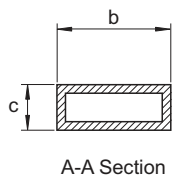
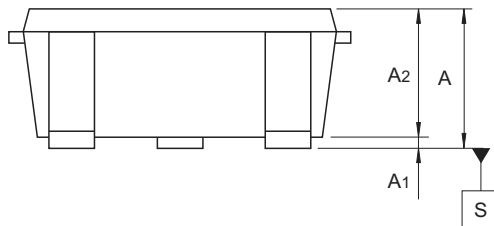
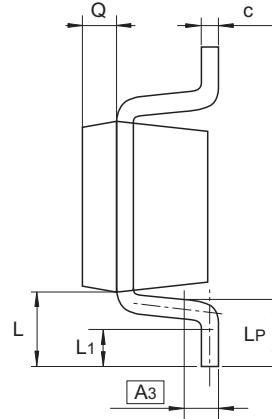
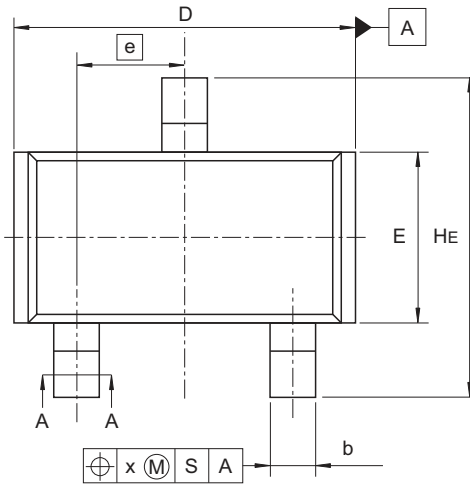


Body-Drain Diode Forward Voltage vs. Case Temperature



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
SC-59A	PLSP0003ZB-A	MPAK(T) / MPAK(T)V	0.011



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
A	1.0	—	1.3
A1	0	—	0.1
A2	1.0	1.1	1.2
A3	—	0.25	—
b	0.35	0.4	0.5
c	0.1	0.16	0.26
D	2.7	—	3.1
E	1.35	1.5	1.65
e	—	0.95	—
HE	2.2	2.8	3.0
L	0.35	—	0.75
L1	0.15	—	0.55
LP	0.25	—	0.65
x	—	—	0.05
Q	—	0.3	—

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### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQK0605JGDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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