

CHANGE NOTIFICATION

NOW PART OF



Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

June 20, 2017

Dear Sir/Madam:

PCN# 062017

Subject: Notification of Change to LTC3884 Die and Datasheet

Please be advised that Linear Technology Corporation has made enhancements to the LTC3884 product die to improve performance in the following areas:

- 1) Fix errata
- 2) Reduce power up times
- 3) Reduce the ADC update period
- 4) Improve on-chip EEPROM robustness
- 5) Support I²C PMBus thresholds compatible with bus power supplies as low as 1.8 volts
- 6) Reduced TON_MIN

The documented errata in the LTC3884 are eliminated. Refer to the following link for the current errata documents <http://cds.linear.com/docs/en/spec-notice/er3884f.pdf>.

T_{INIT}, the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 65ms to 35ms. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner. The ADC update period, T_{CONVERT}, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters. The above changes are shown on the attached pages of the marked up datasheet.

Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.

I²C thresholds are reduced in order to support PMBus communication with other ICs using I/O interface supplies as low as 1.8 volts. TON_MIN will be reduced from nominally 90ns to 60ns in to support large step down rations at relatively high switching frequencies. The new silicon can be identified by the MFR_SPECIAL_ID, PMBus command code 0xE7, with a value of 0x460* where * is a value of 8-F.

Confidential Statement

This change notice is for Analog Devices, Inc.'s customers only.
Distribution or notification to third parties is prohibited.

The die changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised product will have successfully completed 1000 hours burn-in before production release. Product built using the revised die will be shipped after August 20, 2017.

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will assume acceptance of this Change Notice by August 20, 2017.

Should you have any further questions, please feel free to contact your local Analog Devices Inc. sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@ANALOG.COM.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Notes 2, 3). $V_{IN} = 12\text{V}$, $\text{EXTV}_{CC} = 0\text{V}$, $V_{\text{RUNO},1} = 3.3\text{V}$, $f_{\text{SYNC}} = 500\text{kHz}$ (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	
Input Voltage							
V_{IN}	Input Voltage Range	(Note 11)	●	4.5	38	V	
I_Q	Input Voltage Supply Current	$V_{\text{RUNO},1} = 3.3\text{V}$ (Note 16) $V_{\text{RUNO},1} = 0\text{V}$ (Note 16)		25 23		mA mA	
V_{UVLO}	Undervoltage Lockout Threshold When $V_{IN} > 4.3\text{V}$	V_{INTVCC} Falling V_{INTVCC} Rising		3.55 3.90		V V	
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts		65 ³⁵		ms	
$t_{\text{OFF(MIN)}}$	Short Cycle Retry Time			120		ms	
Control Loop							
V_{OUTRL}	Full-Scale Voltage Range Set Point Accuracy (0.6V ~ 2.5V) Resolution LSB Step Size	$V_{\text{OUT_COMMAND}} = 2.75\text{V}$, $\text{MFR_PWM_MODE}[1] = 1$ (Notes 9, 10, 13)	● ●	2.7 -0.5	2.8 0.5	V % Bits mV	
V_{OUTRH}	Full-Scale Voltage Range Set Point Accuracy (0.6V ~ 5.0V) Resolution LSB Step Size	$V_{\text{OUT_COMMAND}} = 5.5\text{V}$, $\text{MFR_PWM_MODE}[1] = 0$ (Notes 9, 10, 13)	● ●	5.40 -0.5	5.60 0.5	V % Bits mV	
V_{LINREG}	Line Regulation	$6\text{V} < V_{IN} < 38\text{V}$	●		± 0.02	%/V	
V_{LOADREG}	Load Regulation	$\Delta V_{\text{ITH}} = 1.35\text{V} \sim 0.7\text{V}$ $\Delta V_{\text{ITH}} = 1.35\text{V} \sim 2\text{V}$	● ●	0.01 -0.01	0.1 -0.1	% %	
$I_{\text{SENSE0},1}$	Input Pin Bias Current	$0\text{V} \leq V_{\text{PIN}} \leq 5.5\text{V}$	●	± 1	± 3	μA	
$V_{\text{SENSEIN0},1}$	V_{SENSE} Input Resistance to GND	$0\text{V} \leq V_{\text{PIN}} \leq 5.5\text{V}$		50		k Ω	
V_{LIMIT}	N			12		Steps	
	$V_{\text{LIMIT_HIGH}}$	$\text{MFR_PWM_MODE}[7].[2]=0, 1, I_{\text{LIM}}[3:0]=1100, V_{\text{OUT}} \leq 3.5\text{V}$ (Note 15)	●	14.5	16.5	18.5	mV
	$V_{\text{LIMIT_LOW}}$	$\text{MFR_PWM_MODE}[7].[2]=0, 1, I_{\text{LIM}}[3:0]=0001, V_{\text{OUT}} \leq 3.5\text{V}$		9.5			mV
	V_{REV}	$\text{MFR_PWM_MODE}[7].[2]=0, 1, V_{\text{OUT}} \geq V_{\text{OV}}$		-7.5			mV
	$V_{\text{LIMIT_HIGH}}$	$\text{MFR_PWM_MODE}[7].[2]=1, 1, I_{\text{LIM}}[3:0]=1100, V_{\text{OUT}} \leq 3.5\text{V}$	●	27.0	29.5	31.0	mV
	$V_{\text{LIMIT_LOW}}$	$\text{MFR_PWM_MODE}[7].[2]=1, 1, I_{\text{LIM}}[3:0]=0001, V_{\text{OUT}} \leq 3.5\text{V}$		17.0			mV
	V_{REV}	$\text{MFR_PWM_MODE}[7].[2]=1, 1, V_{\text{OUT}} \geq V_{\text{OV}}$		-15			mV
	$V_{\text{LIMIT_HIGH}}$	$\text{MFR_PWM_MODE}[7].[2]=0, 0, I_{\text{LIM}}[3:0]=1100$	●	35	42	49	mV
	$V_{\text{LIMIT_LOW}}$	$\text{MFR_PWM_MODE}[7].[2]=0, 0, I_{\text{LIM}}[3:0]=0001$		25			mV
	V_{REV}	$\text{MFR_PWM_MODE}[7].[2]=0, 0, V_{\text{OUT}} \geq V_{\text{OV}}$		-18.8			mV
	$V_{\text{LIMIT_HIGH}}$	$\text{MFR_PWM_MODE}[7].[2]=1, 0, I_{\text{LIM}}[3:0]=1100$	●	67.5	74.5	81.5	mV
	$V_{\text{LIMIT_LOW}}$	$\text{MFR_PWM_MODE}[7].[2]=1, 0, I_{\text{LIM}}[3:0]=0001$		43.5			mV
	V_{REV}	$\text{MFR_PWM_MODE}[7].[2]=1, 0, V_{\text{OUT}} \geq V_{\text{OV}}$		-37.5			mV
$g_{\text{m0},1}$	Resolution Error Amplifier $g_{\text{m(MAX)}}$ Error Amplifier $g_{\text{m(MIN)}}$ LSB Step Size	$I_{\text{TH0},1} = 1.35\text{V}$, $\text{MFR_PWM_CONFIG}[7:5] = 0$ to 7		3 5.76 1 0.68			Bits mmho mmho mmho
$R_{\text{TH0},1}$	Resolution Compensation Resistor $R_{\text{TH(MAX)}}$ Compensation Resistor $R_{\text{TH(MIN)}}$	$\text{MFR_PWM_CONFIG}[4:0] = 0$ to 31 (See Figure 1)		5 70 0.5			Bits k Ω k Ω
Gate Drivers							
TG R_{UP}	TG Pull-Up $R_{\text{DS(ON)}}$	TG High		2.6		Ω	
TG R_{DOWN}	TG Pull-Down $R_{\text{DS(ON)}}$	TG Low		1.5		Ω	
BG R_{UP}	BG Pull-Up $R_{\text{DS(ON)}}$	BG High		2.4		Ω	

3884fb

For more information www.linear.com/LTC3884

5

LTC3884

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Notes 2, 3). $V_{IN} = 12\text{V}$, $\text{EXTV}_{CC} = 0\text{V}$, $V_{\text{RUN0,1}} = 3.3\text{V}$, $f_{\text{SYNC}} = 500\text{kHz}$ (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
BG R_{DOWN}	BG Pull-Down $R_{\text{DS(ON)}}$	BG Low		1.1		Ω
TG	TG Transition Time:	(Note 4)				
t_r	Rise Time	$C_{\text{LOAD}} = 3300\text{pF}$		30		ns
t_f	Fall Time	$C_{\text{LOAD}} = 3300\text{pF}$		30		ns
BG	BG Transition Time:	(Note 4)				
t_r	Rise Time	$C_{\text{LOAD}} = 3300\text{pF}$		30		ns
t_f	Fall Time	$C_{\text{LOAD}} = 3300\text{pF}$		30		ns
TG/BG, t_{1D}	Top Gate Off to Bottom Gate on Delay Time	(Note 4) $C_{\text{LOAD}} = 3300\text{pF}$ at Each Driver		30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate on Delay Time	(Note 4) $C_{\text{LOAD}} = 3300\text{pF}$ at Each Driver		30		ns
$t_{\text{ON(MIN)}}$	Minimum On-Time			90	60	ns

OV/UV Output Voltage Supervisor Channel 0/1

N	Resolution			9		Bits
$V_{\text{OUSTPSP_RL}}$	LSB Step Size	$\text{MFR_PWM_MODE}[1] = 1$ (Note 13)		5.6		mV
$V_{\text{OUSTPSP_RH}}$	LSB Step Size	$\text{MFR_PWM_MODE}[1] = 0$ (Note 13)		11.2		mV
$V_{\text{RANGE_RL}}$	Voltage Monitoring Range	$\text{MFR_PWM_MODE}[1] = 1$	0.5		2.7	V
$V_{\text{RANGE_RH}}$	Voltage Monitoring Range	$\text{MFR_PWM_MODE}[1] = 0$	1		5.6	V
$V_{\text{THAC0_RL}}$	Threshold Accuracy $1\text{V} < V_{\text{OUT}} < 2.5\text{V}$	$\text{MFR_PWM_MODE}[1] = 1$	●		± 1.5	%
$V_{\text{THAC1_RH}}$	Threshold Accuracy $2\text{V} < V_{\text{OUT}} < 5.5\text{V}$	$\text{MFR_PWM_MODE}[1] = 0$	●		± 1.5	%
t_{PROPOV}	OV Comparator Response Time	$V_{\text{OD}} = 10\%$ of Threshold			100	μs
t_{PROPUV}	UV Comparator Response Time	$V_{\text{OD}} = 10\%$ of Threshold			100	μs

 V_{IN} Voltage Supervisor

N	Resolution			9		Bits
V_{INSTP}	LSB Step Size			76		mV
V_{IN}	Full-Scale Voltage		4.5		38	V
V_{INTHACCM}	Threshold Accuracy $9\text{V} < V_{\text{IN}} < 38\text{V}$				± 3	%
	Threshold Accuracy $4.5\text{V} < V_{\text{IN}} \leq 9\text{V}$				± 6.0	%
t_{PROPVIN}	Comparator Response Time ($V_{\text{IN_ON}}$ and $V_{\text{IN_OFF}}$)	$V_{\text{OD}} = 10\%$ of threshold			100	μs

Output Voltage Readback

N	Resolution			16		Bits
V_{OUTSTP}	LSB Step Size			244		μV
$V_{\text{F/S}}$	Full-Scale Sense Voltage	$V_{\text{RUNn}} = 0$ (Note 8)		8		V
$V_{\text{OUT_TUE}}$	Total Unadjusted Error	$V_{\text{OUT}} > 0.6\text{V}$ (Note 8)	●	-0.5	0.5	%
V_{OS}	Zero-Code Offset Voltage				± 500	μV
t_{CONVERT}	Update Rate	(Note 6)		100	90	ms

 V_{IN} Voltage Readback

N	Resolution	(Note 5)		10		Bits
$V_{\text{F/S}}$	Full-Scale Input Voltage	(Note 11)		43		V
V_{INTUE}	Total Unadjusted Error	$V_{\text{IN}} > 4.5\text{V}$ (Note 8)	●		0.5 2	% %
t_{CONVERT}	Update Rate	(Note 6)		100	90	ms

3884tb

LTC3884

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Notes 2, 3). $V_{IN} = 12\text{V}$, $\text{EXTV}_{CC} = 0\text{V}$, $V_{\text{RUN0.1}} = 3.3\text{V}$, $f_{\text{SYNC}} = 500\text{kHz}$ (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS	
Output Current Readback							
N	Resolution	(Note 5)		10		Bits	
V_{IOUTSTP}	LSB Step Size	$0\text{V} \leq V_{\text{ISENSE}^+} - V_{\text{ISENSE}^-} < 16\text{mV}$ $16\text{mV} \leq V_{\text{ISENSE}^+} - V_{\text{ISENSE}^-} < 32\text{mV}$ $32\text{mV} \leq V_{\text{ISENSE}^+} - V_{\text{ISENSE}^-} < 64\text{mV}$ $64\text{mV} \leq V_{\text{ISENSE}^+} - V_{\text{ISENSE}^-} < 128\text{mV}$		15.63 31.25 62.5 125		μV μV μV μV	
$I_{\text{F/S}}$	Full-Scale Input Current	(Note 7) DCR or $R_{\text{ISENSE}} = 1\text{m}\Omega$		± 128		A	
$I_{\text{OUT_TUE}}$	Total Unadjusted Error	$V_{\text{ISENSE}^+} - V_{\text{ISENSE}^-} > 6\text{mV}$ (Note 8)	●		± 1.25	%	
V_{OS}	Zero-Code Offset Voltage				± 50	μV	
t_{CONVERT}	Update Rate	(Note 6)		100 90		ms	
Input Current Readback							
N	Resolution	(Note 5)		10		Bits	
V_{IINSTP}	LSB Step Size Full-Scale Range = 16mV LSB Step Size Full-Scale Range = 32mV LSB Step Size Full-Scale Range = 64mV	Gain = 8, $0\text{V} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} \leq 5\text{mV}$ Gain = 4, $0\text{V} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} \leq 20\text{mV}$ Gain = 2, $0\text{V} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} \leq 50\text{mV}$		15.26 30.52 61		μV μV μV	
$I_{\text{IN_TUE}}$	Total Unadjusted Error	Gain = 8, $2.5\text{mV} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} $, $V_{\text{IN}} = 8\text{V}$ (Note 8) Gain = 4, $4\text{mV} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} $, $V_{\text{IN}} = 8\text{V}$ (Note 8) Gain = 2, $6\text{mV} \leq V_{\text{IIN}^+} - V_{\text{IIN}^-} $, $V_{\text{IN}} = 8\text{V}$ (Note 8)	● ● ●		± 2 ± 1.3 ± 1.2	% % %	
V_{OS}	Zero-Code Offset Voltage				± 50	μV	
t_{CONVERT}	Update Rate	(Note 6)		100 90		ms	
Supply Current Readback							
N	Resolution	(Note 5)		10		Bits	
V_{CHIPSTP}	LSB Step Size Full-Scale Range = 256mV			244		μV	
I_{CHIPTUE}	Total Unadjusted Error	$ V_{\text{IIN}^+} - V_{\text{IN}} \leq 150\text{mV}$ (Note 19)	●		± 3	%	
t_{CONVERT}	Update Rate	(Note 6)		100 90		ms	
Temperature Readback (T0, T1)							
$T_{\text{RES_T}}$	Resolution			0.25		$^\circ\text{C}$	
$T0_TUE$	External Temperature Total Unadjusted Readback Error	$\text{TSNS0}, \text{TSNS1} \leq 1.85\text{V}$ (Note 8) $\text{MFR_PWM_MODE}_{[6]} = 0$ $\text{MFR_PWM_MODE}_{[6]} = 1$ (Note 14)		-3 -10	3 10	$^\circ\text{C}$ $^\circ\text{C}$	
$T1_TUE$	Internal TSNS TUE	$V_{\text{RUN0.1}} = 0.0$, $f_{\text{SYNC}} = 0\text{kHz}$ (Note 8)			± 1	$^\circ\text{C}$	
t_{CONVERT}	Update Rate	(Note 6)		100 90		ms	
INTV_{CC} Regulator/EXTV_{CC}							
V_{INTVCC}	Internal V_{CC} Voltage No Load	$6\text{V} \leq V_{\text{IN}} \leq 38\text{V}$		5.25	5.5	5.75	V
$V_{\text{LDO_INT}}$	INTV _{CC} Load Regulation	$I_{\text{CC}} = 0\text{mA}$ to 20mA , $6\text{V} \leq V_{\text{IN}} \leq 38\text{V}$		0.5	± 2		%
V_{EXTVCC}	EXTV _{CC} Switchover Voltage	$V_{\text{IN}} \geq 7\text{V}$, EXTV _{CC} Rising		4.5	4.7		V
$V_{\text{LDO_HYS}}$	EXTV _{CC} Hysteresis			290			mV
$V_{\text{LDO_EXT}}$	EXTV _{CC} Voltage Drop	$I_{\text{CC}} = 20\text{mA}$, $V_{\text{EXTVCC}} = 5.5\text{V}$		50	100		mV
$V_{\text{IN_THR}}$	V_{IN} Threshold to Enable EXTV _{CC} Switchover	V_{IN} Rising		7			V

3884fb

For more information www.linear.com/LTC3884

7

Confidential Statement
 This change notice is for Analog Devices, Inc.'s customers only.
 Distribution or notification to third parties is prohibited.

LTC3884

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$ (Notes 2, 3). $V_{IN} = 12\text{V}$, $\text{EXTV}_{CC} = 0\text{V}$, $V_{\text{RUN0,1}} = 3.3\text{V}$, $f_{\text{SYNC}} = 500\text{kHz}$ (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
V_{IN_THF}	V_{IN} Threshold to Disable EXTV_{CC} Switchover	V_{IN} Falling		6.5		V
V_{DD33} Regulator						
V_{DD33}	Internal V_{DD33} Voltage	$4.5\text{V} < V_{\text{INTV}_{CC}}$ or $4.8\text{V} < V_{\text{EXTV}_{CC}}$	3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	$V_{DD33} = \text{GND}$, $V_{IN} = \text{INTV}_{CC} = 4.5\text{V}$		100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold			3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold			3.1		V
V_{DD25} Regulator						
V_{DD25}	Internal V_{DD25} Voltage			2.5		V
I_{LIM}	V_{DD25} Current Limit	$V_{DD25} = \text{GND}$, $V_{IN} = \text{INTV}_{CC} = 4.5\text{V}$		80		mA
Oscillator and Phase-Locked Loop						
f_{RANGE}	PLL SYNC Range	Synchronized with Falling Edge of SYNC	●	200	1000	kHz
f_{OSC}	Oscillator Frequency Accuracy	Frequency Switch = 250.0 to 1000.0 kHz	●		± 7.5	%
$V_{TH(\text{SYNC})}$	SYNC Input Threshold	V_{SYNC} Falling V_{SYNC} Rising		1 1.5		V V
$V_{OL(\text{SYNC})}$	SYNC Low Output Voltage	$I_{\text{LOAD}} = 3\text{mA}$		0.2	0.4	V
$I_{\text{LEAK}(\text{SYNC})}$	SYNC Leakage Current in Slave Mode	$0\text{V} \leq V_{\text{PIN}} \leq 3.6\text{V}$			± 5	μA
$\theta_{\text{SYNC-}\theta 0}$	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG[2:0] = 0,2,3 MFR_PWM_CONFIG[2:0] = 5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 4,6		0 60 90 120		Deg Deg Deg Deg
$\theta_{\text{SYNC-}\theta 1}$	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG[2:0] = 3 MFR_PWM_CONFIG[2:0] = 0 MFR_PWM_CONFIG[2:0] = 2,4,5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 6		120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics						
Endurance	(Note 12)	$0^\circ\text{C} < T_J < 85^\circ\text{C}$ EEPROM Write Operations	●	10,000		Cycles
Retention	(Note 12)	$T_J < 125^\circ\text{C}$	●	10		Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, $0^\circ\text{C} < T_J < 85^\circ\text{C}$ During EEPROM Write Operation	●	440	4100	ms
Leakage Current SDA, SCL, ALERT, RUN						
I_{OL}	Input Leakage Current	$0\text{V} \leq V_{\text{PIN}} \leq 5.5\text{V}$	●		± 5	μA
Leakage Current FAULT_n, PGOOD_n						
I_{GL}	Input Leakage Current	$0\text{V} \leq V_{\text{PIN}} \leq 3.6\text{V}$	●		± 2	μA
Digital Inputs SCL, SDA, RUN_n, GPIO_n						
V_{IH}	Input High Threshold Voltage		●		≥ 1.35	V
V_{IL}	Input Low Threshold Voltage		●	1.4	0.8	V
V_{HYST}	Input Hysteresis	SCL, SDA		0.08		V
C_{PIN}	Input Capacitance				10	pF
Digital Input WP						
I_{PUWP}	Input Pull-Up Current	WP		10		μA
Open-Drain Outputs SCL, SDA, FAULT_n, ALERT, RUN_n, SHARE_CLK, PGOOD_n						
V_{OL}	Output Low Voltage	$I_{\text{SINK}} = 3\text{mA}$			0.4	V

3884tb

8

For more information www.linear.com/LTC3884