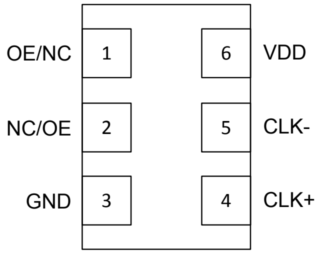
SILICON LABS

Si540 Data Sheet

Low Jitter Any-Frequency XO (125 fs), 0.2 to 800 MHz

The Si540 utilizes Silicon Laboratories' advanced 4th generation DSPLL technology to provide an ultra-low jitter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 800 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. The Si540 offers excellent reliability and frequency stability as well as guaranteed aging performance. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in a small, industry-standard 3.2×5 mm footprint, the Si540 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples one week after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si540 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. This process also guarantees 100% electrical testing of every device. The Si540 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.

Pin Assignments



(Top View)

Pin #	Descriptions
1, 2	*Selectable via ordering option* OE = Output enable; NC = No connect
3	GND = Ground
4	CLK+ = Clock output
5	CLK- = Complementary clock output
6	VDD = Power supply

KEY FEATURES

- Available with any frequency from 0.2 MHz to 800 MHz
- Very low jitter: 125 fs Typ RMS (12 kHz – 20 MHz)
- Excellent PSRR and supply noise immunity: –80 dBc Typ
- 3x tighter stability than SAW oscillators
- 3.3 V, 2.5 V and 1.8 V V_{DD} supply operation from the same part number
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 3.2×5 mm package footprint
- Any custom frequency available with 1 week lead times

APPLICATIONS

- 100G/400G OTN, coherent optics
- 10G/40G/100G optical ethernet
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Datacenter
- Test and measurement
- Clock and data recovery
- FPGA/ASIC clocking

1. Ordering Guide

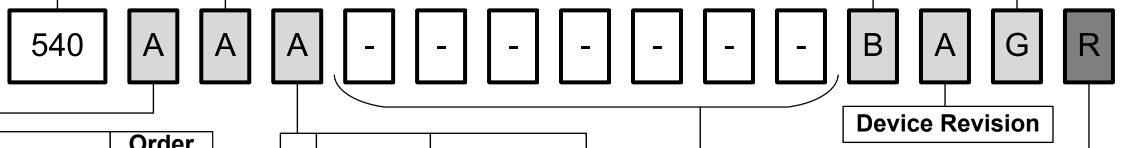
The Si540 XO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in less than two weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.

XO Series	Description
540	Single Frequency

	Temp Stability	Total Stability[2]
A	20 ppm	50 ppm

	Package
B	3.2x5 mm

	Temperature Grade
G	-40 to 85 °C



Signal Format	VDD Range	Order Option
LVPECL	2.5, 3.3 V	A
LVDS	1.8, 2.5, 3.3 V	B
CMOS	1.8, 2.5, 3.3 V	C
CML	1.8, 2.5, 3.3 V	D
HCSL	1.8, 2.5, 3.3 V	E
Dual CMOS (In-Phase)	1.8, 2.5, 3.3 V	F
Dual CMOS (Complementary)	1.8, 2.5, 3.3 V	G
Custom[1]	1.8, 2.5, 3.3 V	X

	OE Pin	OE Polarity
A	Pin 1	Active High
B	Pin 1	Active Low
C	Pin 2	Active High
D	Pin 2	Active Low

	Reel
R	Tape and Reel
<Blank>	Cut Tape

Frequency Code[3]	Description
Mxxxxxx	FCLK < 1 MHz
xMxxxxx	1 MHz ≤ FCLK < 10 MHz
xxMxxxx	10 MHz ≤ FCLK < 100 MHz
xxxMxxx	100 MHz ≤ FCLK < 800 MHz
xxxxxx	Custom code if FCLK > 6 digits

Notes:

1. Contact Silicon Labs for non-standard configurations.
2. Total stability includes temp stability, initial accuracy, load pulling, VDD variation, and 10 year aging at 70 °C.
3. For example: 156.25 MHz = 156M250; 25 MHz = 25M0000. Get custom frequency codes at www.silabs.com/oscillators.

2. Electrical Specifications

Table 2.1. Electrical Specifications

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		–40	—	85	ºC
Frequency Range	F_{CLK}	LVPECL, LVDS, CML	0.2	—	800	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	V_{DD}	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	I_{DD}	LVPECL (output enabled)	—	96	—	mA
		LVDS/CML (output enabled)	—	85	—	mA
		HCSL (output enabled)	—	90	—	mA
		CMOS (output enabled)	—	72	—	mA
		Dual CMOS (output enabled)	—	82	—	mA
		Tristate Hi-Z (output disabled)	—	68	—	mA
Temperature Stability		Frequency stability Grade A	–20	—	20	ppm
Total Stability[1]	F_{STAB}	Frequency stability Grade A	–50	—	50	ppm
Rise/Fall Time (20% to 80% V_{DD})	T_R/T_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS (C_L = 15 pF)	0.8	—	2.5	ns
		HCSL, F_{CLK} >50 MHz	—	—	700	ps
Phase Jitter (RMS), 12 kHz to 20 MHz, $F_{CLK} \geq$ 100 MHz	ϕ_J	Differential Formats	—	125	200	fs
		CMOS, Dual CMOS	—	125	300	fs
Duty Cycle	D_C	All formats	45	—	55	%
Output Enable (OE)[2]	V_{IH}		0.75 × V_{DD}	—	—	V
	V_{IL}		—	—	0.5	V
	T_D	Output Disable Time	—	—	3	µs
	T_E	Output Enable Time	—	—	20	µs
Powerup Time	t_{OSC}	Time until output frequency (F_{CLK}) within spec	—	—	10	ms
LVPECL Output Option[3]	V_{OC}	Mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_O	Swing (diff)	1.1	—	1.9	V_{PP}
LVDS Output Option[4]	V_{OC}	Mid-level	1.125	1.20	1.275	V
	V_O	Swing (diff)	0.5	0.7	0.9	V_{PP}

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Option[5]	V_{OH}	Output voltage high	TBD	700	850	mV
	V_{OL}	Output voltage low	–150	0	150	mV
	V_{SE}	Swing (single-ended)	660	700	850	mV
	V_C	Crossing voltage	250	350	550	mV
CMOS Output Option	V_{OH}		$0.90 \times V_{DD}$	—	—	V
	V_{OL}		—	—	$0.10 \times V_{DD}$	V

Notes:

1. Total Stability includes ±20 ppm temperature stability, initial accuracy, load pulling, VDD variation, and aging for 10 yrs at 70 ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high. Includes a 50 kΩ pull-down to GND for OE active low.
3. 50 Ω to V_{DD} – 2.0 V.
4. R_{term} = 100 Ω (differential).
5. 50 Ω to GND.

Table 2.2. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL)	1
Contact Pads	Gold over Nickel

Note:

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx.

Table 2.3. Thermal Conditions

Package	Symbol	Test Condition	Value	Unit
3.2×5 mm 6-pin CLCC	Θ_{JA}	Still air	TBD	ºC/W
	Θ_{JB}	Still air	TBD	ºC/W
	Θ_{JC}	Still air	TBD	ºC/W

Table 2.4. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	T_{AMAX}	95	ºC
Storage Temperature	T_S	–55 to 125	ºC
Supply Voltage	V_{DD}	–0.5 to 3.8	ºC
Input Voltage	V_{IN}	0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature[2]	T_{PEAK}	260	ºC
Solder Time at T_{PEAK}[2]	T_P	20–40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase output signals. This feature enables replacement of multiple XOs with a single Si540 device.

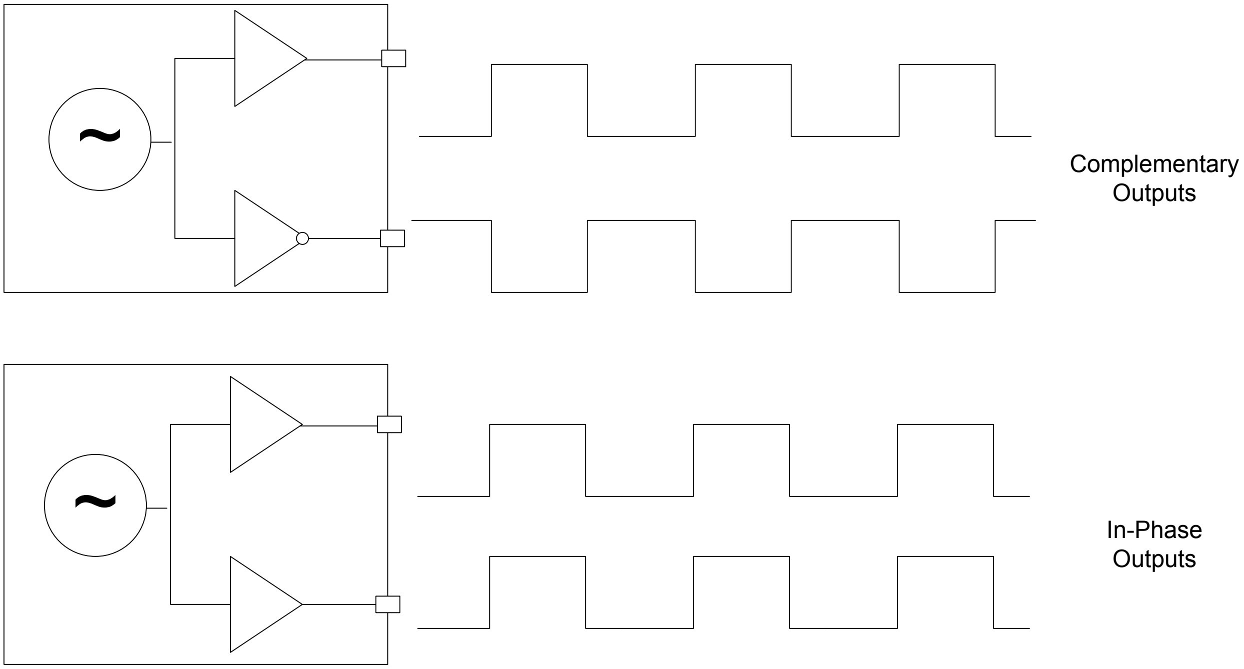


Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

4. Package Outline

The figure below illustrates the package details for the 3.2 × 5 mm Si540. The table below lists the values for the dimensions shown in the illustration.

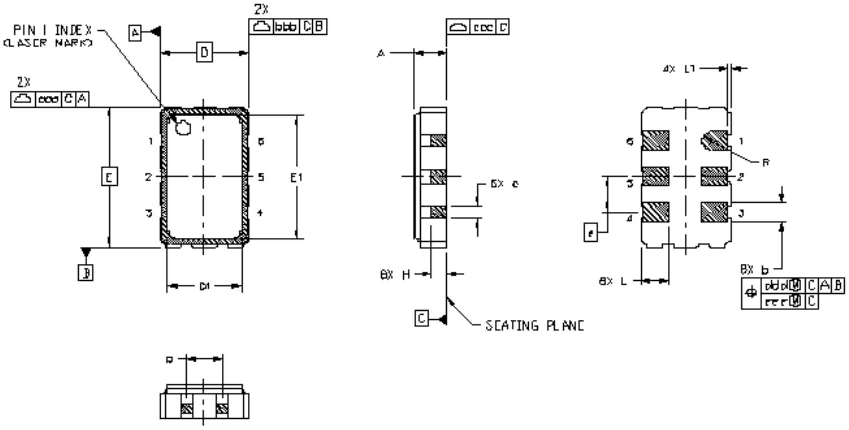


Figure 4.1. Si540 Outline Diagram

Table 4.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.06	1.17	1.28
b	0.54	0.64	0.74
c	0.35	0.45	0.55
D	3.20 BSC		
D1	2.55	2.60	2.65
e	1.27 BSC		
E	5.00 BSC		
E1	4.35	4.40	4.45
H	0.45	0.55	0.65
L	0.90	1.00	1.10
L1	0.05	0.10	0.15
p	1.17	1.27	1.37
R	0.32 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5. PCB Land Pattern

The figure below illustrates the 3.2 × 5.0 mm PCB land pattern for the Si540. The table below lists the values for the dimensions shown in the illustration.

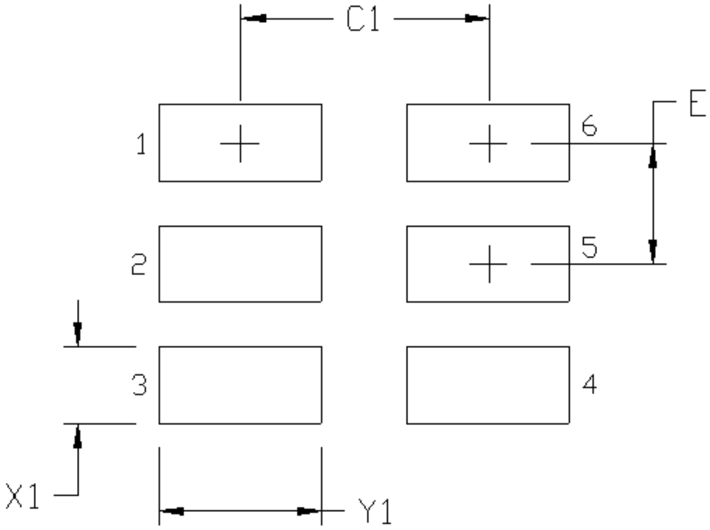


Figure 5.1. Si540 PCB Land Pattern

Table 5.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.60
E	1.27
X1	0.80
Y1	1.70

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. Top Marking

The figure below illustrates the mark specification for the Si540. The table below lists the line information.

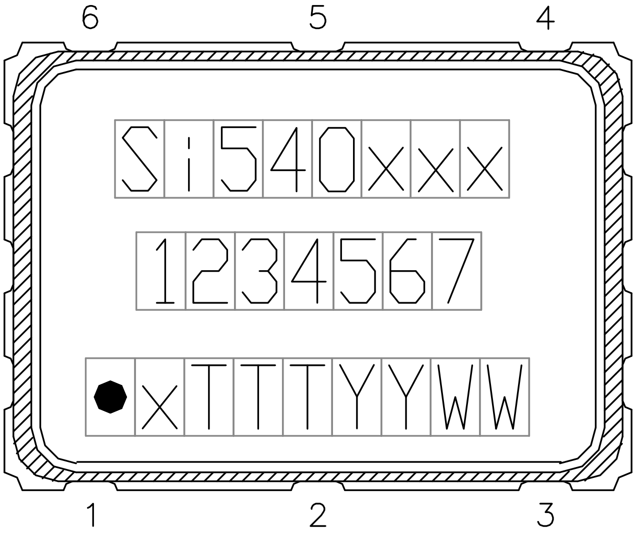


Figure 6.1. Mark Specification

Table 6.1. Si540 Top Mark Description

Line	Position	Description
1	1–8	"Si540", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si540AAA)
2	1–7	Frequency Code (e.g. 100M000 or 6-digit custom code as described in the Ordering Guide)
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	x = Product Revision (A)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

7. Revision History

7.1 Revision 0.3

April 6, 2017

- Initial release.

ClockBuilder Pro

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