

Features

- CMOS 3.0V Core
- Serial Peripheral Interface (SPI) with Multi-I/O
 - SPI Clock polarity and phase modes 0 and 3
 - Double Data Rate (DDR) option
 - Extended Addressing: 32-bit address
 - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
 - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- READ Commands
 - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
 - AutoBoot – power up or reset and execute a Normal or Quad read command automatically at a preselected address
 - Common Flash Interface (CFI) data for configuration information
- Programming (1.5 Mbytes/s)
 - 512-byte Page Programming buffer
 - Quad-Input Page Programming (QPP) for slow clock systems
- Erase (0.5 Mbytes/s)
 - Uniform 256-kbyte sectors
- Cycling Endurance
 - 100,000 Program-Erase Cycles, minimum
- Data Retention
 - 20 Year Data Retention, minimum

Security Features

- One Time Program (OTP) array of 2048 bytes
- Block Protection
 - Status Register bits to control protection against program or erase of a contiguous range of sectors.
 - Hardware and software control options
 - Advanced Sector Protection (ASP)
 - Individual sector protection controlled by boot code or password
- Cypress® 65 nm MirrorBit® Technology with Eclipse™ Architecture
- Core Supply Voltage: 2.7V to 3.6V
- I/O Supply Voltage: 1.65V to 3.6V
- Temperature Range / Grade:
 - Industrial (–40 °C to +85 °C)
 - Industrial Plus (–40 °C to +105 °C)
 - Automotive, AEC-Q100 Grade 3 (–40 °C to +85 °C)
 - Automotive, AEC-Q100 Grade 2 (–40 °C to +105 °C)
 - Automotive, AEC-Q100 Grade 1 (–40 °C to +125 °C)
- Packages (all Pb-free)
 - 16-lead SOIC (300 mils)
 - BGA-24, 8 × 6 mm
 - 5 × 5 ball (ZSA024) footprint

General Description

This document contains information for the S70FL01GS device, which is a dual die stack of two S25FL512S die. For detailed specifications, refer to the discrete die datasheet provided in the [Affected Documents/Related Documents](#) table.

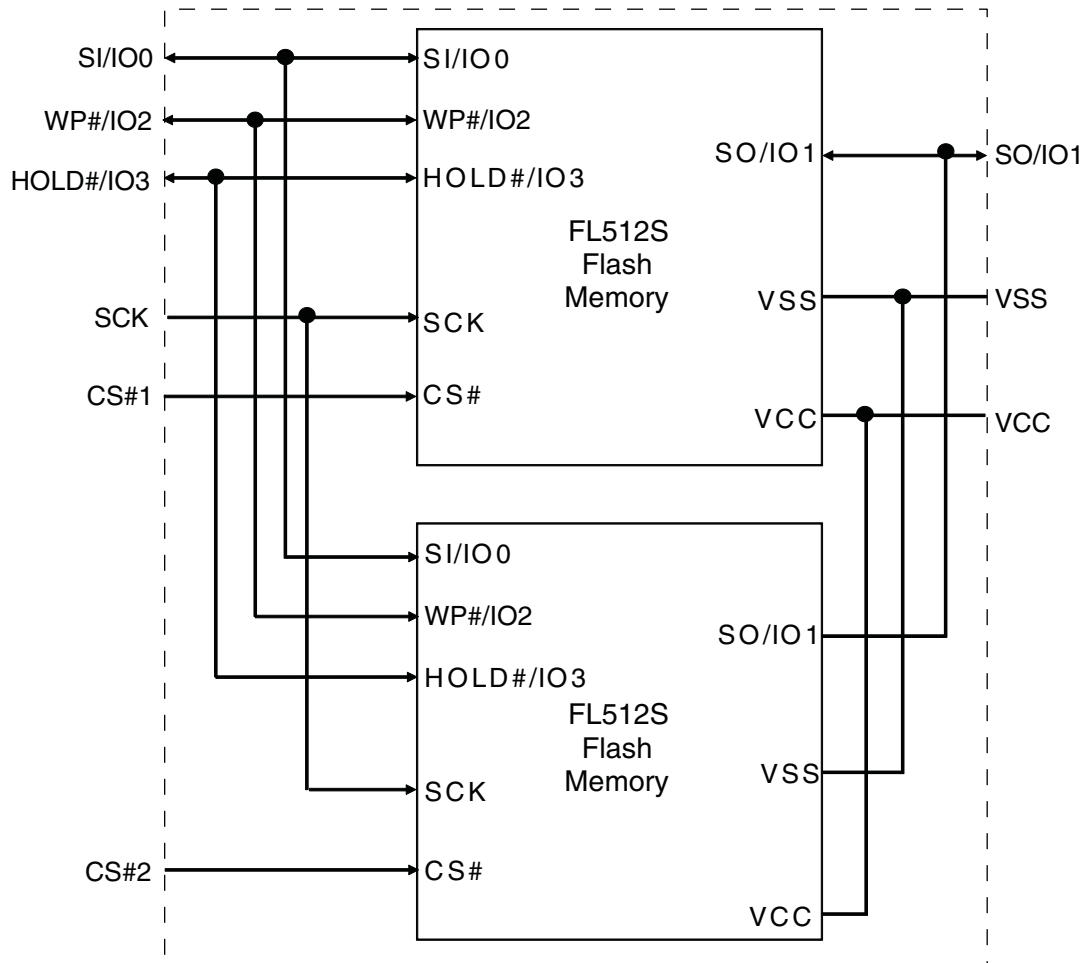
Affected Documents/Related Documents

Document Title	Publication Number
S25FL512S 512 Mbit (64 Mbyte) 3.0V SPI Flash Memory Datasheet	001-98284

Contents

1. Block Diagram	3	10. SDR AC Characteristics	10
2. Connection Diagrams	4	10.1 DDR AC Characteristics	11
3. Input/Output Summary	5	10.2 Capacitance Characteristics	11
4. Device Operations	6	11. Ordering Information	12
4.1 Programming	6	11.1 Valid Combinations — Standard	13
4.2 Simultaneous Die Operation	6	11.2 Valid Combinations — Automotive Grade /	
4.3 Sequential Reads	6	AEC-Q100	13
4.4 Sector/Bulk Erase	6	12. Other Resources	14
4.5 Status Registers	6	12.1 Cypress Flash Memory Roadmap	14
4.6 Configuration Register	6	12.2 Links to Software	14
4.7 Bank Address Register	6	12.3 Links to Application Notes	14
4.8 Security and DDR Registers	6	13. Physical Diagram	15
4.9 Block Protection	6	13.1 SOIC 16 Lead, 300-mil Body Width	15
5. Read Identification (RDID)	7	13.2 24-Ball BGA 8 x 6 mm (ZSA024)	16
6. RESET#	7	14. Revision History	17
7. Versatile I/O Power Supply (V_{IO})	7	Sales, Solutions, and Legal Information	19
8. DC Characteristics	8	Worldwide Sales and Design Support	19
9. AC Test Conditions	9	Products	19
		PSoC® Solutions	19
		Cypress Developer Community	19
		Technical Support	19

1. Block Diagram



2. Connection Diagrams

Figure 1. 16-Pin Plastic Small Outline Package (SO)

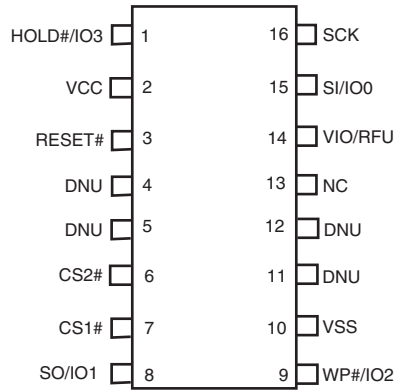
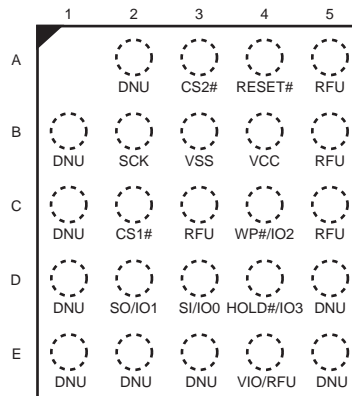


Figure 2. 24-Ball BGA, 5 x 5 Ball Footprint (ZSA024), Top View



Note:

1. V_{IO} is not supported in the S70FL01GS device and is RFU. Refer to [Section 7](#) for more details.

3. Input/Output Summary

Table 2. Signal List

Signal Name	Type	Description
RESET#	Input	Hardware Reset: Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	Serial Clock.
CS1#	Input	Chip Select. FL512S #1.
CS2#	Input	Chip Select. FL512S #2.
SI / IO0	I/O	Serial Input for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	Serial Output for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	Write Protect when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	Hold (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V _{CC}	Supply	Core Power Supply.
V _{IO}	Supply	Versatile I/O Power Supply. Note: V _{IO} is not supported in the S70FL01GS device. Refer to Section 7 . for more details.
V _{SS}	Supply	Ground.
NC	Unused	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V _{CC} .
RFU	Reserved	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V _{IL} . The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V _{SS} . Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

4. Device Operations

4.1 Programming

Each Flash die must be programmed independently due to the nature of the dual die stack.

4.2 Simultaneous Die Operation

The user may only access one Flash die of the dual die stack at a time via its respective Chip Select.

4.3 Sequential Reads

Sequential reads are not supported across the end of the first Flash die to the beginning of the second. If the user desires to sequentially read across the two die, data must be read out of the first die via CS1# and then read out of the second die via CS2#.

4.4 Sector/Bulk Erase

A sector erase command must be issued for sectors in each Flash die separately. Full device Bulk Erase via a single command is not supported due to the nature of the dual die stack. A Bulk Erase command must be issued for each die.

4.5 Status Registers

Each Flash die of the dual die stack is managed by its own Status Registers. Reads and updates to the Status Registers must be managed separately. It is recommended that Status Register control bit settings of each die are kept identical to maintain consistency when switching between die.

4.6 Configuration Register

Each Flash die of the dual die stack is managed by its own Configuration Register. Updates to the Configuration Register control bits must be managed separately. It is recommended that Configuration Register control bit settings of each die are kept identical to maintain consistency when switching between die.

4.7 Bank Address Register

It is recommended that the Bank Address Register bit settings of each die are kept identical to maintain consistency when switching between die.

4.8 Security and DDR Registers

It is recommended that the bit settings for ASP Register, Password Register, PPB Lock Register, PPB Access Register, DYB Access Register, and DDR Data Learning Register in each die are kept identical to maintain consistency when switching between die.

4.9 Block Protection

Each Flash die of the dual die stack will maintain its own Block Protection. Updates to the TBPROT and BPNV bits of each die must be managed separately. By default, each die is configured to be protected starting at the top (highest address) of each array, but no address range is protected. It is recommended that the Block Protection settings of each die are kept identical to maintain consistency when switching between die. In addition, any update to the FREEZE bit must be managed separately for each die. If the FREEZE bit is set to a logic 1, it cannot be cleared to a logic 0 until a power-on-reset is executed on each die that has the FREEZE bit set to 1.

5. Read Identification (RDID)

The Read Identification (RDID) command outputs the one-byte manufacturer identification, followed by the two-byte device identification and the bytes for the Common Flash Interface (CFI) tables. Each die of the FL01GS dual die stack will have identical identification data as the FL512S die, with the exception of the CFI data at byte 27h, as shown in [Table 3](#).

Table 3. Product Group CFI Device Geometry Definition

Byte	Data	Description
27h	1Bh	Device Size = 2^N byte

6. RESET#

Note that the hardware RESET# input (pin 3 on the 16-pin SO package and ball A4 on the 5x5 BGA package) is bonded out and active for the S70FL01GS device. For applications that do NOT require use of the RESET# pin, it is recommended to not use RESET# for PCB routing channels that would cause the RESET# signal to be asserted Low (V_{IL}). Doing so will cause the device to reset to standby state. The RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used.

7. Versatile I/O Power Supply (V_{IO})

Note that the Versatile I/O (V_{IO}) power supply (pin 14 on the 16-pin SO package and ball E4 on the 5x5 BGA package) is not supported, and pin 14 and ball E4 are RFU (Reserved for Future Use) in the standard configuration of the S70FL01GS device. Contact your local sales office to confirm availability with the V_{IO} feature enabled.

8. DC Characteristics

This section summarizes the DC Characteristics of the device.

Table 4. DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ (1)	Max	Unit
V_{IL}	Input Low Voltage	–	-0.5	–	$0.2 \times V_{CC}$	V
V_{IH}	Input High Voltage	–	$0.7 \times V_{CC}$	–	$V_{CC} + 0.4$	V
V_{OL}	Output Low Voltage	$I_{OL} = 1.6 \text{ mA}$, $V_{CC} = V_{CC \text{ min}}$	–	–	$0.15 \times V_{CC}$	V
V_{OH}	Output High Voltage	$I_{OH} = -0.1 \text{ mA}$	$0.85 \times V_{CC}$	–		V
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC \text{ Max}}$, $V_{IN} = V_{IH}$ or V_{IL}	–	–	± 4	μA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC \text{ Max}}$, $V_{IN} = V_{IH}$ or V_{IL}	–	–	± 4	μA
I_{CC1}	Active Power Supply Current (READ)	Serial SDR @ 50 MHz Serial SDR @ 133 MHz Quad SDR @ 80 MHz Quad SDR @ 104 MHz Quad DDR @ 66 MHz Quad DDR @ 80 MHz Outputs unconnected during read data return (2)	–	–	18 36 50 61 75 90	mA
I_{CC2}	Active Power Supply Current (Page Program)	$CS\# = V_{CC}$	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR)	$CS\# = V_{CC}$	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	$CS\# = V_{CC}$	–	–	100	mA
I_{CC5}	Active Power Supply Current (BE) (3)	$CS\# = V_{CC}$	–	–	200	mA
I_{SB} (Industrial)	Standby Current	RESET#, $CS\# = V_{CC}$; SI, SCK = V_{CC} or V_{SS} , Industrial Temp	–	140	200	μA
I_{SB} (Industrial Plus)	Standby Current	RESET#, $CS\# = V_{CC}$; SI, SCK = V_{CC} or V_{SS} , Industrial Plus Temp	–	140	600	μA

Notes:

1. Typical values are at $T_{AI} = 25^\circ\text{C}$ and $V_{CC} = 3\text{V}$.
2. Output switching current is not included.
3. Bulk Erase current is for both die erasing simultaneously.

9. AC Test Conditions

Figure 3. Input, Output, and Timing Reference Levels

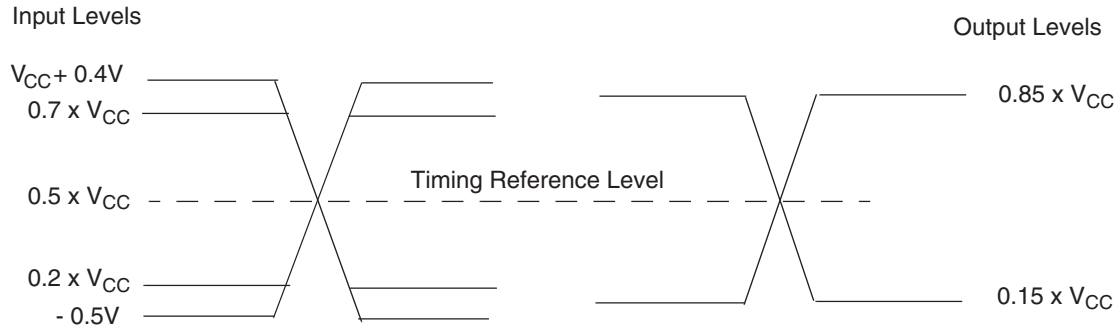


Figure 4. Test Setup

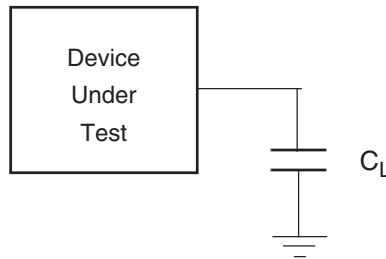


Table 5. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30 15 (4)		pF
	Input Rise and Fall Times		2.4	ns
	Input Pulse Voltage	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$		V
	Input Timing Ref Voltage	$0.5 \times V_{CC}$		V
	Output Timing Ref Voltage	$0.5 \times V_{CC}$		V

Notes:

1. Output High-Z is defined as the point where data is no longer driven.
2. Input slew rate: 1.5 V/ns.
3. AC characteristics tables assume clock and data signals have the same slew rate (slope).
4. DDR Operation.

10. SDR AC Characteristics

Table 6. SDR AC Characteristics (Single Die Package, $V_{CC} = 2.7V$ to $3.6V$)

Symbol	Parameter	Min	Typ	Max	Unit
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	DC	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for single commands (4)	DC	–	133	MHz
$F_{SCK, C}$	SCK Clock Frequency for the following dual and quad commands: DOR, 4DOR, QOR, 4QOR, DIOR, 4DIOR, QIOR, 4QIOR	DC	–	104	MHz
$F_{SCK, QPP}$	SCK Clock Frequency for the QPP, 4QPP commands	DC	–	80	MHz
P_{SCK}	SCK Clock Period	$1/F_{SCK}$	–	∞	
t_{WH}, t_{CH}	Clock High Time (5)	$45\% P_{SCK}$	–	–	ns
t_{WL}, t_{CL}	Clock Low Time (5)	$45\% P_{SCK}$	–	–	ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	–	V/ns
t_{CS} (7)	CS# High Time (Read Instructions) CS# High Time (Program/Erase)	10 50	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	3000 (6)	ns
t_{SU}	Data in Setup Time	1.5	–	–	ns
t_{HD}	Data in Hold Time	2	–	–	ns
t_V	Clock Low to Output Valid	–	–	8.0 (2) 7.65 (3) 6.5 (4)	ns
t_{HO}	Output Hold Time	2	–	–	ns
t_{DIS}	Output Disable Time	0	–	8	ns
t_{WPS}	WP# Setup Time	20 (1)	–	–	ns
t_{WPH}	WP# Hold Time	100 (1)	–	–	ns
t_{HLCH}	HOLD# Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHH}	HOLD# Active Hold Time (relative to SCK)	3	–	–	ns
t_{HHCH}	HOLD# Non-Active Setup Time (relative to SCK)	3	–	–	ns
t_{CHHL}	HOLD# Non-Active Hold Time (relative to SCK)	3	–	–	ns
t_{HZ}	HOLD# Enable to Output Invalid	–	–	8	ns
t_{LZ}	HOLD# Disable to Output Valid	–	–	8	ns

Notes:

1. Only applicable as a constraint for WRR instruction when SRWD is set to a 1.
2. Full V_{CC} range (2.7 - 3.6V) and $CL = 30$ pF.
3. Regulated V_{CC} range (3.0 - 3.6V) and $CL = 30$ pF.
4. Regulated V_{CC} range (3.0 - 3.6V) and $CL = 15$ pF.
5. $\pm 10\%$ duty cycle is supported for frequencies ≤ 50 MHz.
6. Maximum value only applies during Program/Erase Suspend/Resume commands.
7. When switching between die, a minimum time of t_{CS} must be kept between the rising edge of one chip select and the falling edge of the other for operations and data to be valid.

10.1 DDR AC Characteristics

Table 7. DDR AC Characteristics 66 MHz and 80 MHz Operation

Symbol	Parameter	66 MHz			80 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
$F_{SCK, R}$	SCK Clock Frequency for DDR READ instruction	DC	–	66	DC	–	80	MHz
$P_{SCK, R}$	SCK Clock Period for DDR READ instruction	15	–	∞	12.5	–	∞	ns
t_{WH}, t_{CH}	Clock High Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{WL}, t_{CL}	Clock Low Time	45% P_{SCK}	–	–	45% P_{SCK}	–	–	ns
t_{CS}	CS# High Time (Read Instructions)	10	–	–	10	–	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	–	3	–	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	3	–	–	3	–	–	ns
t_{SU}	IO in Setup Time	2	–	3000 (2)	1.5	–	3000 (2)	ns
t_{HD}	IO in Hold Time	2	–	–	1.5	–	–	ns
t_V	Clock Low to Output Valid	0	–	6.5 (1)	–	–	6.5 (1)	ns
t_{HO}	Output Hold Time	1.5	–	–	1.5	–	–	ns
t_{DIS}	Output Disable Time	–	–	8	–	–	8	ns
t_{LZ}	Clock to Output Low Impedance	0	–	8	0	–	8	ns
t_{IO_skew}	First IO to last IO data valid time	–	–	600	–	–	600	ps

Notes:

1. Regulated V_{CC} range (3.0 - 3.6V) and $CL = 15$ pF.
2. Maximum value only applies during Program/Erase Suspend/Resume commands.

10.2 Capacitance Characteristics

Table 8. Capacitance

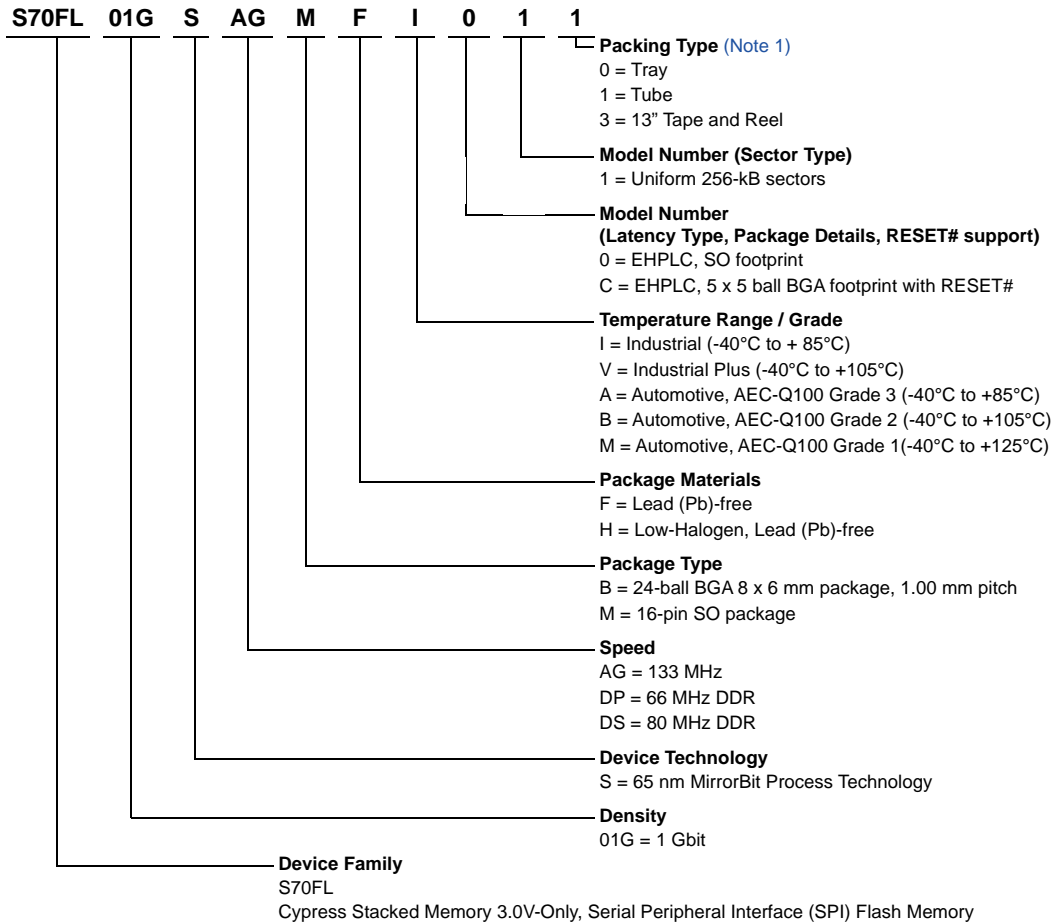
	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#1, CS#2, RESET#)	1 MHz	–	16	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz	–	16	pF

Note:

1. For more information on capacitance, please consult the IBIS models.

11. Ordering Information

The ordering part number is formed by a valid combination of the following:



Notes:

1. EHPLC = Enhanced High Performance Latency Code table.
2. Uniform 256-kB sectors = All sectors are uniform 256-kB with a 512B programming buffer.

11.1 Valid Combinations — Standard

Table 9 lists the valid combinations configurations planned to be supported in volume for this device.

Table 9. S70FL01GS Valid Combinations — Standard

S70FL01GS Valid Combinations					Package Marking (1)
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	
S70FL01GS	AG	MFI, MFV	01	0, 1, 3	FL01GS + A + (temp) + F + (Model Number)
	DP				FL01GS + D + (temp) + F + (Model Number)
	DS				FL01GS + S + (temp) + F + (Model Number)
	AG	BHI, BHV	C1	0, 3	FL01GS + A + (temp) + H + (Model Number)
	DP				FL01GS + D + (temp) + H + (Model Number)
	DS				FL01GS + S + (temp) + H + (Model Number)

Note:

1. Package Marking omits the leading "S70" and package type.

11.2 Valid Combinations — Automotive Grade / AEC-Q100

Table 10 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non-AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 10. S70FL01GS Valid Combinations — Automotive Grade / AEC-Q100

S70FL01GS Valid Combinations					Package Marking (1)
Base Ordering Part Number	Speed Option	Package and Temperature	Model Number	Packing Type	
S70FL01GS	AG	MFA, MFB, MFM	01	0, 1, 3	FL01GS + A + (temp) + F + (Model Number)
	DS				FL01GS + S + (temp) + F + (Model Number)
	AG	BHA, BHB, BHM	C1	0, 3	FL01GS + A + (temp) + H + (Model Number)
	DS				FL01GS + S + (temp) + H + (Model Number)

Note:

1. Package Marking omits the leading "S70" and package type.

12. Other Resources

12.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

12.2 Links to Software

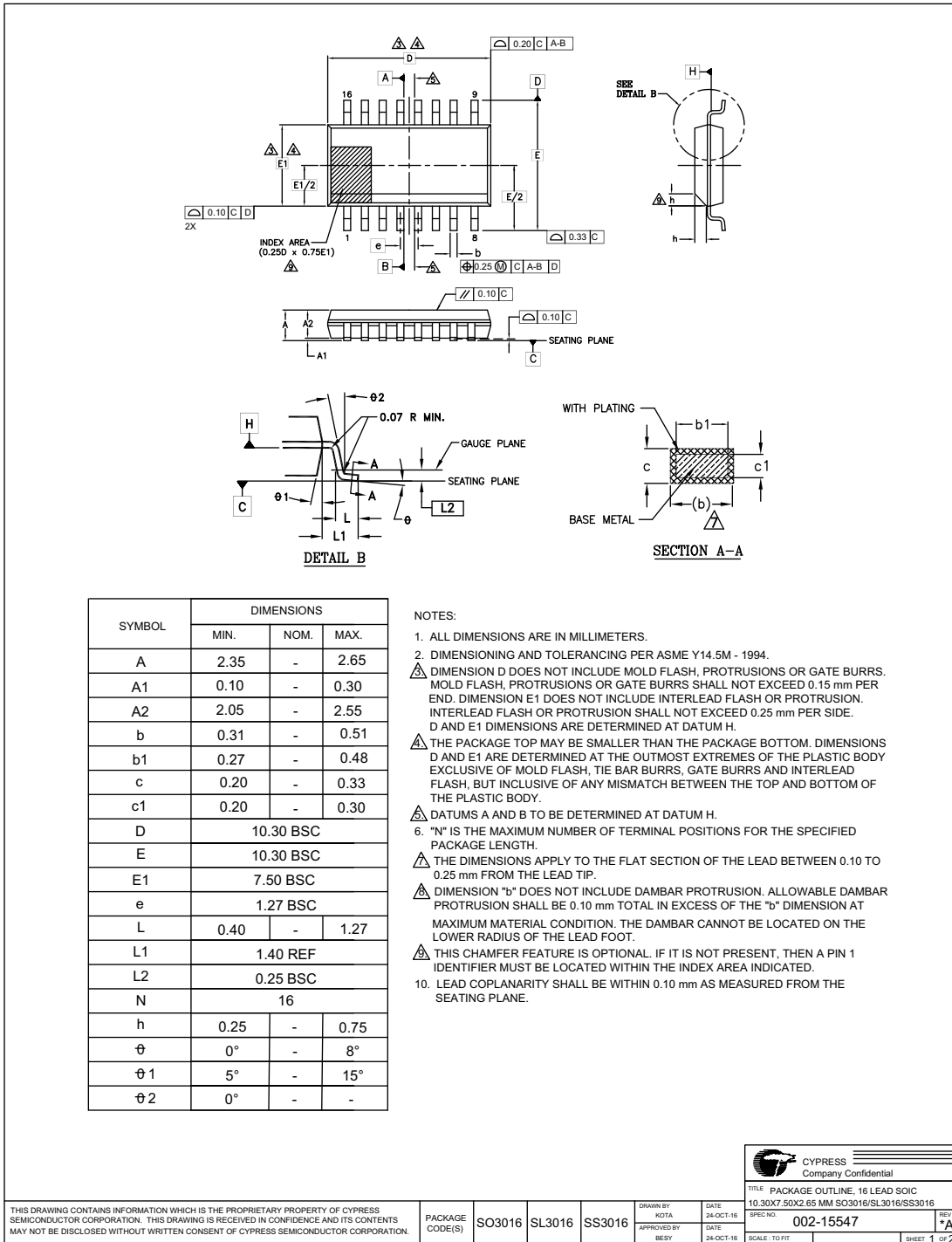
www.cypress.com/software-and-drivers-cypress-flash-memory

12.3 Links to Application Notes

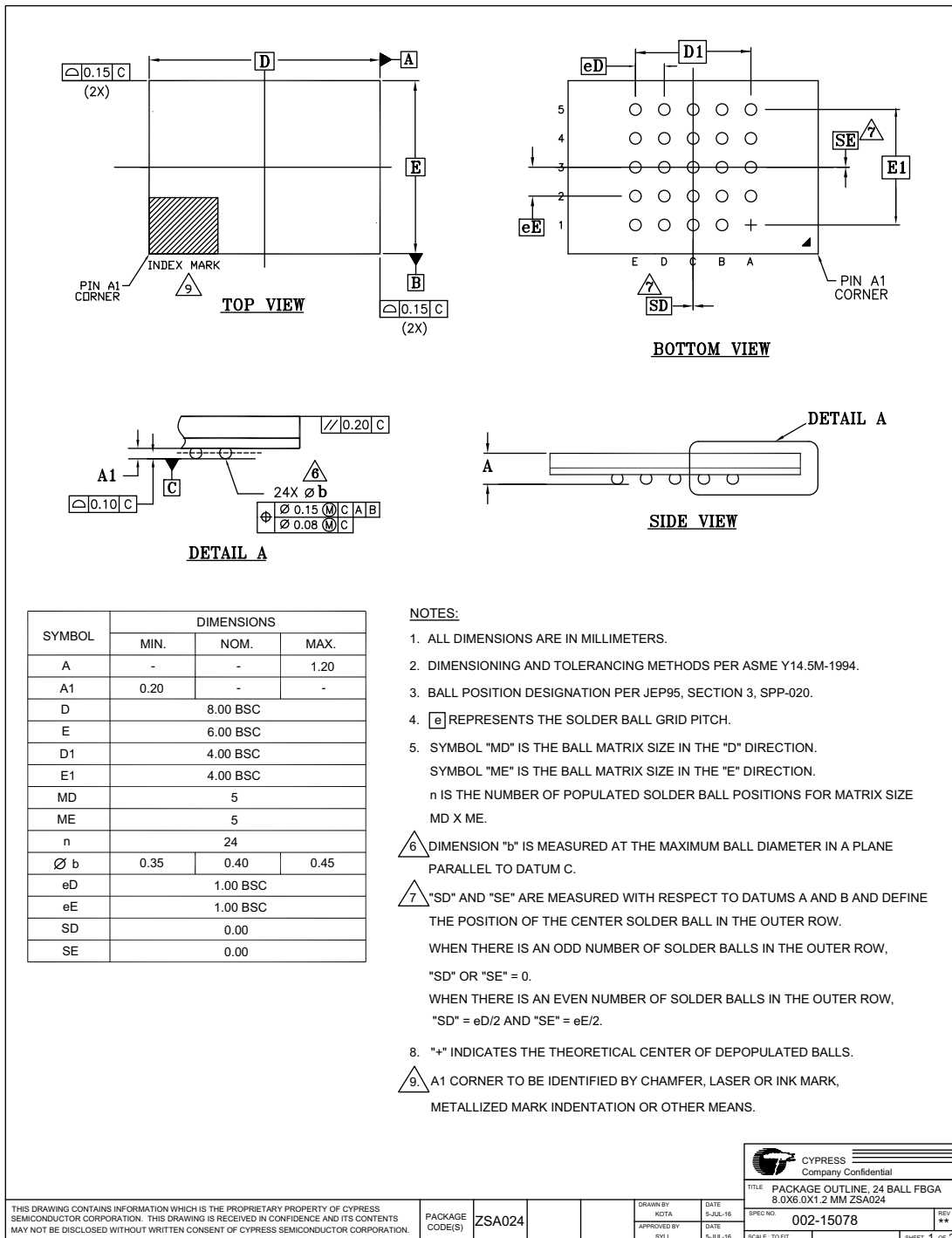
www.cypress.com/appnotes

13. Physical Diagram

13.1 SOIC 16 Lead, 300-mil Body Width



13.2 24-Ball BGA 8 x 6 mm (ZSA024)



14. Revision History

Document Title: S70FL01GS, 1 Gbit (128 Mbyte) 3.0V SPI Flash Document Number: 001-98295				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	—	BWHA	11/06/2012	Initial release
*A	—	BWHA	04/25/2013	Global: Datasheet designation updated from Advance Information to Preliminary DC Characteristics: DC Characteristics table: changed Max value of ILI, ILO, ICC1, and ISB
*B	—	BWHA	05/16/2013	SOIC 16 Physical Diagram: Updated package nomenclature from S03016 to SL3016
*C	—	BWHA	08/22/2013	Valid Combinations: Valid Combinations table: added MFV DC Characteristics: DC Characteristics table: added ISB (Automotive)
*D	—	BWHA	11/08/2013	Global: Datasheet designation updated from Preliminary to Full Production
*E	—	BWHA	03/19/2014	Features: Packages (all Pb-free): added BGA-24, 8 x 6 mm Connections Diagrams: Added figure: 24-Ball BGA, 5 x 5 Ball Footprint (FAB024), Top View Ordering Information: Added options to: Model Number, Package Materials, Package Type, and Speed Valid Combinations: Added option to S70FL01GS Valid Combinations Table SDR AC Characteristics: SDR AC Characteristics (Single Die Package, VCC = 2.7V to 3.6V) table: updated tv Min DDR AC Characteristics: Updated DDR AC Characteristics 66 MHz Operation table Capacitance Characteristics: Capacitance table: updated Max values and removed note
*F	—	BWHA	11/07/2014	Valid Combinations: Added DP Speed Option for BGA 5x5 package
*G	—	BWHA	04/21/2015	Valid Combinations: Added BHV option
*H	4871631	BWHA	08/24/2015	Updated to Cypress template. Changed Automotive Temperature Range to Industrial Plus Temperature Range in Features and Section 4 .
*I	5123878	BWHA	02/03/2016	Updated General Description .
*J	5536564	BWHA	12/02/2016	Updated Features on page 1 : Added Extended and Automotive Grade temperatures. Updated DDR AC Characteristics 66 MHz and 80 MHz Operation on page 11 table: Corrected t _{HO} Min value, t _{CSH} and t _{SU} Max value. Ordering Information on page 12 : Added Extended and Automotive Grade. Added Other Resources on page 14 .
*K	5612027	ECAO	01/17/2017	Added I _{CC1} value for Quad DDR @ 80 MHz in Table 4, DC Characteristics on page 8 Updated I _{CC5} value in Table 4, DC Characteristics on page 8 Updated DDR AC Characteristics 66 MHz and 80 MHz Operation on page 11 Removed Extended (-40°C to +125°C) temperature option in Ordering Information Updated Physical Diagram : Updated package name and drawing from SL3016 to SS3016. Updated package name and drawing from FAB024 to ZSA024.

Document Title: S70FL01GS, 1 Gbit (128 Mbyte) 3.0V SPI Flash Document Number: 001-98295				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*L	5669602	ECAO	04/05/2017	<p>Updated Figure 2, 24-Ball BGA, 5 x 5 Ball Footprint (ZSA024), Top View on page 4.</p> <p>Removed SS3016 from Section 13.1, SOIC 16 Lead, 300-mil Body Width on page 15.</p> <p>Removed CS# from Table 2, Signal List on page 5.</p> <p>Updated t_{SU} in Table 6, SDR AC Characteristics (Single Die Package, $V_{CC} = 2.7V$ to $3.6V$) on page 10.</p> <p>Updated Cypress logo.</p> <p>Updated Sales page.</p>
*M	5783913	ECAO	06/23/2017	<p>Changed OTP total space in Security Features.</p> <p>Updated I_{SB} values in Table 4.</p>

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2012-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.