

BGSA13GN10

Single-Pole Triple Throw Antenna Tuning Switch

Data Sheet

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Page	Subjects (major changes since last revision)
6	added on Table. 3 Absolute Maximum RF Voltage
9	deleted RF Operating Voltage on Table. 7
12	Package Dimensions Drawing figure updated (Figure3)

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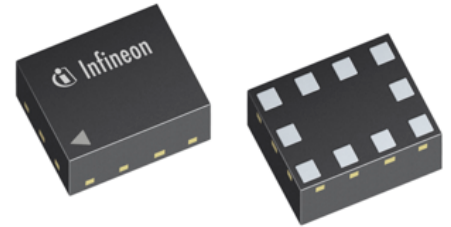
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BGSA13GN10 Single-Pole Triple Throw Antenna Tuning Switch

1 Features

- high-linearity SP3T for antenna aperture switching applications
- Ultra-Low R_{ON} port featuring 0.8Ω in ON state
- Ultra-Low C_{OFF} port featuring $120 fF$ in OFF state
- High max RF voltage handling
- Low harmonic generation
- No power supply blocking required
- Battery supply: 1.8 to 3.6 V
- Control voltage: 1.35 to 3.3 V (control high)
- Suitable for EDGE / C2K / LTE / WCDMA Applications
- 0.1 to 5.0 GHz coverage
- Small form factor 1.1 mm x 1.5 mm
- $400 \mu m$ pad pitch
- RoHS and WEEE compliant package

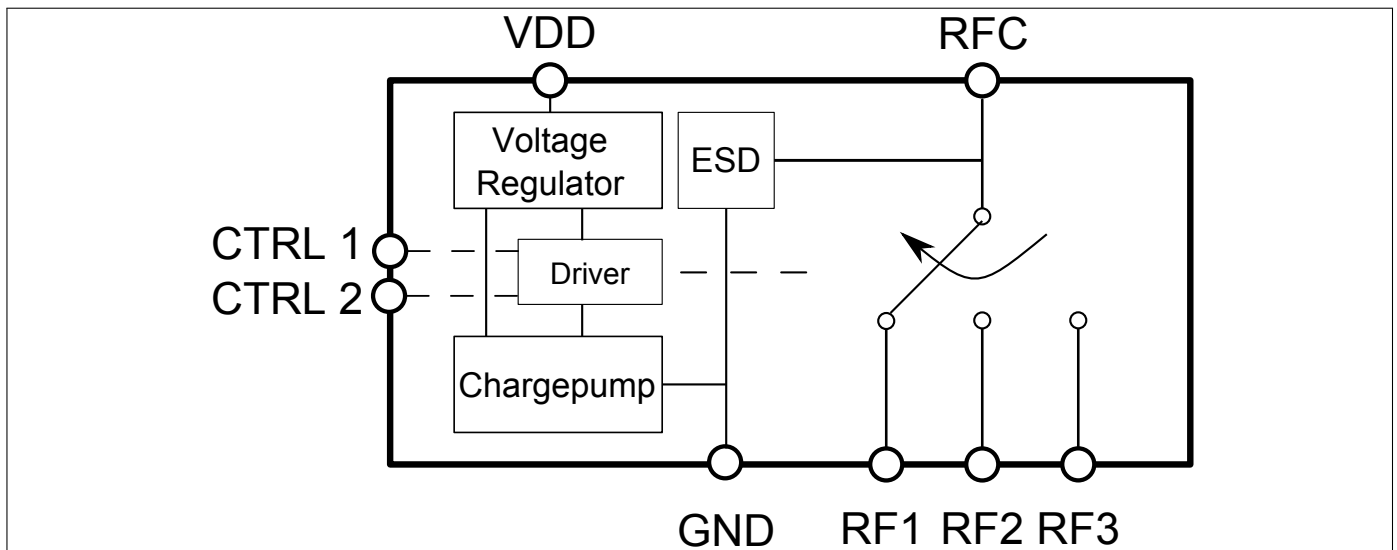


2 Product Description

The BGSA13GN10 is a Single Pole Triple Throw (SP3T) RF antenna aperture switch optimized for low C_{off} enabling applications up to 5.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Table 1: Ordering Information

Type	Package	Marking/Type Code	Chip
BGSA13GN10	TSNP10-1/-2	A3	BGSA13GN10


Figure 1: BGSA13GN10 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	¹⁾
Supply voltage ²⁾	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	$^\circ\text{C}$	–
RF input power	P_{RF_TRX}	–	–	39	dBm	25% Duty Cycle
RF voltage ³⁾	V_{RF_max}	–	–	48	V	All switch throws operated in isolation mode.
ESD capability, CDM ⁴⁾	V_{ESDCDM}	-1.5	–	+1.5	kV	
ESD capability, HBM ⁵⁾	V_{ESDHBM}	-1	–	+1	kV	
ESD capability, system level (RFC port) ⁶⁾	V_{ESDANT}	-8	–	+8	kV	RFC vs system GND, with 27 nH shunt inductor
Junction temperature	T_j	–	–	125	$^\circ\text{C}$	–

¹⁾ Switch has no highpass response. There is also a high ohmic DC to the RF path. The DC voltage at RF ports V_{RFDC} has to be 0V.

²⁾ Note: Consider any ripple voltages on top of V_{DD} . A high RF ripple at the V_{DD} can exceed the maximum ratings by $V_{DD} = V_{DC} + V_{Ripple}$.

³⁾ 1000h over 8 years lifetime-short pulse duration

⁴⁾ Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

⁵⁾ Human Body Model ANSI/ESDA/JEDEC JS-001-2012 ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$).

⁶⁾ IEC 61000-4-2 ($R = 330\text{ }\Omega$, $C = 150\text{ pF}$), contact discharge.

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 3: Maximum Ratings, Table II at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTRL}	-0.7	–	3.3	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.8	2.85	3.6	V	–
Supply current ¹⁾	I_{DD}	–	80	150	μA	–
Control voltage low	$V_{Ctrl,low}$	0		0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} \ll V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	μA	–
Control current high	$I_{Ctrl,high}$	-1	0	1	μA	$V_{Ctrl,high} \ll V_{DD}$
Ambient temperature	T_A	-30	25	85	$^{\circ}C$	–
RF switching time	t_{sw}	2	5	7	μs	tested in parametric verification
Startup time	t_{sw}		20	30	μs	tested in parametric verification

¹⁾ $T_A = -30\text{ °C} - +85\text{ °C}$, $V_{DD} = 1.8 - 3.6\text{ V}$

5 Logic Table

Table 5: Logic Table

CTRL 1	CTRL 2	Mode
0	0	RF1 connected to RFC
0	1	RF2 connected to RFC
1	0	RF3 connected to RFC
1	1	Isolation Mode

6 RF small signal parameter

Table 6: RF small signal parameter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	5.0	GHz	–
RF1 Switch ON resistance	$R_{ON,RF1}$	–	0.8		Ω	RF1 to RFC
RF1 Switch OFF capacitance	$C_{OFF,RF1}$	–	300		fF	RF1 to RFC
RF2 Switch ON resistance	$R_{ON,RF2}$	–	1.4		Ω	RF2 to RFC
RF2 Switch OFF capacitance	$C_{OFF,RF2}$	–	160		fF	RF2 to RFC
RF3 Switch ON resistance	$R_{ON,RF3}$	–	1.6		Ω	RF3 to RFC
RF3 Switch OFF capacitance	$C_{OFF,RF3}$	–	120		fF	RF3 to RFC
Parasitic RF shunt capacitance	$C_{SH,PAR}$	–	42		fF	RFx to GND
Switch series inductance	L_{SER}	–	0.1		nH	
RF1 Insertion Loss ^{1,2,3}						
698 - 960 MHz	IL	0.16	0.20	0.25	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C},$ $Z_0 = 50 \Omega$
1710 - 1980 MHz		0.23	0.29	0.38	dB	
1981 - 2169 MHz		0.29	0.27	0.39	dB	
2170 - 2690 MHz		0.32	0.36	0.47	dB	
RF2 Insertion Loss ^{1,2,3}						
698 - 960 MHz	IL	0.20	0.27	0.35	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C},$ $Z_0 = 50 \Omega$
1710 - 1980 MHz		0.29	0.39	0.49	dB	
1981 - 2169 MHz		0.36	0.45	0.55	dB	
2170 - 2690 MHz		0.44	0.53	0.64	dB	
RF3 Insertion Loss ^{1,2,3}						
698 - 960 MHz	IL	0.20	0.28	0.36	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C},$ $Z_0 = 50 \Omega$
1710 - 1980 MHz		0.37	0.44	0.53	dB	
1981 - 2169 MHz		0.39	0.46	0.57	dB	
2170 - 2690 MHz		0.49	0.63	0.75	dB	
RF1 Return Loss ^{1,2,3}						
All Ports @ 698 - 960 MHz	RL	21	26	31	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C}, Z_0 = 50 \Omega$
All Ports @ 1710 - 2690 MHz		17	20	25	dB	
RF2 Return Loss ^{1,2,3}						
All Ports @ 698 - 960 MHz	RL	21	26	31	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C}, Z_0 = 50 \Omega$
All Ports @ 1710 - 2690 MHz		18	20	27	dB	
RF3 Return Loss ^{1,2,3}						
All Ports @ 698 - 960 MHz	RL	21	26	31	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C}, Z_0 = 50 \Omega$
All Ports @ 1710 - 2690 MHz		15	17	25	dB	

¹⁾ Valid for all RF power levels, no compression behavior

²⁾ Network analyser input power: $P_{IN} = -20 \text{ dBm}$
³⁾ On application board without any matching components

Table 7: RF small signal parameter - Isolation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Isolation RFx to RFC^{1,2,3}						
698 - 915 MHz	ISO	23	26	30	dB	$V_{DD} = 1.8 - 3.6 V,$ $T_A = -30 \dots +85 \text{ }^\circ\text{C},$ $Z_0 = 50 \Omega$
1710 - 1980 MHz		17	20	27	dB	
1981 - 2170 MHz		15	18	25	dB	
2171 - 2690 MHz		14	17	24	dB	

7 RF large signal parameter

Table 8: RF large signal specifications
Harmonic Generation up to 12.75 GHz^(1,2,3)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
All RF Ports - Second Order Harmonics	P_{H2}	–	105	–	dBc	25 dBm, 50Ω , $f_0 = 786 \text{ MHz}$
All RF Ports - Third Order Harmonics	P_{H3}	–	115	–	dBc	25 dBm, 50Ω , $f_0 = 786 \text{ MHz}$
All RF Ports - Second Order Harmonics	P_{H2}	–	93	–	dBc	36 dBm, 50Ω , $f_0 = 824 \text{ MHz}$
All RF Ports - Third Order Harmonics	P_{H3}	–	94	–	dBc	33 dBm, 50Ω , $f_0 = 824 \text{ MHz}$
All RF Ports	P_{Hx}	105	–	–	dBc	25 dBm, 50Ω

Intermodulation Distortion IMD2^(1,2,3)

IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 9
IIP2, high	IIP2,h	–	120	–	dBm	

Intermodulation Distortion IMD3^(1,2,3)

IIP3	IIP3	–	75	–	dBm	IIP3 conditions table 10
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SV LTE Intermodulation^(1,2,3)

IIP3,SVLTE	IIP3,SV	–	75	–	dBm	SV-LTE conditions table 11
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¹Terminating Port Impedance: $Z_0 = 50 \Omega$
²Supply Voltage: $V_{DD} = 1.8 - 3.6 V$
³On application board without any matching components

Table 9: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 10: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 11: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

8 Package Outline and Pin Configuration

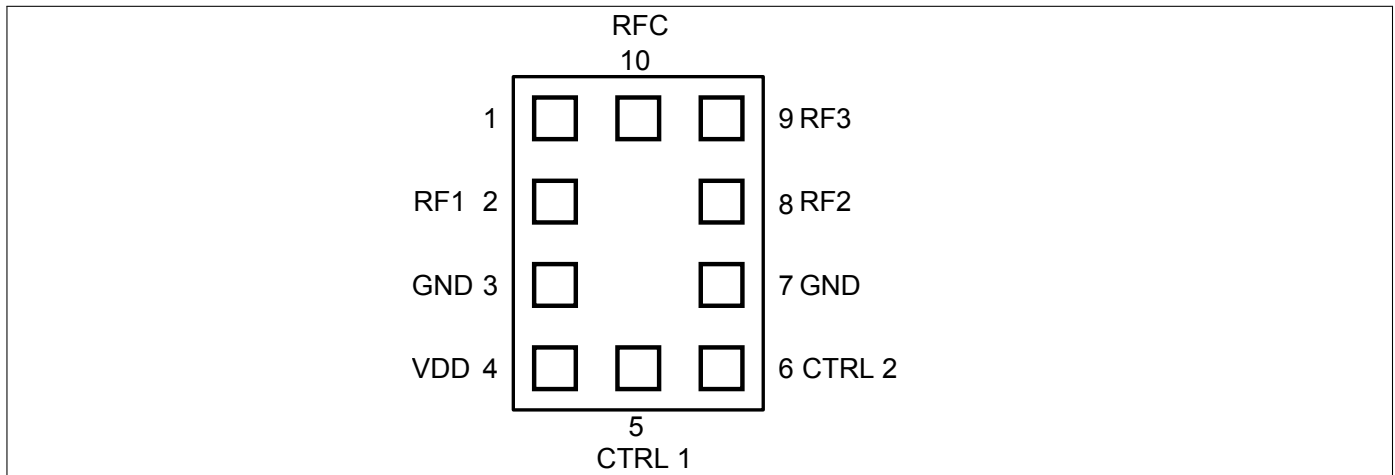


Figure 2: Pinout (top view)

Table 12: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	N.C.	N.C.		Not connected
2	RF1	I/O		RF1
3	GND	GND		Ground
4	VDD	PWR		Supply voltage
6	CTRL1	I		Control 1 Pin
6	CTRL2	I		Control 2 Pin
7	GND	GND		Ground
8	RF2	I/O		RF2
9	RF3	I/O		RF3
10	RFC	I/O		Common RF

Table 13: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	<i>X</i>	1.1 ± 0.05	mm
Y-Dimension	<i>Y</i>	1.5 ± 0.05	mm
Size	<i>Size</i>	1.65	mm ²
Height	<i>H</i>	0.375	mm

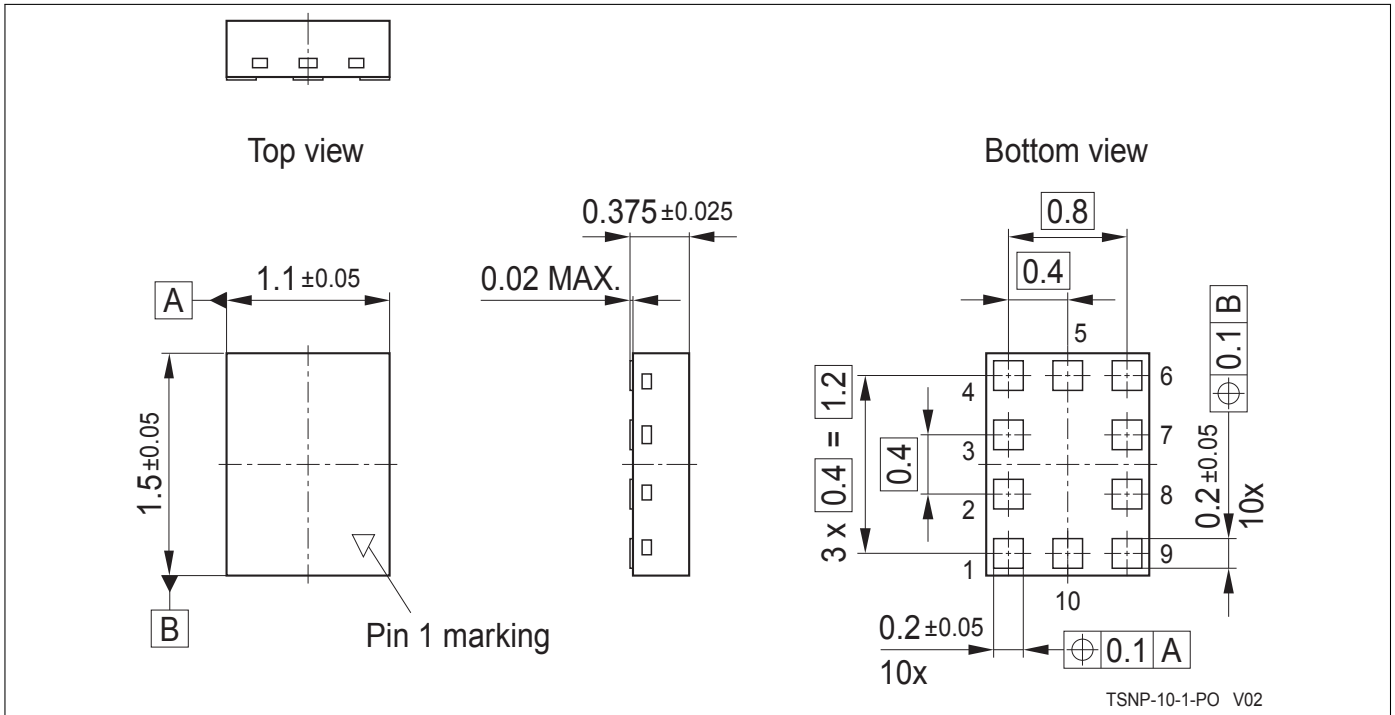


Figure 3: Package Dimensions Drawing (TSNP-10-1)

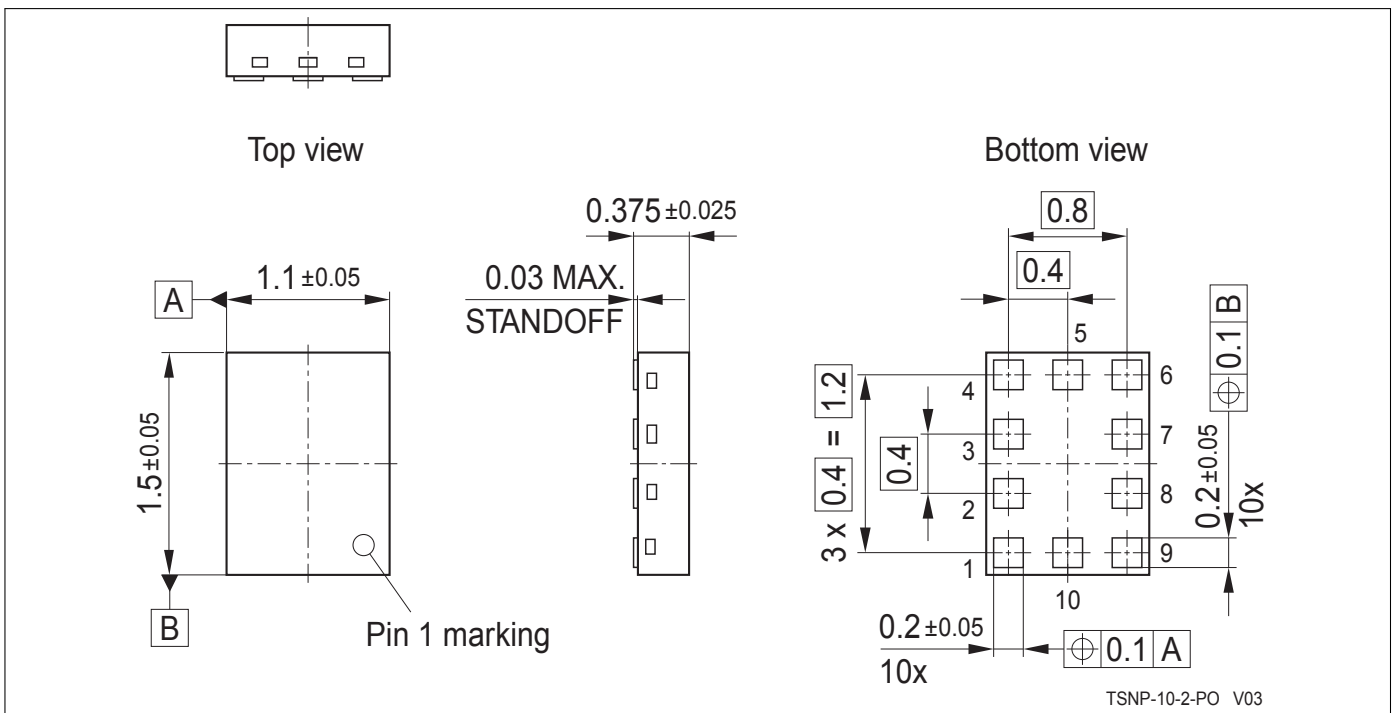


Figure 4: Package Dimensions Drawing (TSNP-10-2)

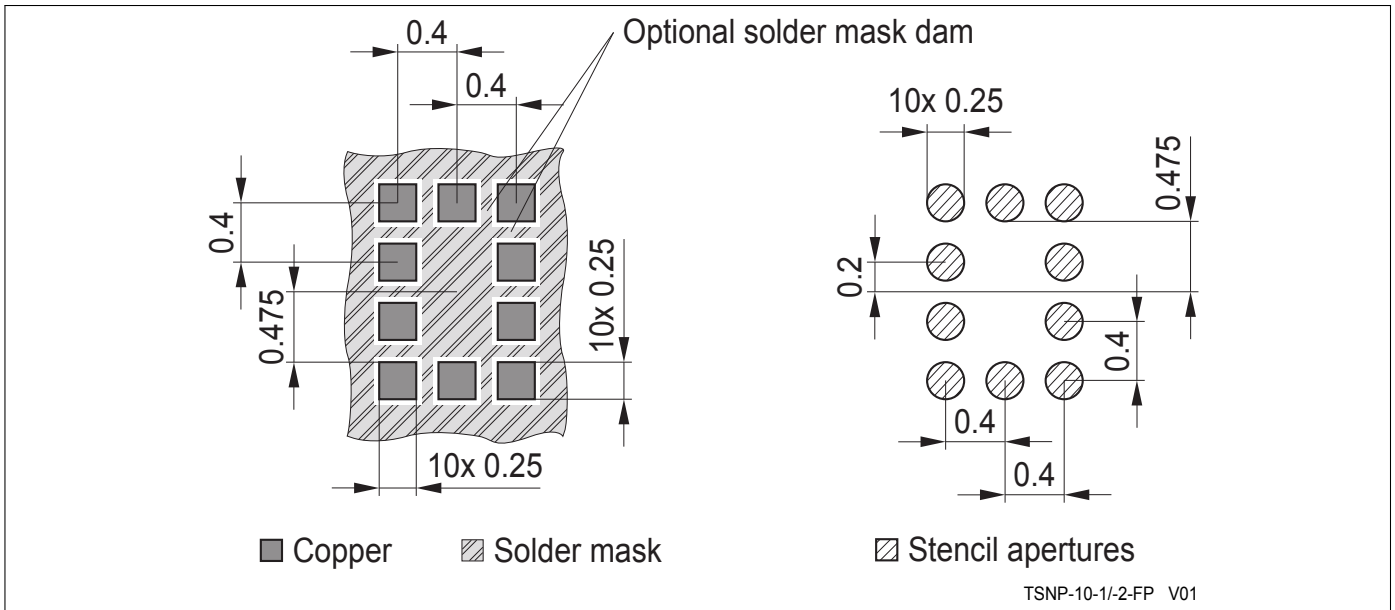


Figure 5: Land pattern and stencil mask (TSNP-10-1/-2)

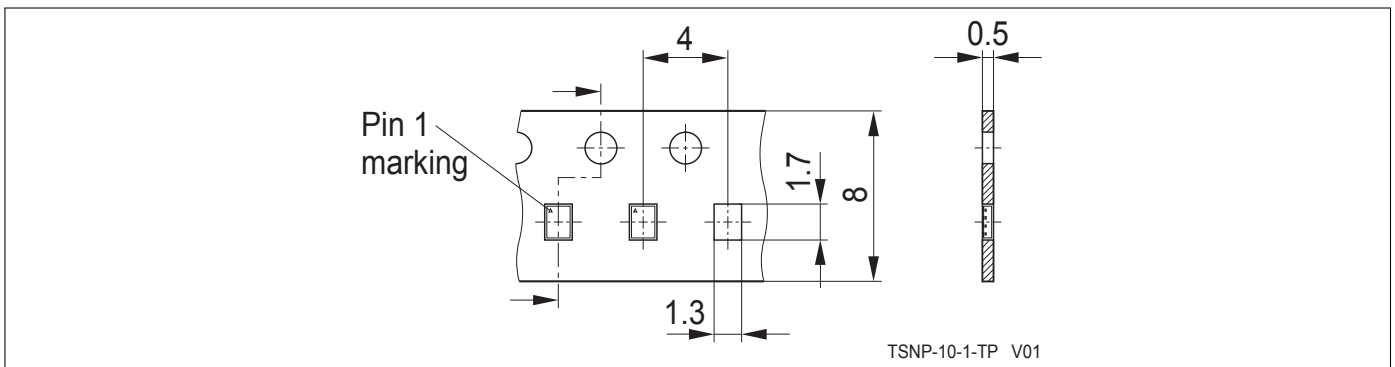


Figure 6: Tape drawing (TSNP-10-1)

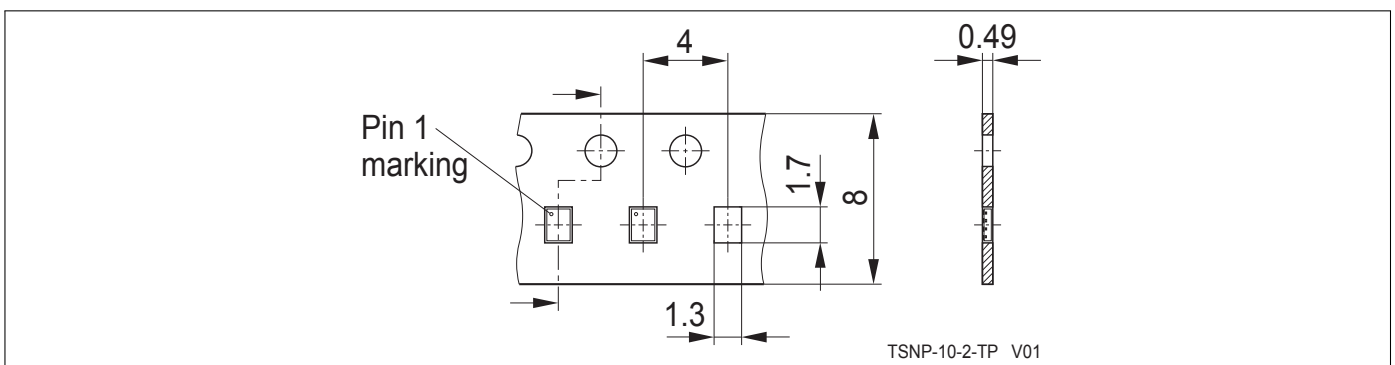


Figure 7: Tape drawing (TSNP-10-2)

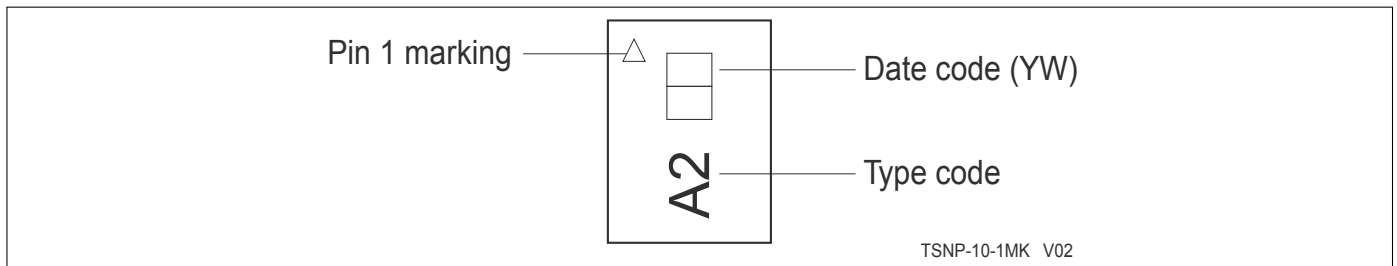


Figure 8: Package marking (TSNP-10-1): Date code digits Y and W are found in Table 13/14

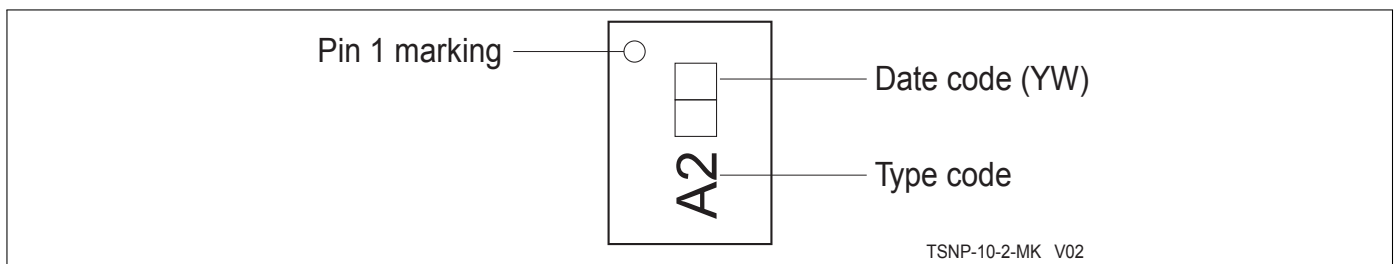


Figure 9: Package marking (TSNP-10-2): Date code digits Y and W are found in Table 13/14

Table 14: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 15: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

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