Control Integrated POwer System (CIPOS™)

Inverter IPM Reference Board Type 1 for 1-Shunt Resistor

About this document

Scope and Purpose

The scope of this application note is to describe the product reference board of the CIPOS™ Mini inverter IPM and the basic requirements for operating the product in a recommended mode. Environmental conditions were considered in the design of the reference board. The design was tested as described in this document but not qualified regarding safety requirements or manufacturing and operation over the whole operating temperature range or lifetime. The boards provided by Infineon are subject to functional testing only.

Reference boards are not subject to the same procedures as regular products regarding Returned Material Analysis (RMA), Process Change notification (PCN) and Product Discontinuation (PD). Reference boards are intended to be used under laboratory conditions by specialists only.

Intended Audience

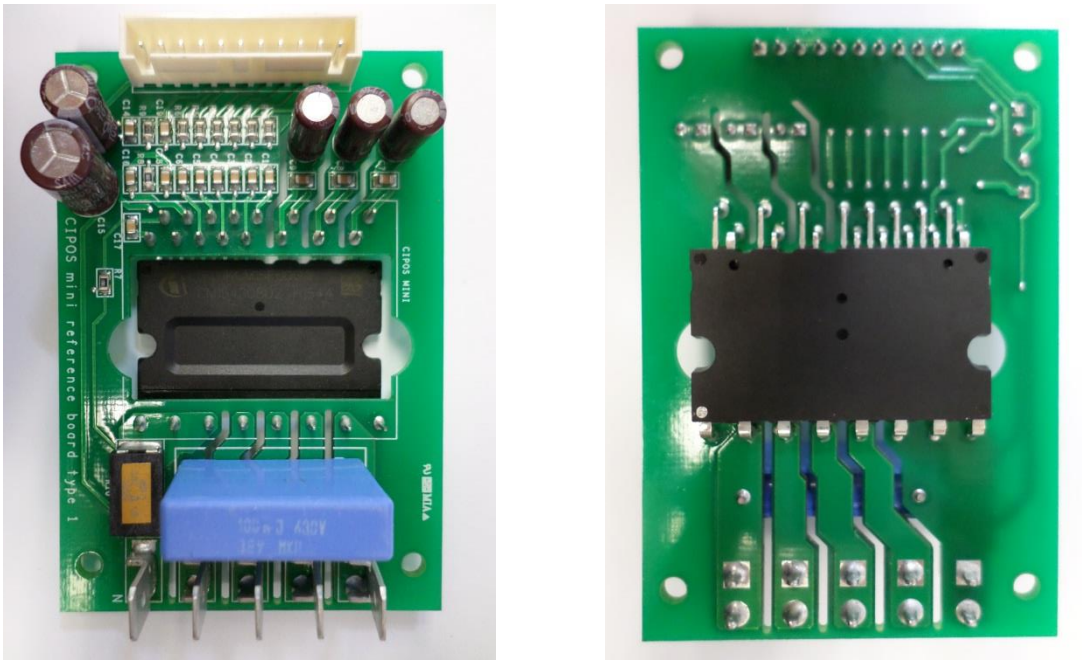
Power electronics engineers who want to evaluate the CIPOS™ Mini inverter IPM.

Table of Contents

1 Introduction

This reference board is composed of the IGCM10F60GA, minimum peripheral components and single current sensing resistor. It is designed for customers to evaluate the performance of the CIPOS™ Mini inverter IPM with simple connections of control signals and power wires. Figure 1 shows the external view of the reference board.

This application note also describes how to design key parameters and PCB layout.



Top view Bottom view

Figure 1 Reference board pictures

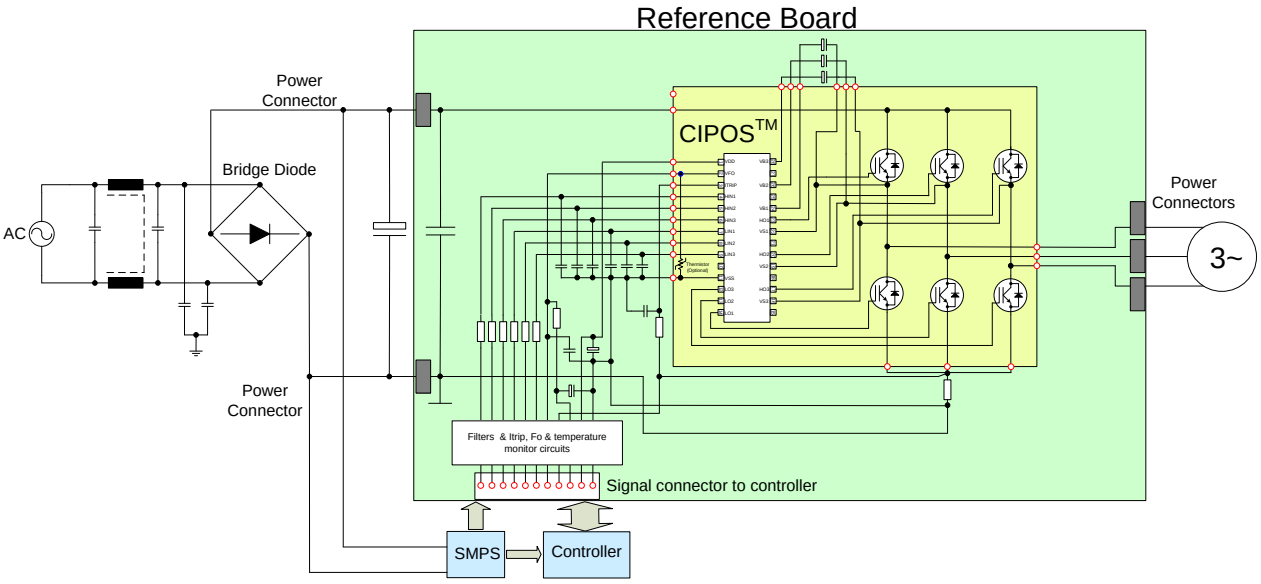


Figure 2 Application example

2 Schematic

Figure 3 shows a circuitry of the reference board.

The reference board consists of interface circuit, bootstrap circuit, snubber capacitor, Short Circuit (SC) protection circuit, fault output circuit, current sensing resistor and passive parts etc.

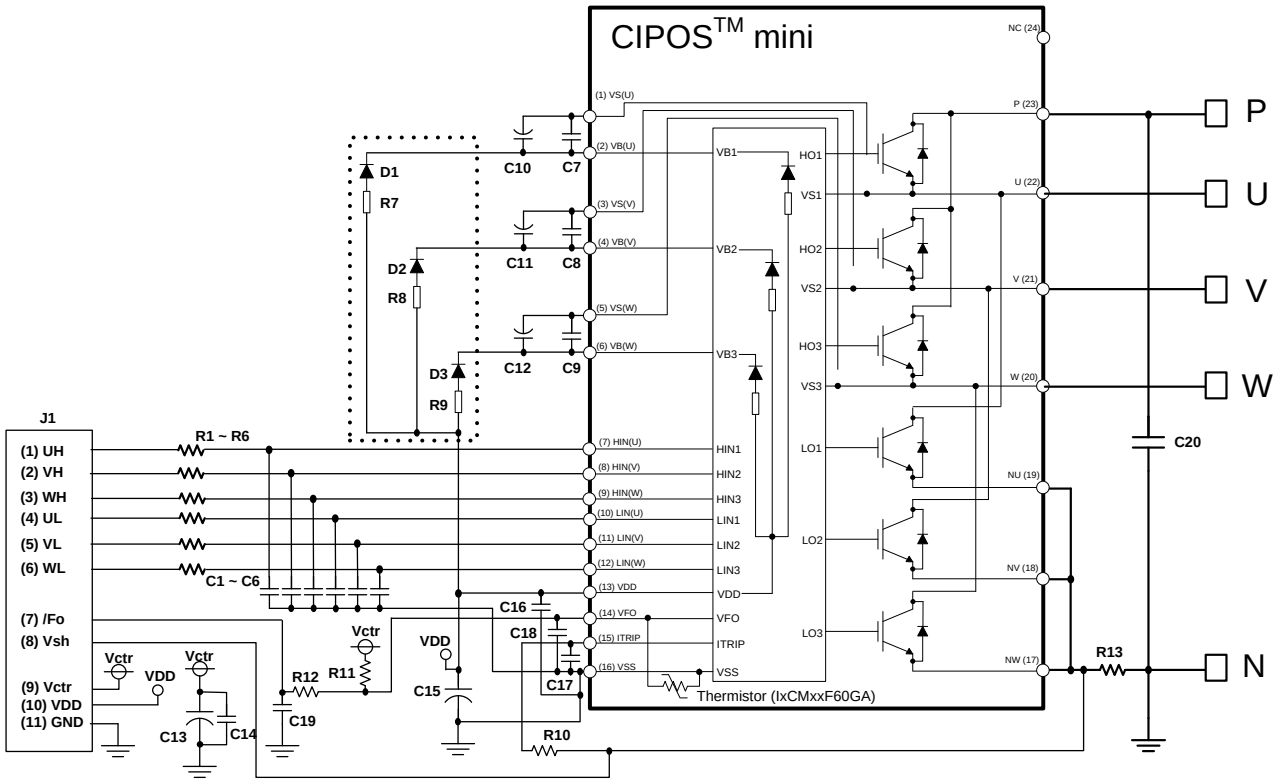


Figure 3 Circuit of the reference board

Note: The "Vctr" on the J1 pin 9 denotes the control signal supply voltage such as 5V or 3.3V.

Note: It is optional to use external bootstrap circuit together with the internal one as shown in the dotted line, in case that a smaller bootstrap resistor is necessary.

3 External Connection

3.1 Signal Connector

Table 1 Pin description of the signal connector (J1 HEADER 11, 11-pin, 2.5mm pin pitch)

Pin	Name	Description
1	HIN(U)	Control signal input for phase U upper side IGBT
2	HIN(V)	Control signal input for phase V upper side IGBT
3	HIN(W)	Control signal input for phase W upper side IGBT
4	LIN(U)	Control signal input for phase U lower side IGBT
5	LIN(V)	Control signal input for phase V lower side IGBT
6	LIN(W)	Control signal input for phase W lower side IGBT
7	/Fo	Fault output signal / Temperature monitor (Optional)
8	Vsh	Sensing signal for voltage of current sensing resistor
9	Vctr	External 5V or 3.3V supply for control signal
10	VDD	External 15V supply for module
11	GND	Ground

3.2 Power Terminals

Table 2 Pin description of power terminals

Terminal Name	Description
U	Output node of U phase
V	Output node of V phase
W	Output node of W phase
P	Positive node of DC link voltage
N	Negative node of DC link voltage

4 Key Parameters Setting

4.1 Circuit of Input Signals (LIN(X), HIN(X))

The input signals are compatible with either TTL or CMOS levels. The logic level can go down to 3.3V. The maximum input voltage of the input signal pin is clamped to 10.5V by the internal Zener diode. However the recommended voltage range of input voltage is up to 5V. The input signals LIN(X) and HIN(X) are active high.

These pins have an internal pull-down structure with a pull-down resistor, which is nominal 5kΩ. The input noise filter inside the CIPOS™ Mini inverter IPM suppresses short pulses and prevents a false IGBT driving from an unintentional operation. The input noise filter time (t_{FLIN}) is typically 270ns. This means that the input signal must stay on more than 270ns so that the driver IC detects the normal PWM input for a correct IGBT driving. CIPOS™ Mini inverter IPM can be connected directly to the controller without an external input RC filter due to the internal pull down resistor and input noise filter, as shown in Figure 4.

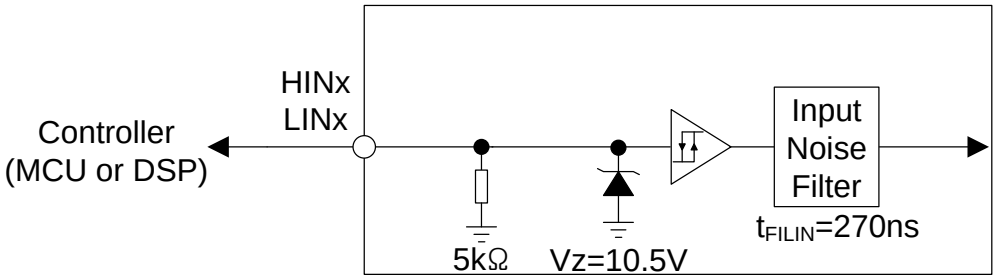


Figure 4 Internal pull-down resistor and input noise filter on input signal pin

4.2 Bootstrap Capacitor

Bootstrapping is a common method for charge pumping from a low potential to a higher one. With this technique a supply voltage can be easily established for a floating high side section of the gate driver. Figure 5 below shows a simple bootstrap circuit diagram. It represents only one-phase effective circuit from a three-phase half bridge inverter. The bootstrap functionality is implemented internally to limit current. Please refer to the datasheet and application note for the bootstrapping method in detail.

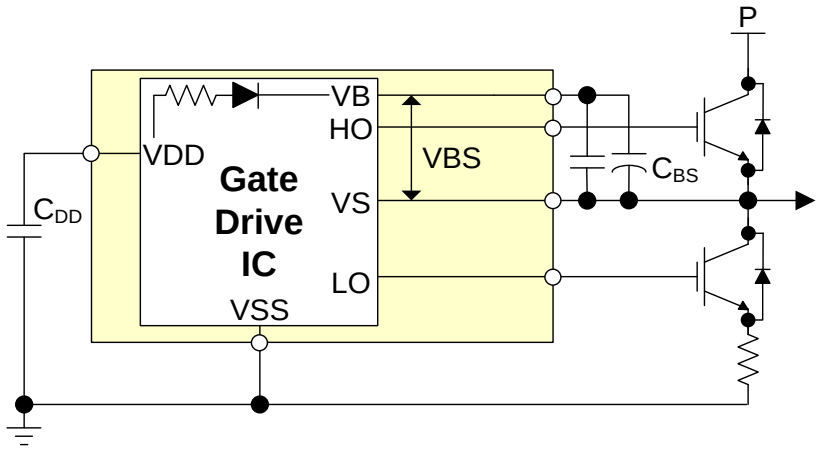


Figure 5 Bootstrap circuit for the supply of the high side gate drive

Key Parameters Setting

A low leakage current of the high side section is very important in order to keep the bootstrap capacitor small. The bootstrap capacitor (C_{BS}) is discharged mainly by the following mechanisms:

- Quiescent current to the high side circuit in IC
- Gate charge for turning high side IGBT on
- Level-shift charge required by level shifters in IC
- Bootstrap capacitor leakage current (can be ignored for a non-electrolytic capacitor)
- Bootstrap diode leakage current
- Bootstrap diode reverse recovery charge

The calculation of the bootstrap capacitor results in the following equation.

$$C_{BS} = \frac{I_{leak} \times t_P}{\Delta V_{BS}}$$

Where,

- C_{BS} : bootstrap capacitor value
- I_{leak} : maximum discharge current of the C_{BS}
- t_P : maximum on pulse width of the high side IGBT
- ΔV_{BS} : voltage drop at the bootstrap capacitor within a switching period

A practical leakage current level (I_{leak}) of the CIPOS™ Mini inverter IPM is max. 1mA for 1 cycle turn on of the HS IGBT.

Figure 6 shows the curve corresponding to the C_{BS} equation above for a continuous sinusoidal modulation when the voltage ripple (ΔV_{BS}) is 0.1V. The recommended bootstrap capacitance for a continuous sinusoidal modulation method is therefore in the range up to 4.7µF for 2~20kHz switching frequencies. In other PWM method case like a discontinuous sinusoidal modulation, the t_P must be set to the longest period of the low side IGBT off.

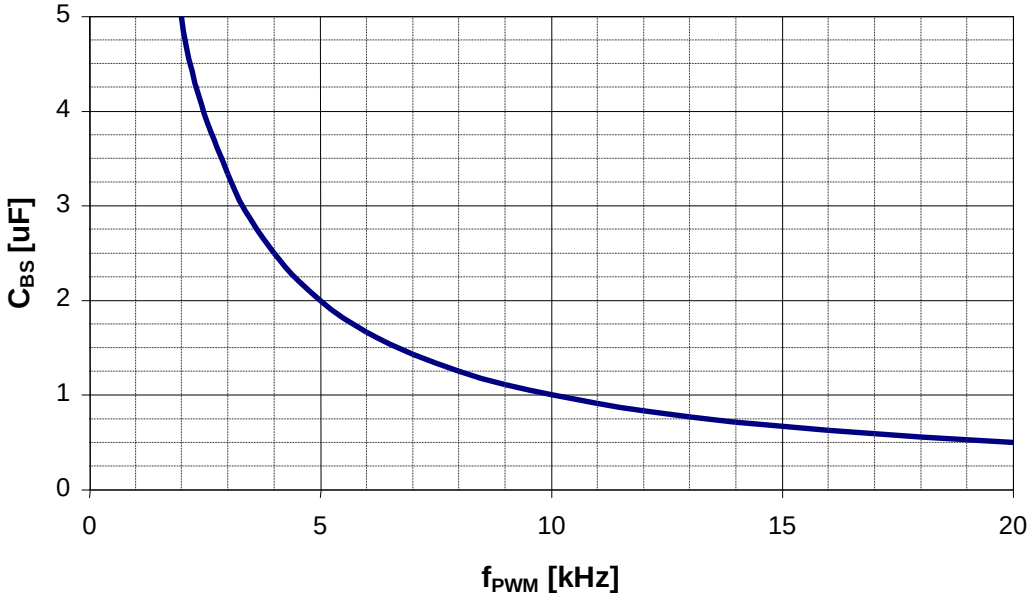


Figure 6 Value of the bootstrap capacitor as a function of the switching frequency, f_{PWM}

4.3 Internal Bootstrap Circuit Characteristics

CIPOS™ Mini inverter IPM includes three bootstrap circuits in the internal drive IC, which consist of three diodes and three resistors, as shown in Figure 5. A typical value of the internal bootstrap resistor is 40Ω. For more information, please refer to the below Table 3. Note that R_{BS2} and R_{BS3} have the same value with the R_{BS1}.

Table 3 Internal bootstrap circuit characteristics

Description	Condition	Symbol	Min.	Typ.	Max.	Unit
Repetitive peak reverse voltage		V_{RRM}	600			V
Bootstrap resistance of U-phase	VS2 or VS3=300V, T_J=25°C VS2 and VS3=0V, T_J=25°C VS2 or VS3=300V, T_J=125°C VS2 and VS3=0V, T_J=125°C	R_{BS1}		35 40 50 65		Ω
Reverse recovery time	I_F=0.6A, di/dt=80A/µs	t_{rr_BS}		50		ns
Forward voltage drop	I_F=20mA, VS2 and VS3=0V	V_{F_BS}		2.6		V

4.4 Over Current Protection

Over Current (OC) protection level is decided by ITRIP positive going threshold voltage ($V_{IT,TH+}$) and current sensing resistance. When the ITRIP voltage exceeds $V_{IT,TH+}$, the module turns off all 6 IGBTs and the fault flag is activated during fault-output duration time, typically 65µs.

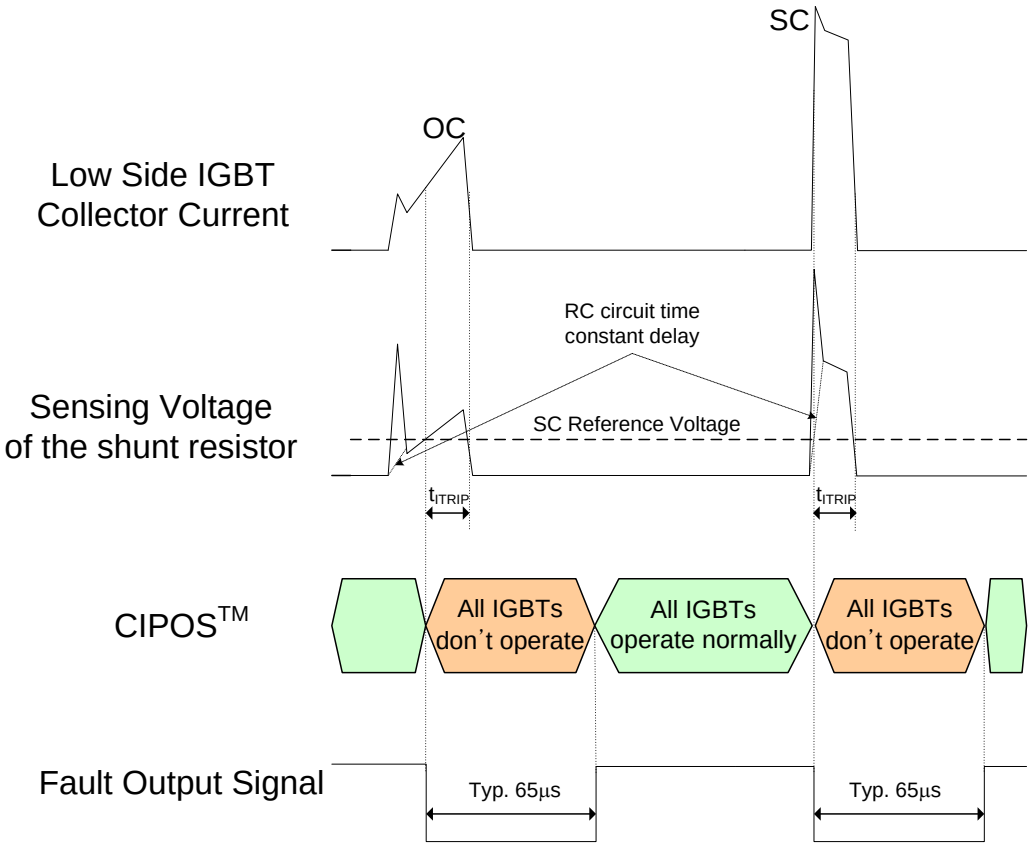


Figure 7 Timing chart of OC protection

4.4.1 Current Sensing Resistor Selection

The value of the current sensing resistor can be calculated with the following equation.

$$R_{SH} = \frac{V_{IT,TH+}}{I_{OC}}$$

Where,

- R_{SH} : current sensing resistor value
- $V_{IT,TH+}$: ITRIP positive going threshold voltage, typ. 0.47V
- I_{OC} : over current level

A maximum value of the OC protection level should be set less than the maximum peak output current in the datasheet absolute maximium ratings while taking into consideration the tolerance of the current sensing resistor.

For example, the maximum peak output current of the IGCM10F60GA is $20A_{peak}$,

$$R_{SH(min)} = \frac{0.47}{20} = 0.024\Omega$$

So the recommended value of the current sensing resistor should be higher than 24mΩ for IGCM10F60GA.

In order to calculate the power rating of the current sensing resistor, the below items has to be taken into account.

- Maximum load current of the inverter module (I_{RMS})
- Current sensing resistor value at Tc=25°C (R_{SH})
- Power derating ratio of the current sensing resistor at T_{SH}=100°C
- Safety margin

And the power rating can be calculated with the equation below.

$$P_{SH} = \frac{I_{RMS}^{\ 2} \times R_{SH} \times \text{Safety margin}}{\text{Derating ratio}}$$

For example, In case of IGCM10F60GA and R_{SH}=24mΩ

- Max. load current of the inverter module (I_{RMS}) : $6A_{RMS}$
- Current sensing resistor value at Tc=25°C (R_{SH}) : 0.024Ω
- Power derating ratio of the current sensing resistor at T_{SH}=100°C : 80%
- Safety margin : 30%

$$P_{SH} = \frac{6A^2 \times 0.024\Omega \times 130\%}{80\%} = 1.4W$$

So the proper power rating of the current sensing resistor is recommended as more than 1.4W.

Based on the equation, condition and calculation method above, some example values of minimum current sensing resistance and required resistor power rating are introduced as shown in below Table 4 for CIPOS™ Mini inverter module products. When choosing a proper current sensing resistance and its power rating, an accurate OC protection level in the application setting should be taken into account for a correct over current detection.

Table 4 Maximum peak current, shunt resistor value and required power rating

Key Parameters Setting

Product	Maximum Peak Current	Minimum Shunt Resistance, RSH	Minimum Shunt Resistor Power, PSH
IKCM30F60xA	60	8mΩ	5W
IGCM20F60xA	45	11mΩ	4W
IGCM15F60xA	30	16mΩ	3W
IGCM10F60xA	20	24mΩ	1.5W
IGCM06x60xA	12	40mΩ	1W
IGCM04F60xA	8	60mΩ	0.7W

4.4.2 Delay Time

An RC filter should be necessary in the OC sensing circuit to prevent a false OC protection caused by noise interference. The time constant of the RC filter should be determined while considering the noise period and the IGBT withstand time against the OC event. When the current flows through the current sensing resistor, the induced voltage drop on the current sensing resistor is supplied to the ITRIP pin of the CIPOS™ Mini inverter IPM through the RC filter. While the ITRIP pin voltage is rising to the ITRIP positive threshold voltage (typ. 0.47V), the filter delay time (t_{Filter}) is created by the RC filter time constant. In addition there is a shutdown propagation delay on ITRIP (t_{ITRIP}) as shown in the Table 5 below.

Table 5 Shut down propagation delay

Item		Condition	Min.	Typ.	Max.	Unit
Shut down propagation delay (t_{ITRIP})	IKCM30F60xA	I_{out} =20A, from $V_{IT,TH+}$ to 10% I_{out}	-	1420	-	ns
	IGCM20F60xA	I_{out} =15A, from $V_{IT,TH+}$ to 10% I_{out}	-	1540	-	
	IGCM15F60xA	I_{out} =10A, from $V_{IT,TH+}$ to 10% I_{out}	-	1340	-	
	IGCM10F60xA	I_{out} =6A, from $V_{IT,TH+}$ to 10% I_{out}	-	1260	-	
	IGCM06x60xA	I_{out} =4A, from $V_{IT,TH+}$ to 10% I_{out}	-	1300	-	
	IGCM04F60xA	I_{out} =2.5A, from $V_{IT,TH+}$ to 10% I_{out}	-	1320	-	

Therefore, the total delay time from occurrence of the OC event to the shutdown of the IGBT gate becomes:

$$t_{total} = t_{Filter} + t_{ITRIP}$$

The shut down propagation delay is in inverse proportion to the current range. Therefore the t_{ITRIP} will be shorter with a higher current condition, comparing to the current condition in the Table 5. The total delay must be less than 5µs of the short circuit withstand time (t_{SC}), which is specified in the datasheet. Thus, the RC time constant should be set in the range of 1~2µs. A recommended RC filter values are 1.8kΩ R10 and 1nF C17.

4.5 Temperature Monitor and Thermal Protection

In case of the CIPOS™ Mini inverter IPM, a built-in thermistor (85kΩ at 25°C) is connected between VFO and VSS pins. The typical application circuit looks like Figure 8 where the VFO pin is used for both thermistor temperature sensing and fault flag. The voltage of the VFO pin decreases as the thermistor temperature increases because the thermistor is a NTC (Negative Temperature Coefficient) type and it is connected to the external pull-up resistor. Note that the voltage variation of the VFO pin, which is generated by the thermistor temperature change, should be always higher than the fault detection level of the micro controller. In this reference board, the pull-up resistor is set to 3.6kΩ so that the VFO voltage becomes 2.95V and 1.95V respectively for 5V and 3.3V control voltage (Vctr) when the thermistor temperature is 100°C, as shown in Figure 9.

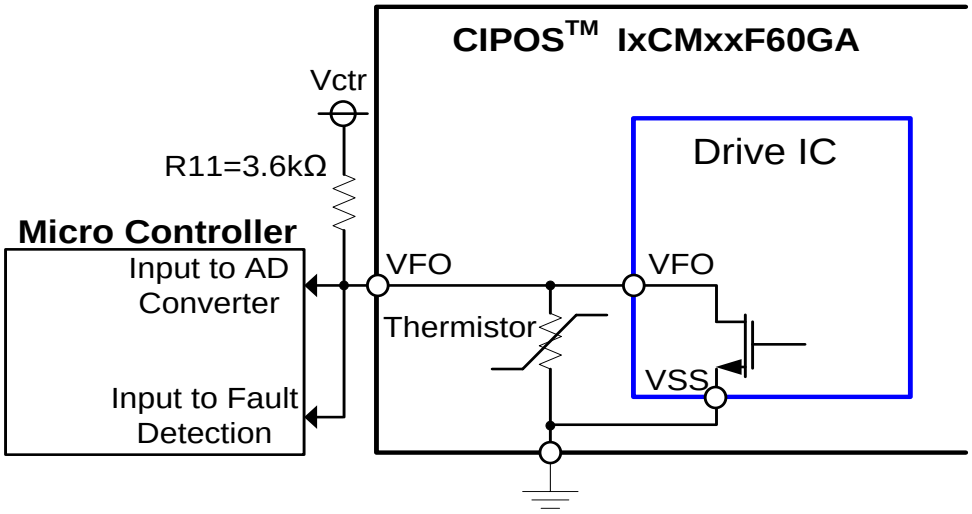


Figure 8 Temperature monitor with built in thermistor and pull up resistor

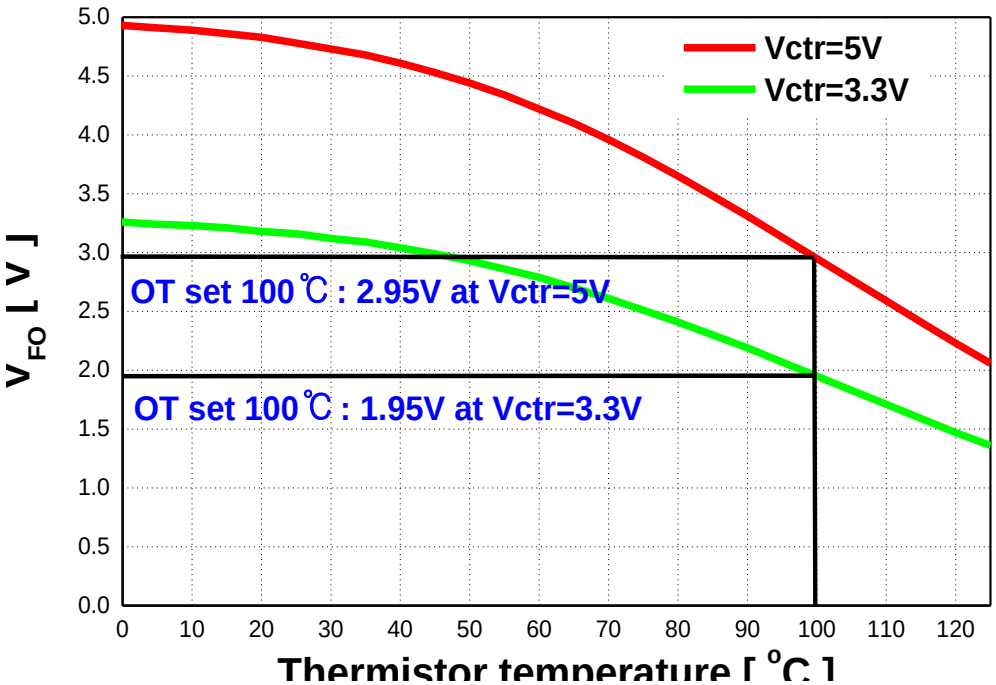


Figure 9 Voltage variation of the VFO along with the NTC thermistor temperature change

5 Part List

Table 6 Part list (Only for reference. Supplier can be changed.)

Symbol	Components	Description	Supplier
R1 ~ R6	100Ω, 1/8W, 5%	Series resistors for input voltage	Walsin
R7 ~ R9	No Connection	See note below	-
R10	1.8kΩ, 1/8W, 1%	Series resistor for current sensing voltage	Walsin
R11	3.6kΩ, 1/8W, 1%	Pull-up resistor for fault output voltage	Walsin
R12	1kΩ, 1/8W, 5%	Series resistor for fault output voltage	Walsin
R13	Content 4.4.1	Current sensing resistor	Vishay
C1 ~ C6	1nF, 25V	Bypass capacitors for input voltage	Walsin
C7 ~ C9	0.1uF, 25V	Bypass capacitors for high side bias voltage	Walsin
C10 ~ C12	22uF, 35V	Bootstrap capacitors	Samyoung
C13	100uF, 35V	Source capacitor for 5 or 3.3V supply voltage	Samyoung
C14	0.1uF, 35V	Bypass capacitor for 5 or 3.3V supply voltage	Walsin
C15	220uF, 35V	Source capacitor for VDD supply voltage	Samyoung
C16	0.1uF, 35V	Bypass capacitor for VDD supply voltage	Walsin
C17	1nF, 25V	Bypass capacitor for current sensing voltage	Walsin
C18	1nF, 16V	Bypass capacitor for fault output voltage	Walsin
C19	1nF, 16V	Bypass capacitor for fault output voltage	Walsin
C20	0.1uF, 630V	Snubber capacitor	Pilkor
D1 ~ D3	No Connection	See note below	-
J1	SMW250-11P	Signal & Power supply connector	Yeonho
U, V, W, P, N	Fasten Tap	Power terminals	KET

Note: It is optional to use external bootstrap circuit together with internal one, in case that smaller bootstrap resistor is necessary.

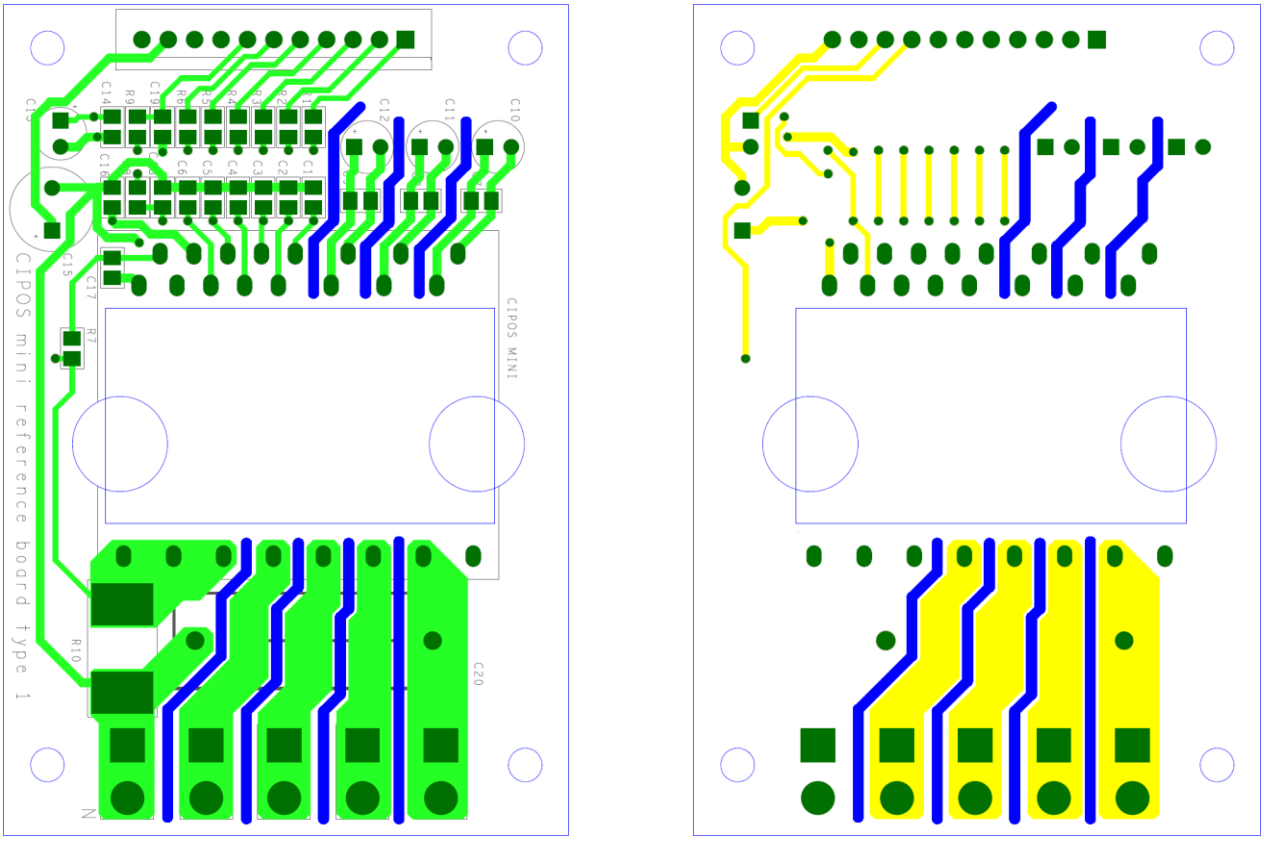
6 PCB Design Guide

In general, there are several issues to be considered when designing a switching power supply application.

- Low stray inductive connection
- Isolation distance
- Component placement

This chapter will explain about the items above and come up with the solutions for the better layout design.

6.1 Layout of Reference Board



Top view Bottom view (transparent)

Figure 10 Layout of reference board type 1 for 1-shunt resistor

1. *The connection between emitters of CIPOS™ Mini inverter IPM (N) and current sensing resistor should be as short and as wide as possible.*
2. *It is recommended that the ground pin of the micro-controller should be directly connected to the VSS pin. Signal ground and power ground should be as short as possible and connected at only one point via the VDD capacitor (C16).*
3. *All of the bypass capacitors should be placed as close to the pins of CIPOS™ Mini inverter IPM as possible.*
4. *The capacitor (C17) for voltage sensing of the current sensing resistor should be placed as close to ITRIP and VSS pins as possible.*
5. *In order to accurately detect the voltage of the current sensing resistor, both sensing and ground patterns should be connected at the pins of the current sensing resistor and should not be overlapped with any patterns for the load current, as shown in Figure 10.*

6. *The snubber capacitor (C20) should be placed as close to the power terminals as possible.*
7. *The PCB routings for power pins such as P, U, V, W and N should be placed on both top and bottom layers with vias to allow high current flowing. They have to keep the minimum isolation distance among the power patterns. The distance should be at least over than 2.54mm.*
8. *Note that there are milling profiles in blue lines on the board to keep the isolation distance*
9. *All components except the CIPOS™ Mini inverter IPM are placed on the top layer.*

7 Reference

[1] Infineon Power Semitech: CIPOS™ Mini IGCM10F60GA; Datasheet Ver. 1.6; Infineon Power Semitech, 2014

Revision History

Major changes since the last revision

Page or Reference	Description of change
Ver1.0, Mar.2012 All pages	First release
Ver1.1, Aug.03.2016 Page 2 Page 12 All pages All pages	Figure 1 Reference board pictures replaced Figure 10 Reference board layout pictures replaced Minor typo fixed Template changed
Ver1.11, Sep.09.2016 All pages	Minor typo fixed

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