4.1.7 Registers to Read OTP Data

The following are used for reading the OTP data:

`otp_addr` - is the address of the data to read

`otp_data` - is the data once read

`otp_read_en` - must be set to 1 to initiate a read; this bit is auto cleared

`otp_busy` – indicates the OTP is busy. For normal I2C reads, the data will be available by the time the read enable bit is set and the data is read, so in most cases this bit is not needed.

The table below is the map for OTP memory. Registers 0x04 – 0x0F correspond to the I2C registers and are loaded at power up or wake from sleep. If the bit `Usestore` is set, then the first two registers are not reloaded on a wake from sleep.

OTP BYTE	7	6	5	4	3	2	1	0
0x04	sw_low4field	sw_op						
0x05	sw_fieldpolsel		sw_hyst					
0x06	sltime							
0x08	sw_tamper						slfast	sltimeena
0x09	power up a0							
0x0A	power up a1							
0x0B	power up a2							
0x0C	df_burstsize			df_bw				df_iir
0x0D	power up a3							
0x0E	power up a4							
0x0F	power up a5							
0x14	Base part number dropping the “Si72”, for example 01 for Si7201							
0x15	Variant according to data sheet represented in hex., for example, variant 50 is 0x32							
0x16 – 0x17	Reserved							
0x18 – 0x1B	4 byte serial number							
0x1C	Reserved							
0x1D	Temperature sensor offset adjustment							
0x1E	Temperature sensor gain adjustment							
0x20	On chip field generator calibration. This is a signed integer BperVcal in the range of ±127.							
0x21 - 0x26	a0 – a5 for 20 mT scale and no magnet temperature compensation							
0x27 - 0x2C	a0 - a5 for 200 mT scale and no magnet temperature compensation							
0x2D - 0x32	a0 – a5 for 20 mT scale at 25°C -0.12%/°C magnet temperature compensation (Neodymium)							
0x33 - 0x38	a0 – a5 for 200 mT scale at 25°C -0.12%/°C magnet temperature compensation (Neodymium)							
0x39 - 0x3E	a0 – a5 for 20 mT scale at 25°C -0.2%/°C magnet temperature compensation (Ceramic)							
0x3F - 0x44	a0 – a5 for 200 mT scale at 25°C -0.2%/°C magnet temperature compensation (Ceramic)							

4.1.8 Control of On-Chip Test Coil

`tm_fg` - Test Field Generator Coil

tm_fg	Current in coil
00b	None
01b	Positive direction
10b	Negative direction
11b	None

Avoid transitions between states 1 & 2, due to a possible short term high current spike.

The nominal magnetic field output of the on chip generator varies with coil current. The coil current varies with coil resistance and power supply voltage, so the nominal magnetic field output varies according to

$$Bout = BperVnom \times \left(1 + \frac{BperVcal}{256}\right) \times V_{DD}$$

BperVnom is [TBD in the range of 20 mT]

This can be used to calculate the expected magnetic field from the test coil for a given V_{DD}. This is somewhat temperature dependent so the actual measured field will vary according to the accuracy of the part as well as temperature. Generally, as the coil is turned on and off the measured variation in field should be within ±25% of expectation based on the calculated field generation.

5. Making Temperature Measurements

Every magnetic field conversion has an associated temperature measurement. During magnetic field measurement cycles, this data is used for compensating the hall sensor data to keep the desired temperature coefficient of magnetic field measurement.

The temperature data is available by setting the `dspsigsel` field of register 0xC3 to 0x01.

Once the `dspsigsel` field is set, the temperature sensor data is read from registers 0xC1 and 0xC2 as 15b unsigned number (see also 4.1.2 Fields Associated with Reading DATA).

The temperature sensor data can be read after one conversion or after a burst of conversions.

Note: The temperature sensor data is not averaged after performing a burst. Only the magnetic field data is averaged.

The data in 0xc1 and 0xc2 is combined into a 12 bit signed number:

$$value = 32 \times Dspigm[6:0] + (Dspisigl[7:0] >> 3)$$

$$Temperature\_raw = -2.1 \times 10^{-6} value^2 + 0.1522 \times value - 273$$

The data read in this way does not have offset and gain correction applied. The offset and gain correction is stored in registers 0x1D and 0x1E which are read as signed integers.

$$Offset = \frac{signed\_value(0x1D)}{16}$$

$$Gain = 1 + \frac{signed\_value(0x1E)}{2048}$$

And finally

$$Temperature = gain \times (Temperature\_raw) + offset$$

Typically, the gain and offset terms are calculated only once and then are saved. The temperature measurement circuit has noise and quantization errors of approximately ±0.3°C. Adding averaging to the calculated temperature will reduce these errors.

6. Pin Description

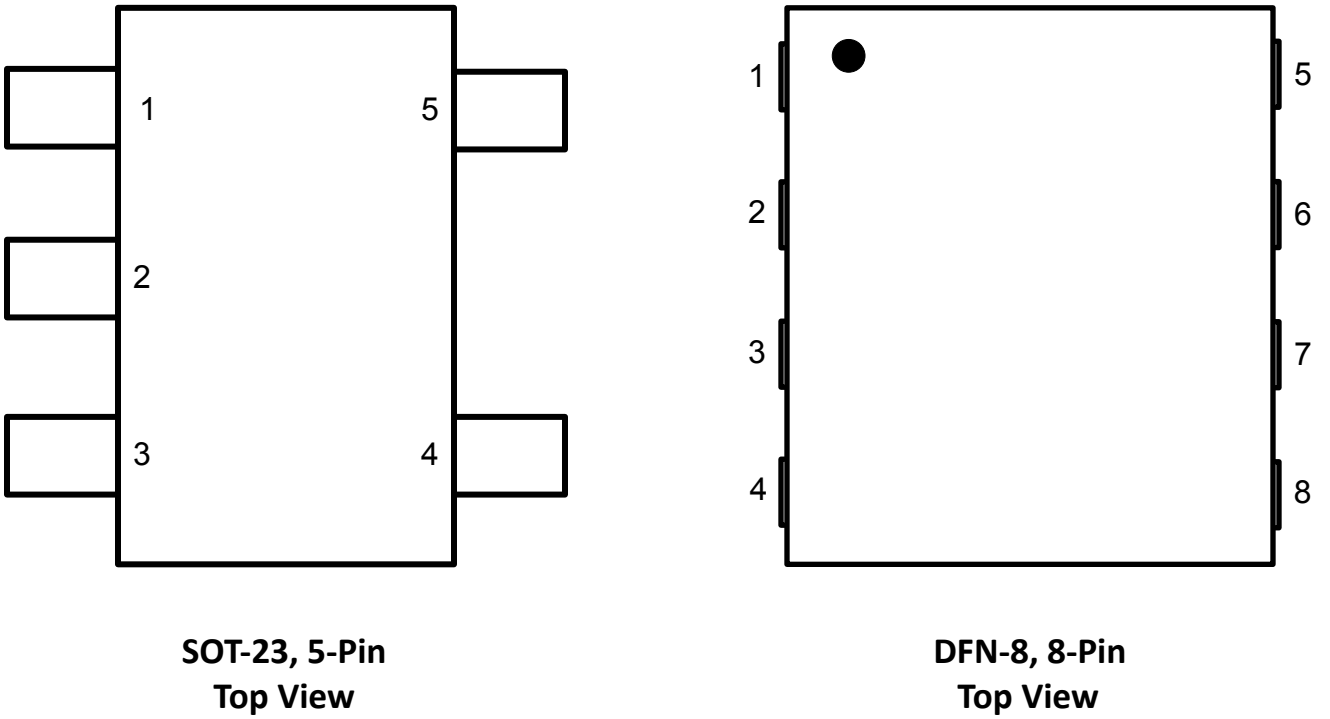


Figure 6.1. Pin Assignments

Table 6.1. Five-Pin

Pin name	Pin number	Description
SDA	1	I²C data
GND	2	Ground
SCL	3	I²C clock
V_{DD}	4	Power +1.7 to +5.5 V
ALERT/VOUT	5	Analog or digital ouput

Table 6.2. Eight-Pin

Pin name	Pin number	Description
GND	1, 5	Ground
SCL	2	I²C SCL
NC	3, 7	Not connected
SDA	4	I²C SDA
OUT	6	OUTPUT pin

7. Ordering Guide

Part Number	Deafault Output Polarity (high field)	IDD (typ. @3.3V)	Default BOP, BRP	Sleep/ Idle Time	Temper-ature Com-pensa-tion	Temper-ature accura-cy	Tamper Thresh-old	Digital Filtering	I2C Ad-dress	VDD	Pack-age	Temper-ature Rating
Si7210-B-00-IV(R)	High (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±1.0 °C	19.84 mT	None	0x30	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-01-IV(R)	Low (open drain)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±1.0 °C	19.84 mT	None	0x30	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-02-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	19.84 mT	None	0x31	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-03-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x32	1.7 - 5.5 V	SOT23-5	-40°C - 125°C
Si7210-B-04-IV(R)	Low (push-pull)	0.4 µA	BOP = ±1.1 mT (max) BRP = ±0.2 mT (min) | BOP - BRP| = 0.4 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x33	1.7 - 5.5 V		

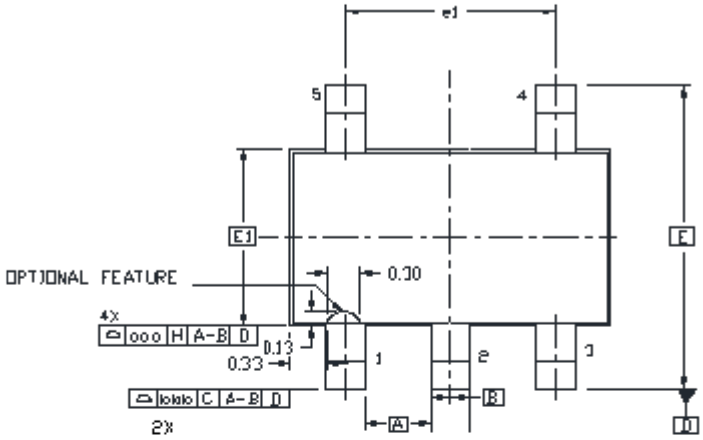
Part Number	Deafault Output Polarity (high field)	IDD (typ. @3.3V)	Default BOP, BRP	Sleep/ Idle Time	Temper-ature Com-pensa-tion	Temper-ature accura-cy	Tamper Thresh-old	Digital Filtering	I2C Ad-dress	VDD	Pack-age	Temper-ature Rating
Si7210-B-05-IV(R)	Low (push-pull)	0.4 µA	BOP = ±2.15 mT (max) BRP = ±0.35 mT (min) | BOP - BRP| = 0.8 mT (typ)	200 msec (sleep)	None	±4.0 °C	None	None	0x33	1.7 - 5.5 V	SOT23-5	-40°C - 125°C

Note:

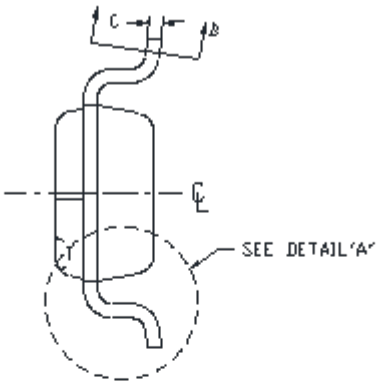
1. All I2C parts have the base part number Si7210. A is the die revision. The next two digits are used with this look up table to give more specific information. E is the temperature range (-40 to +150°C). M or V is the package type (DFN or SOT23) the optional (R) is the designator for tape and reel (xx pieces per reel). Parts not ordered by the full reel will be supplied in cut tape.
2. North pole of a magnet at the bottom of a SOT23 package is defined as positive field.

8. Package Outline

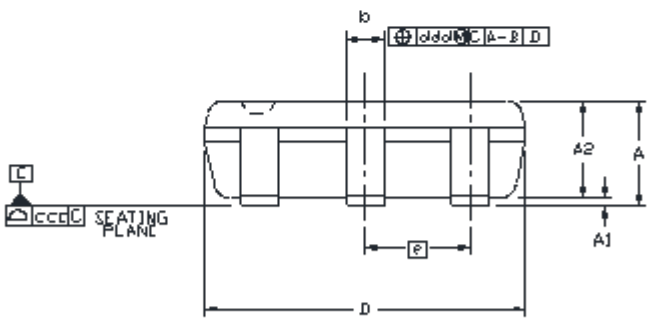
8.1 SOT23 3-Pin Package



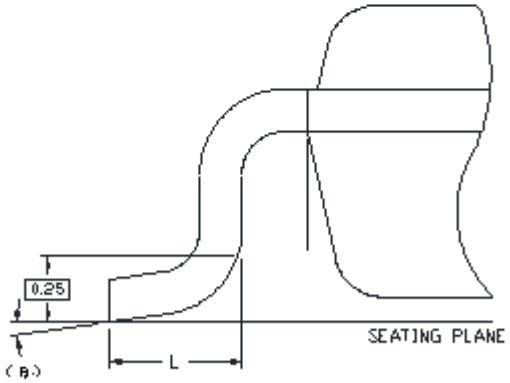
TOP VIEW
6 LEAD



END VIEW



SIDE VIEW
6 LEAD



DETAIL "A"

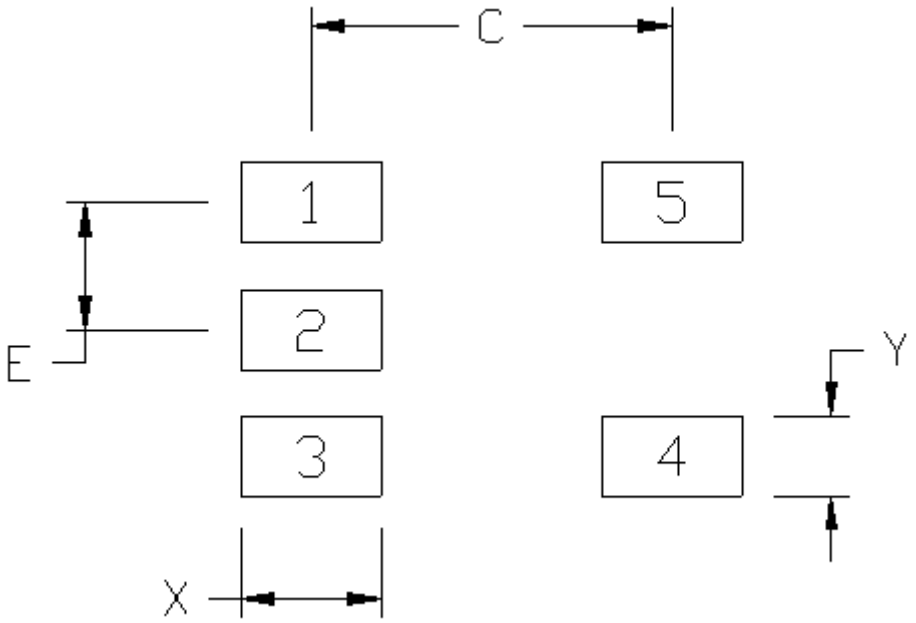
Dimension	MIN	MAX
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.80 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.15	
ccc	0.10	
ddd	0.20	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

9. Land Patterns

9.1 SOT23 Five-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Note:

General

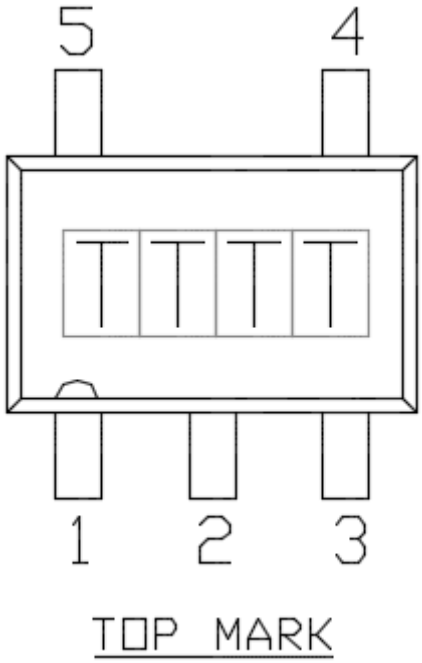
1. 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

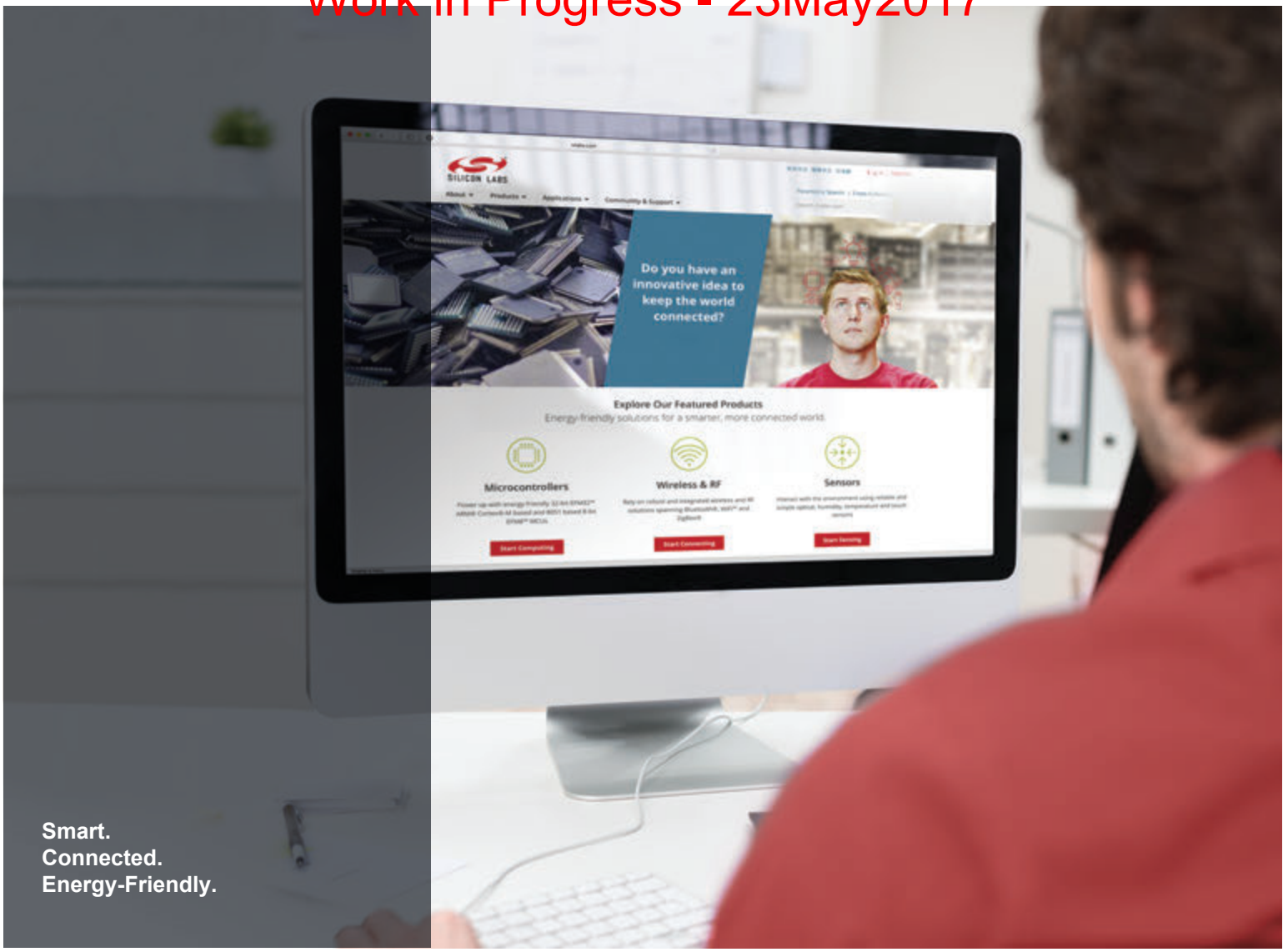
Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

10. Top Marking

10.1 SOT23 5-Pin Topmarking





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