ESD242-B1-W01005

Protection Devices

TVS (Transient Voltage Suppressor)
Bi-directional, 3.3 V, 6 pF, 01005, RoHS and Halogen Free compliant

Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD): ±18 kV (air / contact discharge)
  - IEC61000-4-4 (EFT): ±2 kV / ±40 A (5/50 ns)
  - IEC61000-4-5 (Surge): ±4.5 A (8/20 µs)
- Bi-directional working voltage up to: V_{RWM} = ±3.3 V
- Line capacitance: C_L = 6 pF (typical) at f = 1 MHz
- Clamping voltage: V_{CL} = 6 V (typical) at I_{TLP} = 16 A with R_{DYN} = 0.09 Ω (typical)
- Very low reverse current: I_R < 1 nA (typical)
- Small form factor SMD Size 01005 and low profile 0.43 mm x 0.23 mm x 0.15 mm
- Bi-directional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package

RoHS

Guidelines for optimized PCB design and assembly process are available in *[2]*.

Potential applications

- IC/ASICs in audio, headset
- Human digital interfaces, buttons, GPIO

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

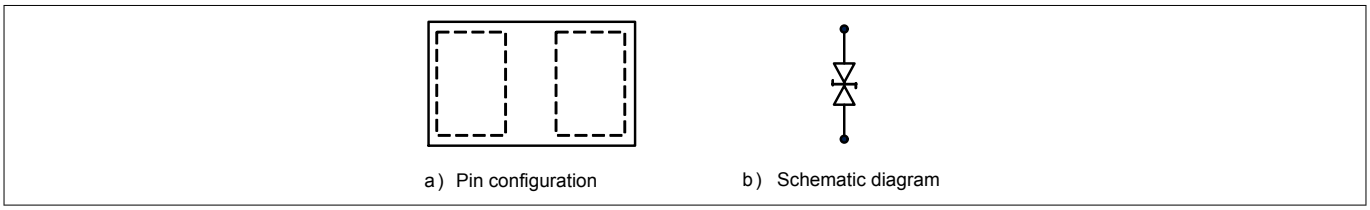

Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD242-B1-W01005	WLL-2-2	1 line, bi-directional	AC [1)]

1 The device does not have any marking on the device top. The marking code is on the pads.

Table of contents

1 Maximum ratings

Note: *T_A = 25 °C, unless otherwise specified*

Table 2 Maximum ratings[1)]

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±3.3	V
ESD discharge [2)]	V_{ESD} (contact)	±18	kV
	V_{ESD} (air)	±18	
Peak pulse power [3)]	P_{PK}	25	W
Peak pulse current [3)]	I_{PP}	±4.5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: ***Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.***

1 Device is electrically symmetrical
2 V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)
3 Stress pulse: 8/20µs current waveform according to IEC61000-4-5

2 Electrical characteristics

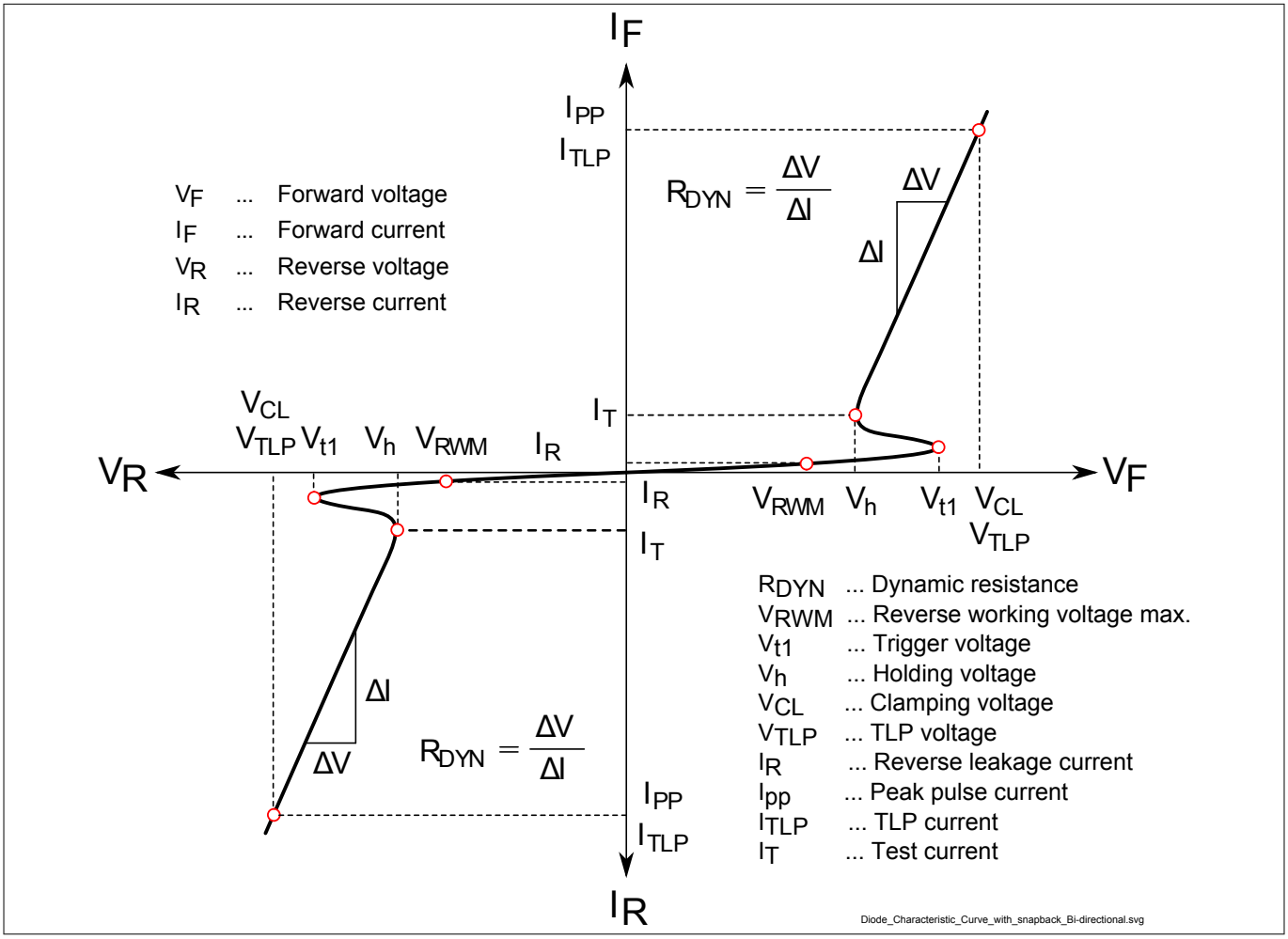

Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics (T_A = 25 °C, unless otherwise specified) [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Trigger Voltage[2)3)]	V_{t1}	5	6	–	V	–
Holding voltage[4)]	V_h	4	5.7	7.2	V	I_R = 1 mA
Reverse current	I_R	–	1	30	nA	V_R = 3.3 V

Table 4 AC characteristics (T_A = 25 °C, unless otherwise specified) [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	6	–	pF	V_R = 0 V, f = 1 MHz
		–	6	–		V_R = 0 V, f = 1 GHz

Table 5 ESD and Surge characteristics (T_A = 25 °C, unless otherwise specified) [1)]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage [5)]	V_{CL}	–	6	–	V	I_{TLP} = 16 A, t_p = 100 ns
		–	7	–		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage [6)]		–	5	–		I_{PP} = 1 A, t_p = 8/20 µs
		–	6	–		I_{PP} = 4 A, t_p = 8/20 µs
Dynamic resistance [5)]	R_{DYN}	–	0.09		Ω	t_p = 100 ns

1 Device is electrically symmetrical
2 Verified by design
3 Voltage forced
4 Current forced
5 Please refer to Application Note AN210 *[1]*. TLP parameters: Z_0 = 50 Ω , t_p = 100ns, t_r = 0.6 ns.
6 Stress pulse: 8/20µs current waveform according to IEC61000-4-5

3 Typical characteristic diagrams

Note: *T_A = 25 °C, unless otherwise specified*

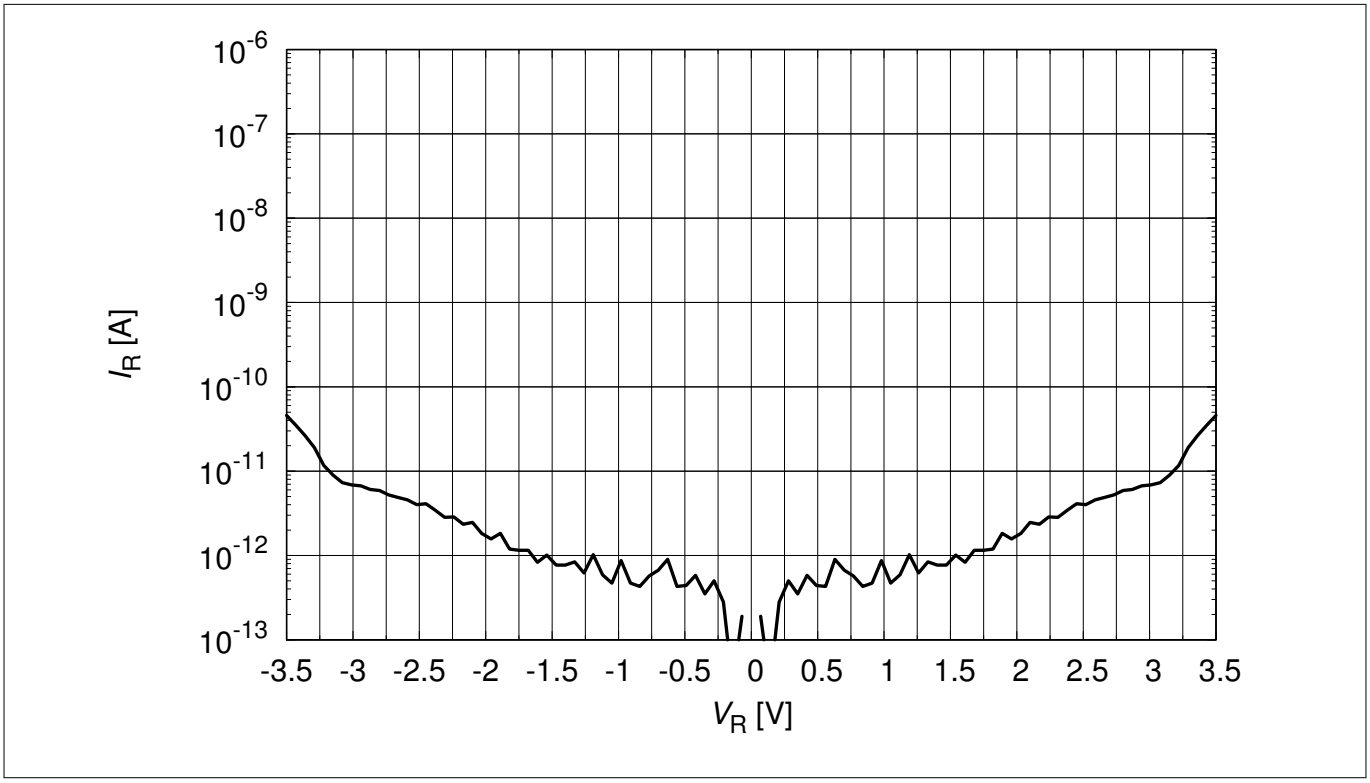

Figure 3 Reverse leakage current: $I_R = f(V_R)$

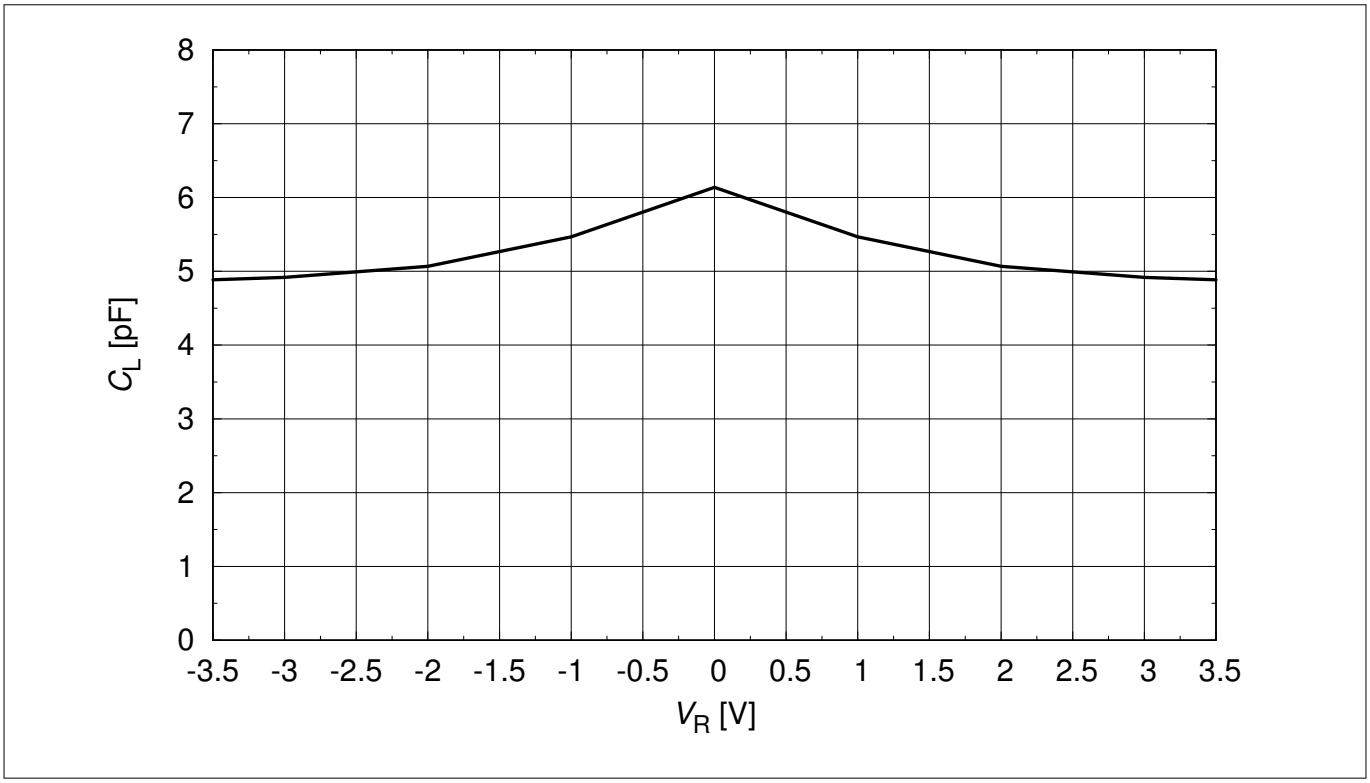

Figure 4 Line capacitance: $C_L = f(V_R)$, f = 1 MHz

Typical characteristic diagrams

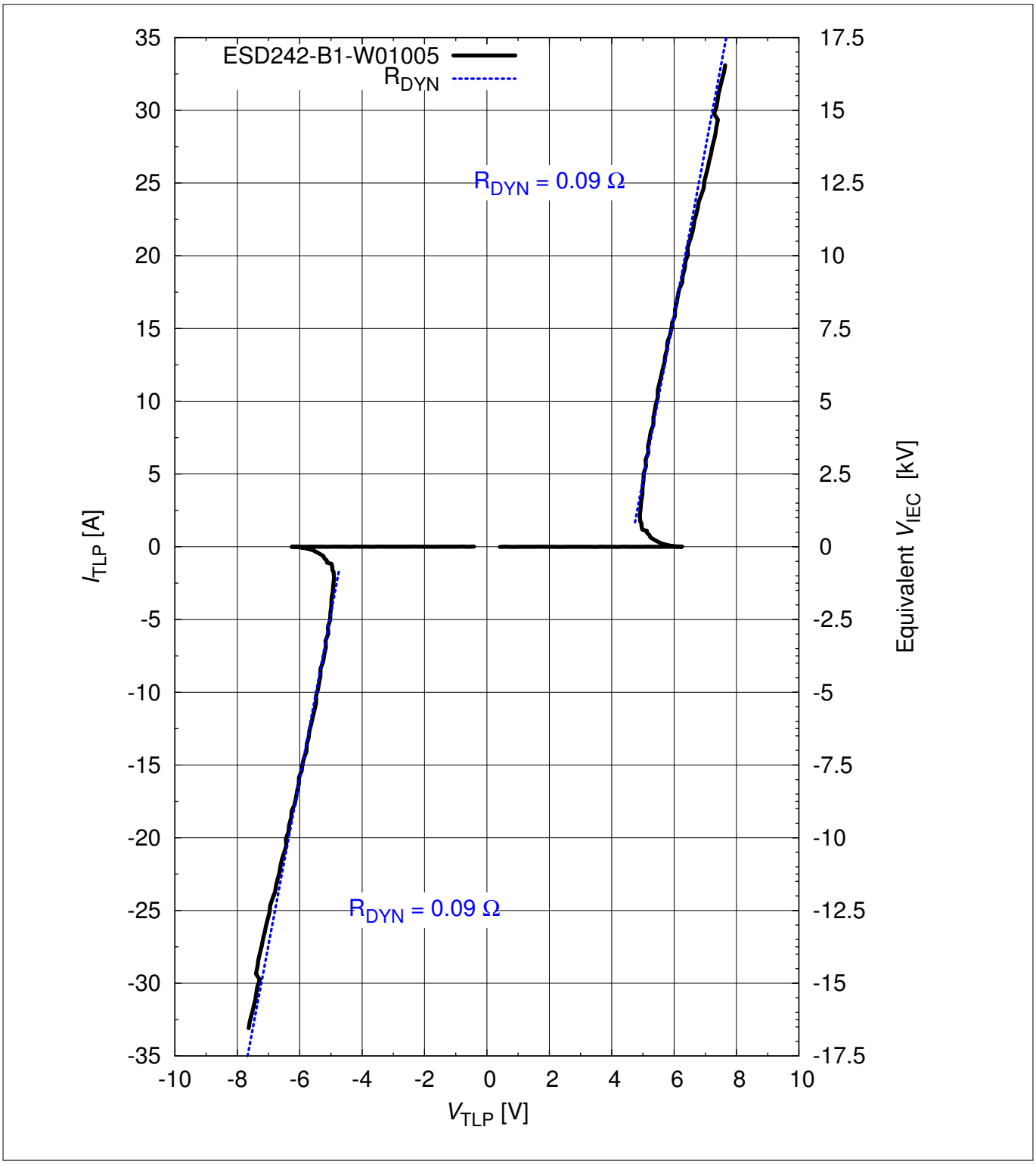

Figure 5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ *[1]*

Typical characteristic diagrams

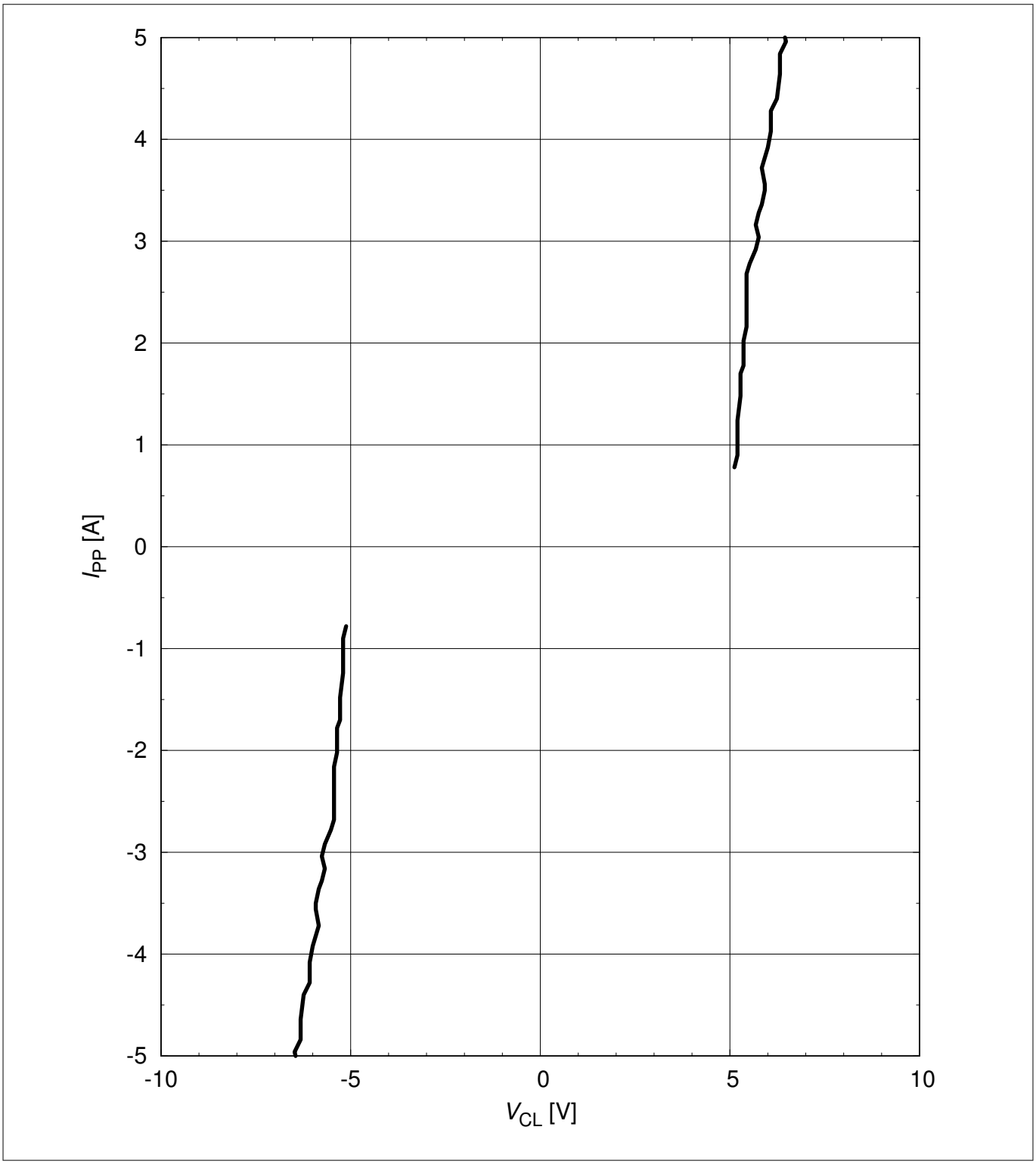

Figure 6 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ *[1]*

4 Package information

4.1 WLL-2-2 package

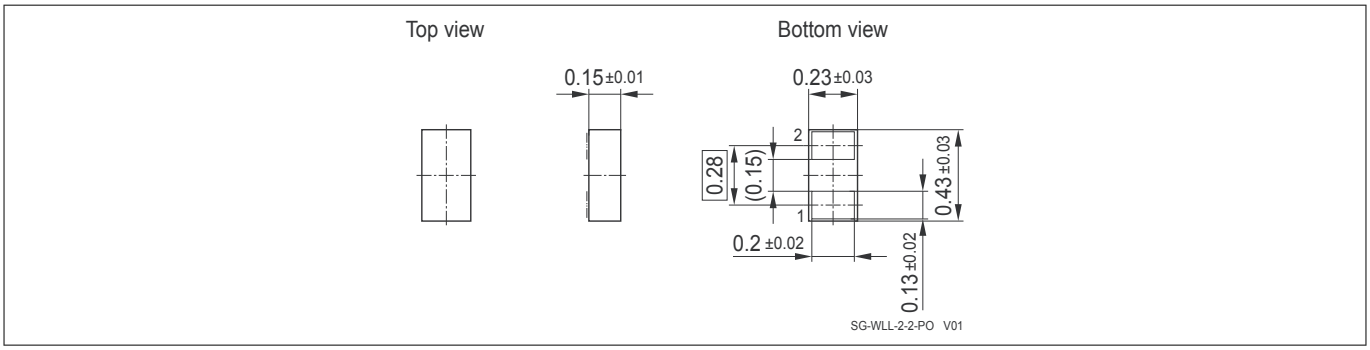

Figure 7 WLL-2-2 package outline (dimension in mm)

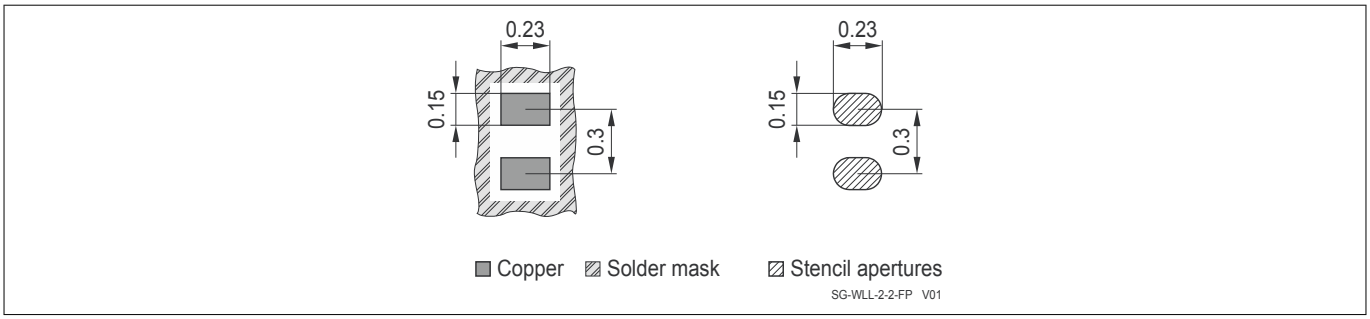

Figure 8 WLL-2-2 footprint (dimension in mm), recommendation for Printed Circuit Board assembly see *[2]*

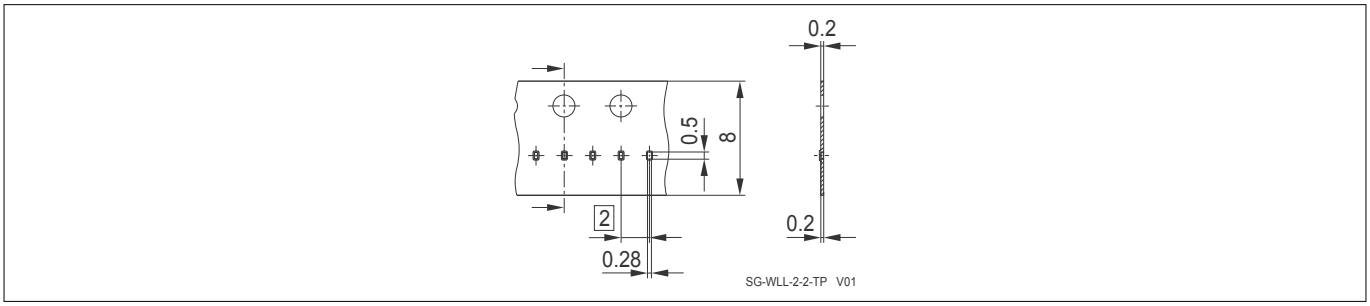

Figure 9 WLL-2-2 packing (dimension in mm)

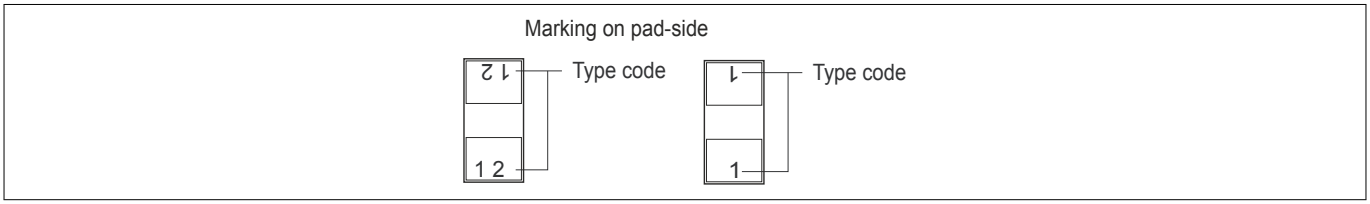

Figure 10 WLL-2-2 marking example (see *Table 1*)

5 References

[1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL

[3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Rev. 0.9.1, 2016-01-25	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2017-06-26	
All	Final datasheet

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