Three-Phase Brushless Motor Predriver

BD63001AMUV

General Description

BD63001AMUV is a Three-Phase Brushless Motor Predriver that uses upper Pch and lower Nch MOS transistor for an external output power transistor. It generates a driving signal from the Hall sensor and drives PWM through the input control signal. In addition, the supply voltage that can be applied is 12V or 24V, it has various controls and built-in protection functions, making it useful for a variety of purposes. Since the IC adopts small packages, it can be used on small diameter motors.

Features

- Built-in 120° Commutation Logic Circuit
- Drives Upper Pch, Lower Nch MOS transistor
- PWM control system /DC control system
- CW/CCW Function
- FG Output (1FG Output)
- Current Limit Protection Circuit (CL)
- Overheat Protection Circuit (TSD)
- Under Voltage Protection Circuit (UVLO)
- Over Voltage Protection Circuit (OVLO)
- Motor Lock Protection (MLP)

Application

- OA apparatus
- Other general public welfare apparatus

Key Specifications

- Power Supply Voltage Rating: 3 3 V
- Operating temperature range: -40°C to +85°C
- Predriver Output Current Rating(Continuous) : ±30mA
- Predriver Output Current Rating(Peak) (Note 1) : ±200mA
- The Current Limit Detect Voltage: 0.2V±10%
- UVLO Lockout Voltage: 3.7V(Typ)

(Note1) tw≦1μs, 50kHz

Package W(Typ) x D(Typ) x H(Max)

VQFN024V4040
4.00mm x 4.00mm x 1.00mm

Typical Application Circuits

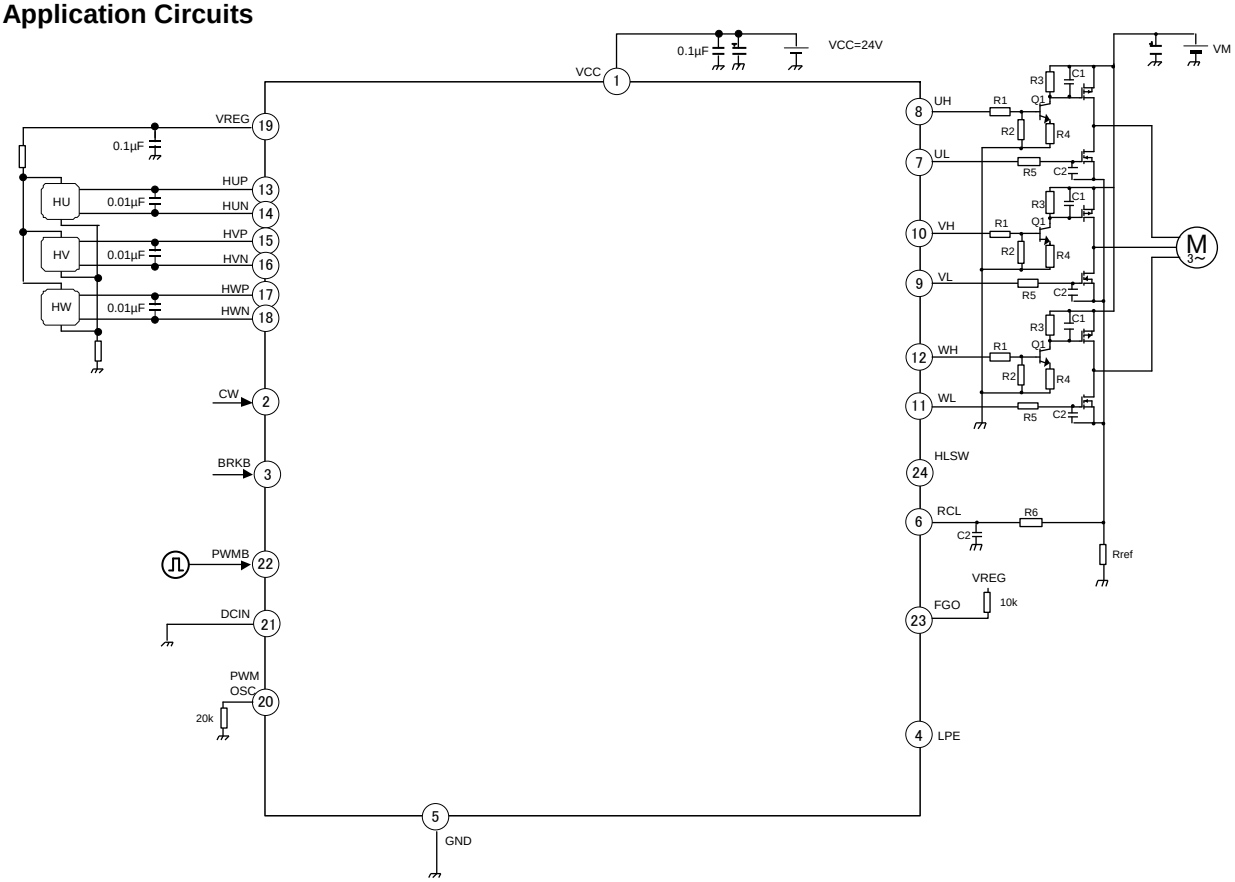


Figure 1. Application Circuit in HLSW=OPEN ("H")

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuits - continued

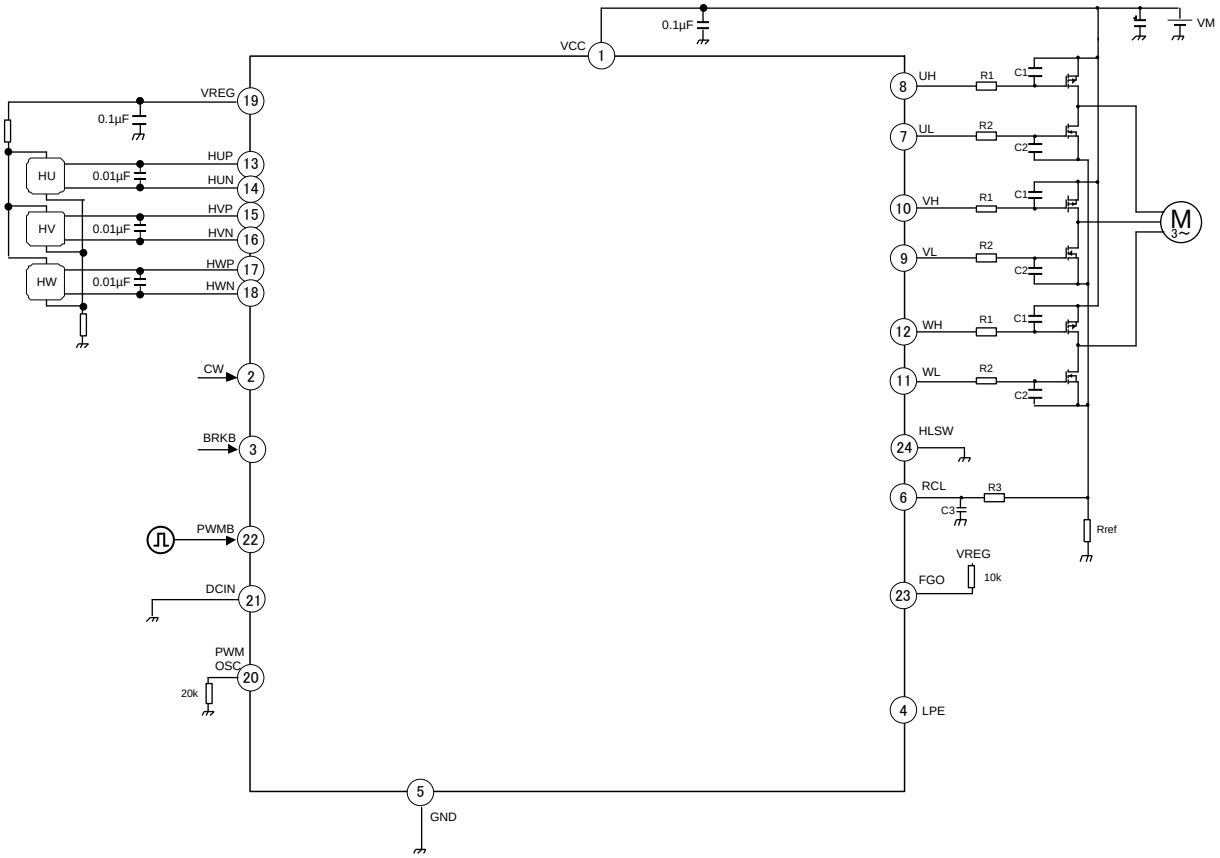


Figure 2. Application Circuit in HLSW="L"

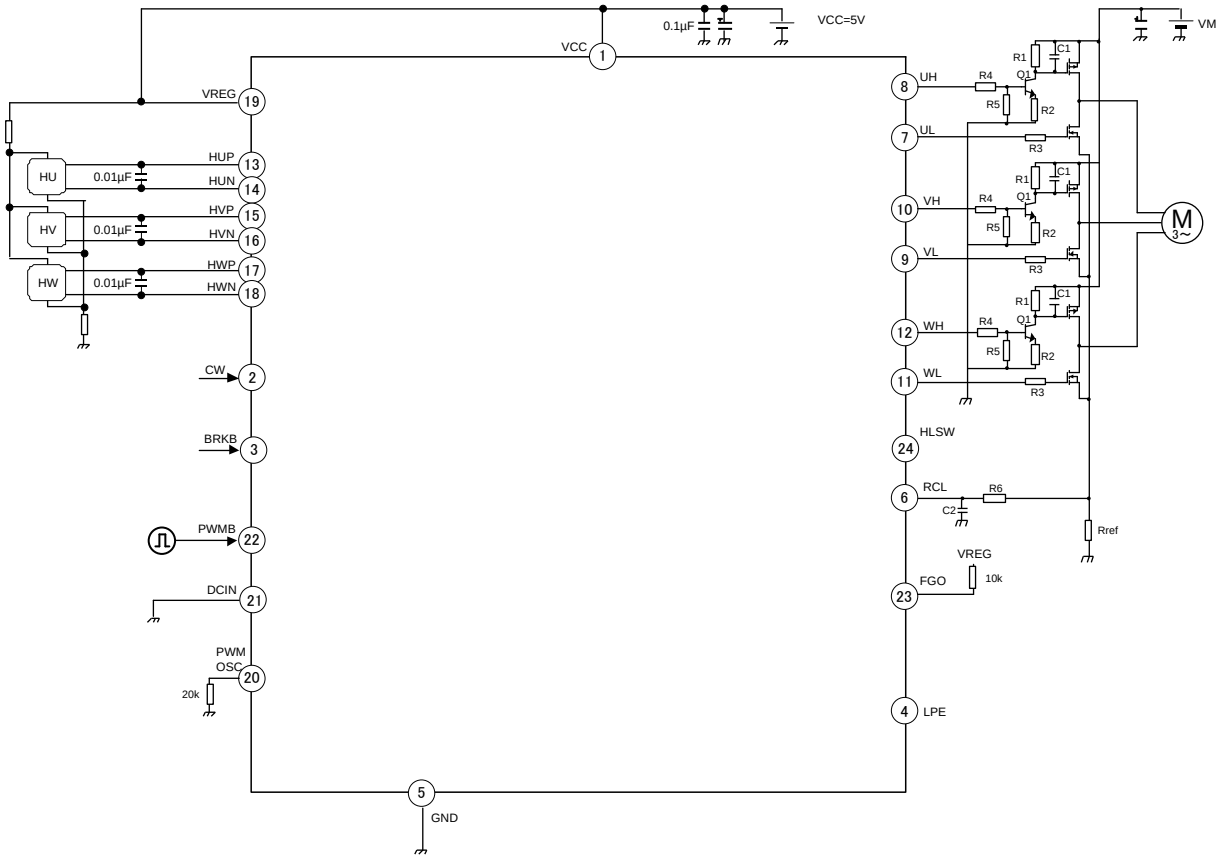


Figure 3. Application Circuit in VCC=VREG

Contents

Pin Configuration

(TOP VIEW)

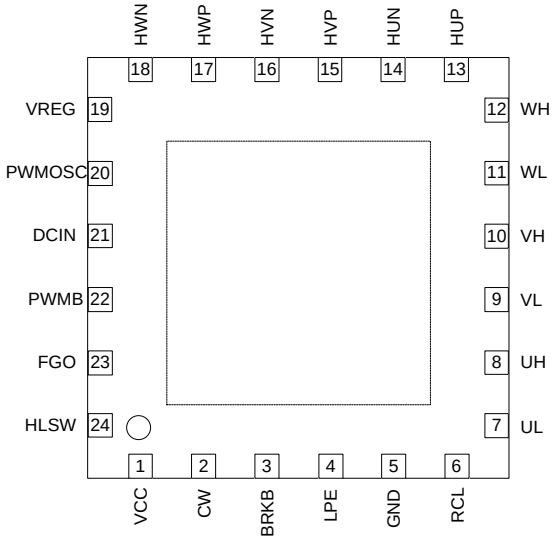


Figure 4. Pin Configuration

Block Diagram

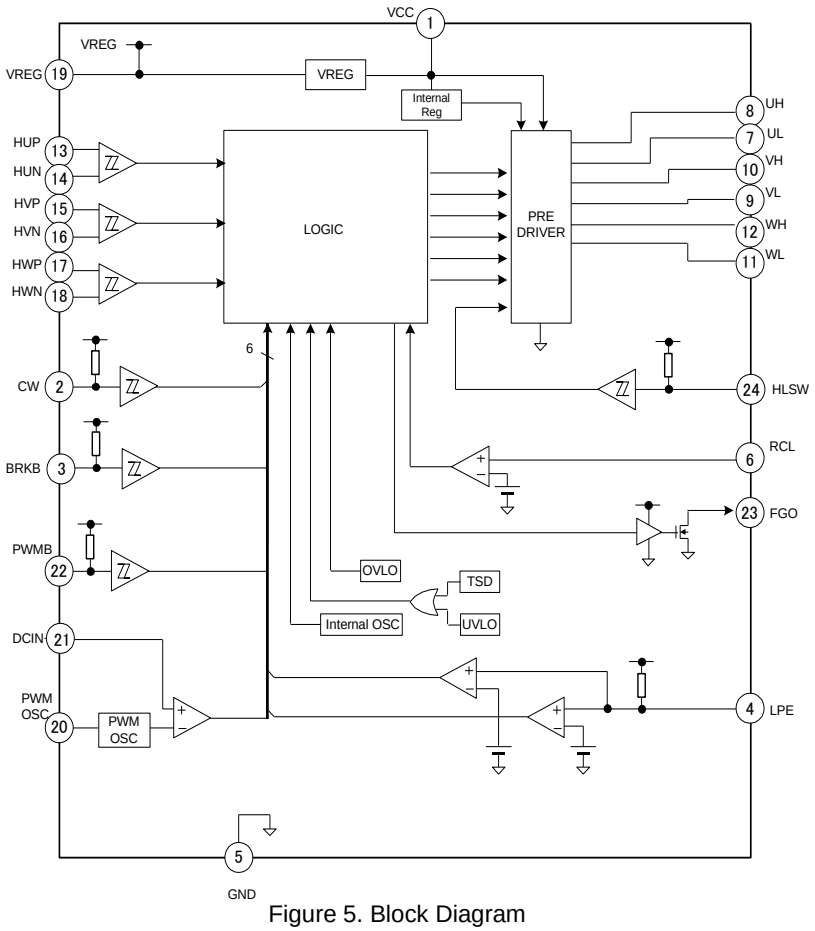


Figure 5. Block Diagram

Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	VCC	Power Supply	13	HUP	U Phase Hall Input +
2	CW	CW/CCW Input (H:CW, L:CCW)	14	HUN	U Phase Hall Input -
3	BRKB	Brake Input (negative logic)	15	HVP	V Phase Hall Input +
4	LPE	Motor Lock Protection Setting (H/M/L input)	16	HVN	V Phase Hall Input -
5	GND	Ground	17	HWP	W Phase Hall Input +
6	RCL	Detect Voltage Input for Over-Current	18	HWN	W Phase Hall Input -
7	UL	Output UL	19	VREG	Regulator Output
8	UH	Output UH	20	PWMOSC	Setting PWM Oscillator Frequency
9	VL	Output VL	21	DCIN	DC Input
10	VH	Output VH	22	PWMB	PWM Input (negative logic)
11	WL	Output WL	23	FGO	FG(1 phase output)
12	WH	Output WH	24	HLSW	Upper MOS Gate Output Switch

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{CC}	-0.3 to +33.0	V
Predriver Output Voltage	$V_{(UH,VH,WH)}$	-0.3 to +V_{CC}	V
Predriver Output Voltage	$V_{(UL,VL,WL)}$	-0.3 to +10.5	V
FGO Terminal Voltage	V_{FGO}	-0.3 to +7.0	V
Other Input and Output Terminal Voltages	$V_{I/O}$	-0.3 to +5.5	V
Predriver Output Current (Continuous)	I_{OUT1}	±30	mA
Predriver Output Current (Peak)	I_{OUT2}	±200 (Note 1)	mA
FGO Output Current	I_{FGO}	5	mA
VREG Output Current	I_{VREG}	-30	mA
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Junction Temperature	Tjmax	150	°C

(Note 1) tw≤1μs,50kHz

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC1}	6	24	28	V
Supply Voltage(V_{REG}=V_{CC})	V_{CC2}	4.5	5	5.5	V

Thermal Resistance (Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s (Note 3)	2s2p (Note 4)	
VQFN024V4040				
Junction to Ambient	θ_{JA}	150.6	37.9	°C/W
Junction to Top Characterization Parameter (Note 2)	Ψ_{JT}	20	9	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4)Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Function Description

1. Commutation Logic
This IC adopts a 120° commutation mode, and the truth table is as follows:

(1) HLSW="H" or OPEN

HU	HV	HW	CW (CW="H" or OPEN)						CCW (CW="L")						
			UH	UL	VH	VL	WH	WL	UH	UL	VH	VL	WH	WL	FGO
H	L	H	L	PWM	H	L	L	L	H	L	L	PWM	L	L	L
H	L	L	L	PWM	L	L	H	L	H	L	L	L	L	PWM	L
H	H	L	L	L	L	PWM	H	L	L	L	H	L	L	PWM	L
L	H	L	H	L	L	PWM	L	L	L	PWM	H	L	L	L	Hi-z
L	H	H	H	L	L	L	L	PWM	L	PWM	L	L	H	L	Hi-z
L	L	H	L	L	H	L	L	PWM	L	L	L	PWM	H	L	Hi-z

(2) HLSW="L"

HU	HV	HW	CW (CW="H" or OPEN)						CCW (CW="L")						
			UH	UL	VH	VL	WH	WL	UH	UL	VH	VL	WH	WL	FGO
H	L	H	H	PWM	L	L	H	L	L	L	H	PWM	H	L	L
H	L	L	H	PWM	H	L	L	L	L	L	H	L	H	PWM	L
H	H	L	H	L	H	PWM	L	L	H	L	L	L	H	PWM	L
L	H	L	L	L	H	PWM	H	L	H	PWM	L	L	H	L	Hi-z
L	H	H	L	L	H	L	H	PWM	H	PWM	H	L	L	L	Hi-z
L	L	H	H	L	L	L	H	PWM	H	L	H	PWM	L	L	Hi-z

(Note) When PWMB="H", PWM="L", When PWMB="L", PWM="H"

Caution: In the following sentence, Upper side predriver output is under the condition of HLSW=OPEN (or "H").
In HLSW="L", the output H/L of Upper side predriver becomes the reverse.

2. Regulator Output Terminal (VREG)
This is a constant output voltage terminal of 5V (Typ). It is recommended to connect capacitors of 0.01µF to 1µF.
Please be careful that VREG current should not exceed the maximum ratings in case it will be used for supply voltage of hall elements.

3. PWM Input Terminal (PWMB)
Speed can be controlled by inputting Duty of PWM signal into PWMB (negative logic). When PWMB="L", lower side predriver output that corresponds to the Hall input logic is "H". In addition, PWMB terminal is pulled up to VREG through a resistance of 100kΩ(Typ) ±30kΩ. When using PWM input, please use it with DC input under 1V (Typ) or short to GND.

PWMB	Lower Side Predriver Output Logic
H or OPEN	L
L	H

4. DC Input Terminal (DCIN)
Speed can be controlled by the DC signal to input into DCIN.
PWM signal becomes 100% duty at DCIN=3.0V (Typ) and becomes 0% duty at DCIN= 1.0V (Typ). When using DC input, please use it with PWMB input "H" or OPEN.

DCIN	Duty
1V(Typ)	0%
3V(Typ)	100%

5. PWMOSC Input Terminal (PWMOSC)
When using DC input, the PWM frequency f_{PWM} [kHz] is fixed by an external resistor R [kΩ] connected to PWMOSC.
F_{PWM} [kHz] = 400/R

Function Description – continued

6. CW/CCW Input Terminal (CW)
Rotation direction can be switched with CW terminal. When CW=”H” or OPEN, the direction is CW. When CW=”L”, the direction is CCW. However, we do not recommend changing the direction of rotation while the motor is rotating. This is because if direction of rotation is changed while rotating, the rotation speed becomes equal to the hall frequency, which is less than approximately 40Hz (Typ). After a short brake, the rotation direction will switch to a new setting. In addition, CW terminal is pulled up to VREG through a resistance of 1010kΩ (Typ) ±300kΩ.

CW	Direction
H or OPEN	CW
L	CCW

7. Brake Input Terminal (BRKB)
Motor rotation can be quickly stopped by BRKB terminal (negative logic). When BRKB=”L”, all upper side predriver outputs are “H” and all lower side predriver outputs are “L” (short brake). When BRKB=”H” or OPEN, then the short brake action is released. In addition, BRKB terminal is pulled up to VREG through a resistance of 100kΩ (Typ) ±30kΩ.

BRKB	Operation
H or OPEN	Normal
L	Short brake

8. Hall Input (HALL: HUP, HUN, HVP, HVN, HWP, HWN)
Hall input amplifier inside the IC is designed with a hysteresis (±12mV(Typ)) in order to prevent false trigger due to noise. Always set correct bias current for the Hall element so that the amplitude of Hall input voltage will be over the minimum input voltage ($V_{HALLMIN}$). It is recommended to connect a ceramic capacitor with about 100pF to 0.01µF value between the input terminals of the Hall amplifier. The in-phase input voltage range ($V_{HALLCM1}$:0V to V_{REG}-1.7V, $V_{HALLCM2}$:0V to V_{REG}) is designed for Hall input amplifier, set within this range when applying bias to the Hall element.
Moreover, “H” or “L” of HU, HV ,HW in Commutation Logic means the following.

HU	HV	HW	HUP	HUL	HVP	HVN	HWP	HWN
H	L	H	H	L	L	H	H	L
H	L	L	H	L	L	H	L	H
H	H	L	H	L	H	L	L	H
L	H	L	L	H	H	L	L	H
L	H	H	L	H	H	L	H	L
L	L	H	L	H	L	H	H	L

When HU, HV ,HW become all “H” or all “L”, a circuit will detect these Hall input abnormalities and make all upper side predriver outputs “L” and all lower side predriver output “L”.

9. FG Output Terminal (FGO)
1FG signal that is controlled by hall signal is output from FGO terminal. In addition, because FG terminal is an open drain terminal, use a resistor of about 10kΩ to 100kΩ pulled up to supply voltage. In that case, please be careful that FGO voltage or current should never exceed rating.

Function Description – continued

10. Power Supply Terminal (VCC)
    (1) When IC is operated in 4.5V to 5.5V, VCC is short to VREG and connected to the power supply. In 6V to 28V, connect a power source only to VCC.

    (2) Stabilize VCC voltage by placing a bypass capacitor near the terminal, as much as possible, in case VCC voltage might change considerably by motor BEMF and PWM switching. Increase capacitance of the capacitor as necessary when drawing large current and motor with large BEMF. Please be careful that VCC voltage never exceeds ratings.

    (3) It is recommended to place a laminated ceramic capacitor of around 0.01µF to 0.1µF in parallel in order to decrease the impedance of power supply broadband.

    (4) VCC terminal has a clamp element for preventing ESD damage. If applying a steep pulse signal and voltage such as it surges more than the ratings, this clamp element operates, which might be a cause of destruction. It is effective to put a ener diode that corresponds to VCC absolute maximum ratings. Please note that IC might be destroyed when the backward voltage is applied to VCC and GND terminals.

11. Ground Terminal (GND)
    Wiring impedance from this terminal should be as low as possible to reduce noise of switching current and stabilizing basic voltage inside the IC; and the impedance should also be the lowest potential in any operating condition. In addition, please do pattern design to not have the common impedance as the other GND pattern

12. Predriver Output Terminal (UH, UL, VH, VL, WH, WL)
    By a driving signal produced with internal logic, the driving signal to an external output power transistor is output. Upper Gate functional voltage is VCC and Lower Gate functional voltage is 9.5V (Typ). Also when V_{CC}=5V, Lower Gate functional voltage is V_{CC}-0.2V (Typ). Additionally, When driver output converts “L” to “H” or “H” to “L”, dead time (1µs(Typ)) can be set to prevent simultaneous ON of external upper and lower FET.

13. Comparator Input Terminal for Detecting Output Current (RCL)
    When operating with current limit, please be sure to connect RNF and RCL. In addition, please do not have the same impedance as other GND patterns by using low impedance wiring, since motor drive current flows into the RCL terminal resistor for detecting current to GND. Please design pattern considering wiring that is less influenced by noise. Additionally, when RCL terminal is shorted to GND, large current might flow due to a lack of normal current limit operation.

14. H Side Output Logic Switching Terminal (HLSW)
    By changing HLSW, the gate logic of the upper output is changed. In HLSW=”L”, the gate logic of upper output is inverted. In addition, HLSW terminal is pulled up to VREG through a resistance of 200kΩ (Typ) ±60kΩ.

15. Control Signal Sequence
    It is recommended that input control signals DCIN, PWMB, CW terminals are turned ON after inputting VCC. If LPE terminal is set to “H” or “M” at startup, please take note that if motor rotation cannot be detected within the set time (edge of FG signal cannot be input), then the MLP circuit starts and motor fails to start. The order of priority is to set control signal and IC internal signal. Please refer to the following table.

Priority of Control Signal

Priority	Input / Internal Signals
1st	UVLO
2nd	BRKB↑↓,CW↑↓,PWMB↓ ,DCIN↑
3rd	TSD,MLP,HALLERR
4th	OVLO
5th	BRKB
6th	CL
7th	PWM,CW,HLSW,DCIN

(Note) ↑↓ means rising and falling edges of signal.
For signal name, please refer to state transition diagram.

Protection Circuit

(1) Current Limit Circuit (CL Circuit)
Current limit of output (Current limit: CL) can be realized by changing the voltage of the output current with a resistor, and then by inputting the voltage into the RCL terminal. In order to avoid error detection of current detection comparator by RCL spike noise that occurs at output ON, mask time is set. Current detection is invalid during mask time after RCL voltage becomes more than 0.2V (Typ). Then all lower side predriver outputs are “L”, and they are returned automatically after the specified time (32µs (Typ)). This operation is not synchronized with PWM signal that is input into PWMB terminal. Moreover, if it happens that the noise is longer than the 0.5µs (Typ) internal mask time, set mask time using external low pass filter.

(2) Thermal Shutdown Circuit (TSD Circuit)
When chip temperature of driver IC rises and exceeds the set temperature (175°C (Typ)), the thermal shut down circuit (Thermal Shut Down: TSD) activates. At this time, all the upper side predriver outputs become “L” and all the lower side predriver outputs become “L”. In addition, the TSD circuit is designed with a hysteresis (25°C (Typ)), therefore, when the chip temperature drops, it will return to normal working condition. However, the purpose of the TSD circuit is to protect driver IC from a thermal breakdown, therefore, temperature of this circuit will be over working temperature when it is started up. Thus, thermal design should have sufficient margin, avoid continuous use and action of the circuit as a precaution.

(3) Under Voltage Lock Out Circuit (UVLO Circuit)
There is a built-in under voltage lock out circuit (Under Voltage Lock Out: UVLO circuit) used to ensure the lowest power supply voltage for drive IC to work and to prevent error action of the IC. When VCC voltage declines to V_{UVL} (3.7V (Typ)), all the upper side predriver outputs become “L” and all the lower side predriver outputs become “L”. At the same time, UVLO circuit is designed with hysteresis, so when VCC voltage reaches more than V_{UVH} (4.15V (Typ)), it will operate at normal working condition.

(4) Over Voltage Lock Out Circuit (OVLO Circuit)
There is a built-in over voltage lock out circuit (Over Voltage Lock Out: OVLO) used to prevent rise of V_{CC} when motor is decelerating. When V_{CC} is over V_{OVH} (31V (Typ)), a certain time (4ms (Typ)) of short brake action is conducted. What’s more, because OVLO circuit is designed with hysteresis, when V_{CC} is below V_{OVL} (30V (Typ)), it can return to normal working condition after a certain time of short brake action.

(5) Motor Lock Protection Circuit (MLP Circuit)
There is a built-in motor lock protection circuit (Motor Lock Protection: MLP). The ON/OFF of MLP circuit and monitoring time can be set by the LPE terminal.
In monitoring Hall signals, when the LPE = “H” and Hall signal logic does not change in more than 1.1sec (Typ) or LPE =”M” and Hall signal logic does not change in more than 2.2sec (Typ), all the upper side predriver outputs are locked “L” and all the lower side predriver outputs are locked “L”.

There are four ways to release the latch
(a) The latch is released by Switching BRKB logic
(b) The latch is released by Switching CW logic.
(c) After PWMB = “H” or OPEN state and is detected for 15ms (Typ), latch can be released by falling edges of subsequent PWMB.
(d) After DCIN = GND or under 1V (Typ) state is detected for 15ms (Typ), latch can be released by rising edges of subsequent PWMB.

However, when LPE = “L”, MLP circuit does not work during short brake action (including switching rotation direction) or TSD.
LPE terminal is pulled up to VREG through a resistance of 100kΩ (Typ) ±30 kΩ.

LPE	Monitoring Time
H or OPEN	1.1sec(Typ)±30%
M	2.2sec(Typ)±30%
L	Disable

Electrical Characteristic (Unless otherwise specified Ta=25°C, V_{CC}=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Whole]						
Circuit Current	I_{CC}	-	2.5	5.0	mA	
VREG Voltage	V_{REG}	4.5	5.0	5.5	V	I_{VREG} = -10mA
[Predriver Output]						
Upper Side High Voltage	V_{OHH}	V_{CC}-0.6	V_{CC}-0.2	V_{CC}	V	I_{OUT} = -5mA
Upper Side Low Voltage	V_{OHL}	0	0.2	0.6	V	I_{OUT} = 5mA
Lower Side High Voltage1	V_{OLH1}	8.1	9.5	10.5	V	I_{OUT} = -5mA, No load capacitance
Lower Side High Voltage2	V_{OLH2}	V_{CC}-0.6	V_{CC}-0.2	V_{CC}	V	V_{CC} = 5V, I_{OUT} = 5mA
Lower Side Low Voltage	V_{OLL}	0	0.2	0.6	V	I_{OUT} = 5mA
[Hall Input]						
Input Bias Current	I_{HALL}	-2.0	-0.1	+2.0	µA	V_{HALL} = 0V
Phase Input Voltage Range 1	V_{HALLCM}	0	-	V_{REG}-1.7	V	
Phase Input Voltage Range 2	V_{HALLCM}	0	-	V_{REG}	V	In one side bias (When Hall IC is used)
Minimum Input Voltage	$V_{HALLMIN}$	50	-	-	mV_{P-P}	
Hysteresis	ΔV_{HALL}	15	24	40	mV	
HYS Level +	$V_{HALLHY+}$	5	12	22	mV	
HYS Level -	$V_{HALLHY-}$	-22	-12	-5	mV	
[Input of Control : BRKB]						
Input Current	I_{BRKB}	-80	-50	-30	µA	V_{BRKB} = 0V
Voltage Input H	V_{BRKBH}	2.0	-	V_{REG}	V	
Voltage Input L	V_{BRKBL}	0	-	0.8	V	
Minimum Input Pulse Width	$t_{PLSMIN1}$	1	-	-	msec	
[Input of Control : CW]						
Input Current	I_{CW}	-8	-5	-3	µA	V_{CW} = 0V
Voltage Input H	V_{CWH}	2.0	-	V_{REG}	V	
Voltage Input L	V_{CWL}	0	-	0.8	V	
Minimum Input Pulse Width	$t_{PLSMIN2}$	1	-	-	msec	
[Input of Control : HLSW]						
Input Current	I_{IN}	-40	-25	-15	µA	V_{HLSW} = 0V
Voltage Input H	V_{HLWSHH}	2.0	-	V_{REG}	V	
Voltage Input L	V_{HLSWL}	0	-	0.8	V	
[Input of Control : LPE]						
Input Current	I_{LPE}	-80	-50	-30	µA	V_{LPE} = 0V
Input Voltage “H”	V_{LPH}	0.8×V_{REG}	-	V_{REG}	V	
Input Voltage “M”	V_{LPM}	0.4×V_{REG}	-	0.6×V_{REG}	V	
Input Voltage “L”	V_{LPL}	0	-	0.2×V_{REG}	V	
[Input of Control : PWMOSC]						
External R Inflow Current	I_{RHG}	-30	-20	-10	µA	R = 20kΩ
Oscillator Frequency	f_{PWM}	14	20	26	kHz	R = 20kΩ
[Input of Control : PWMB]						
Input Current	I_{PWMB}	-80	-50	-30	µA	V_{PWMB} = 0V
Voltage Input H	V_{PWMBH}	2.0	-	V_{REG}	V	
Voltage Input L	V_{PWMBL}	0	-	0.8	V	

Electrical Characteristic – continued (Unless otherwise specified Ta=25°C, V_{CC}=24V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Input of Control : DCIN]						
Input Bias Voltage	V_{BIAS}	-1	0	1	μA	V_{DCIN} = 0V
Input Voltage 1	V_{DCIN1}	0.75	1	1.25	V	0% Output duty cycle
Input Voltage 2	V_{DCIN2}	2.75	3	3.25	V	100% Output duty cycle
Phase Input Voltage Range	V_{ICM}	0	-	V_{REG}-1.7	V	
[FGO]						
Output Voltage L	V_{FGOL}	0	0.1	0.3	V	I = 2mA
[Current Limit : RCL]						
Detect Voltage	V_{CL}	0.18	0.20	0.22	V	
[UVLO]						
Release Voltage	V_{UVH}	3.95	4.15	4.35	V	
Lock Out Voltage	V_{UVL}	3.5	3.7	3.9	V	
[OVLO]						
Release Voltage	V_{OVL}	28.0	30.0	32.0	V	
Lockout Voltage	V_{OVH}	29.0	31.0	33.0	V	

Typical Performance Curves

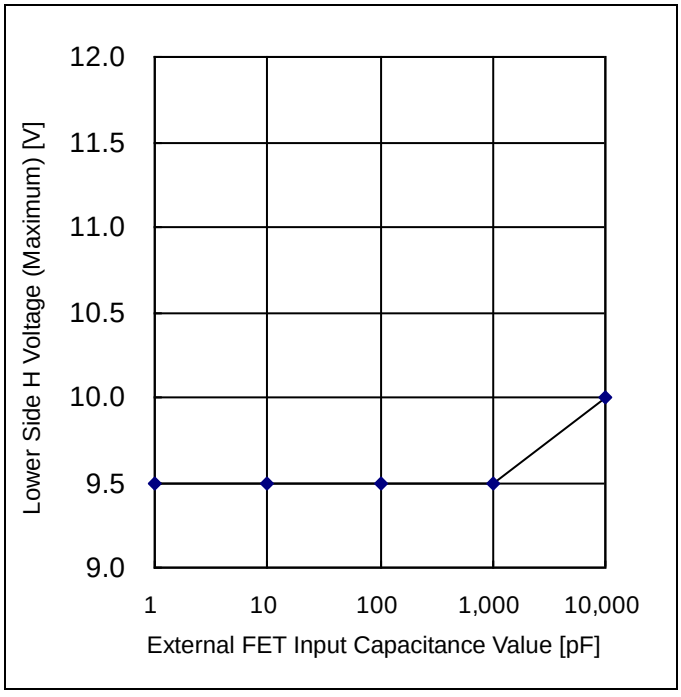


Figure 6. Predriver Lower Side H Voltage (Maximum) vs External FET Input Capacitance Value (V_{CC}=24V, PWMB: 20 kHz, 50%)

Timing Chart

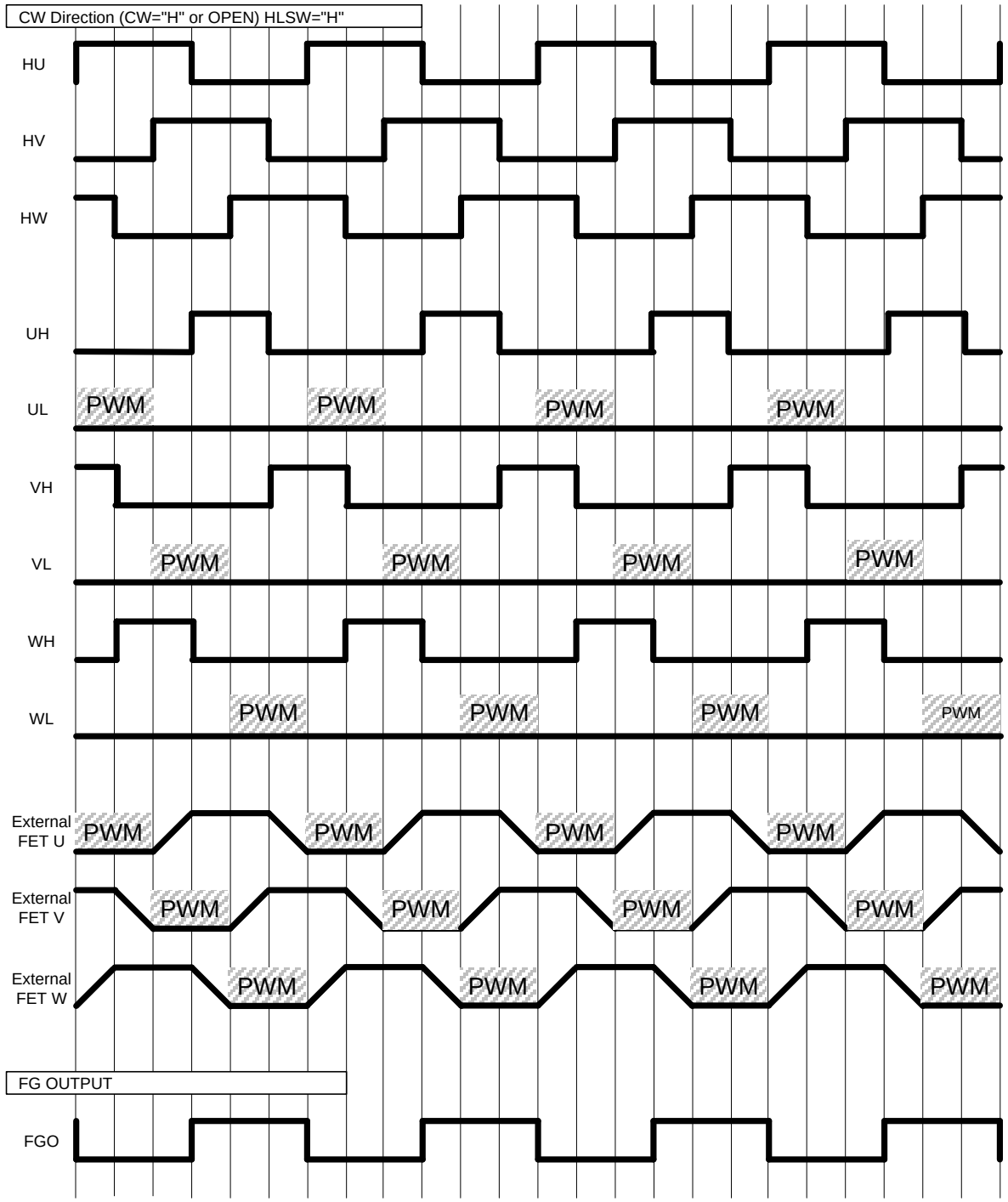


Figure 7. Timing Chart 1

*In HLSW=”L”, the output H/L of UH, VH, WH becomes the reverse.

Timing Chart – continued

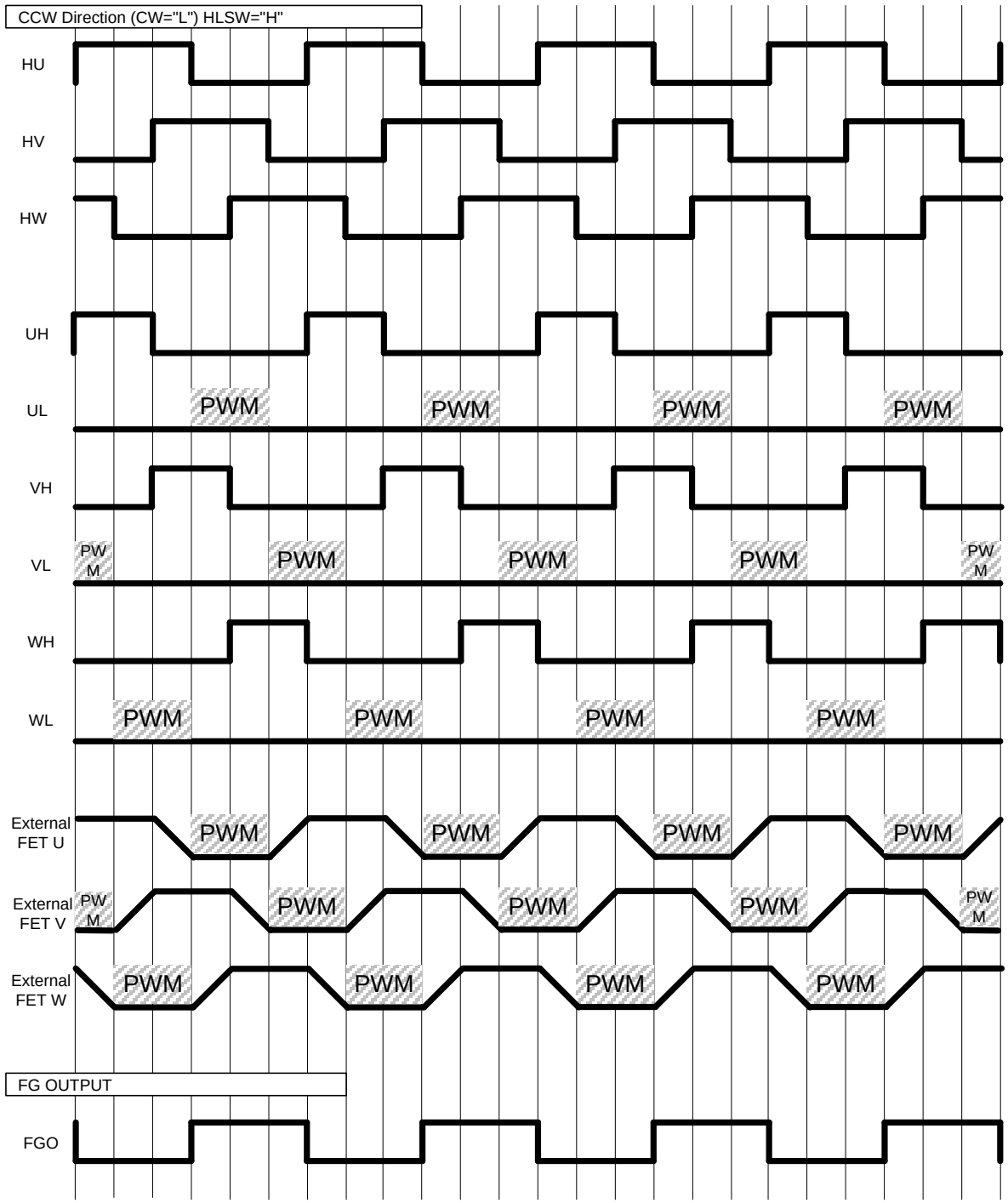


Figure 8. Timing Chart 2

*In HLSW=”L”, the output H/L of UH, VH, WH becomes the reverse.

State Transition Diagram

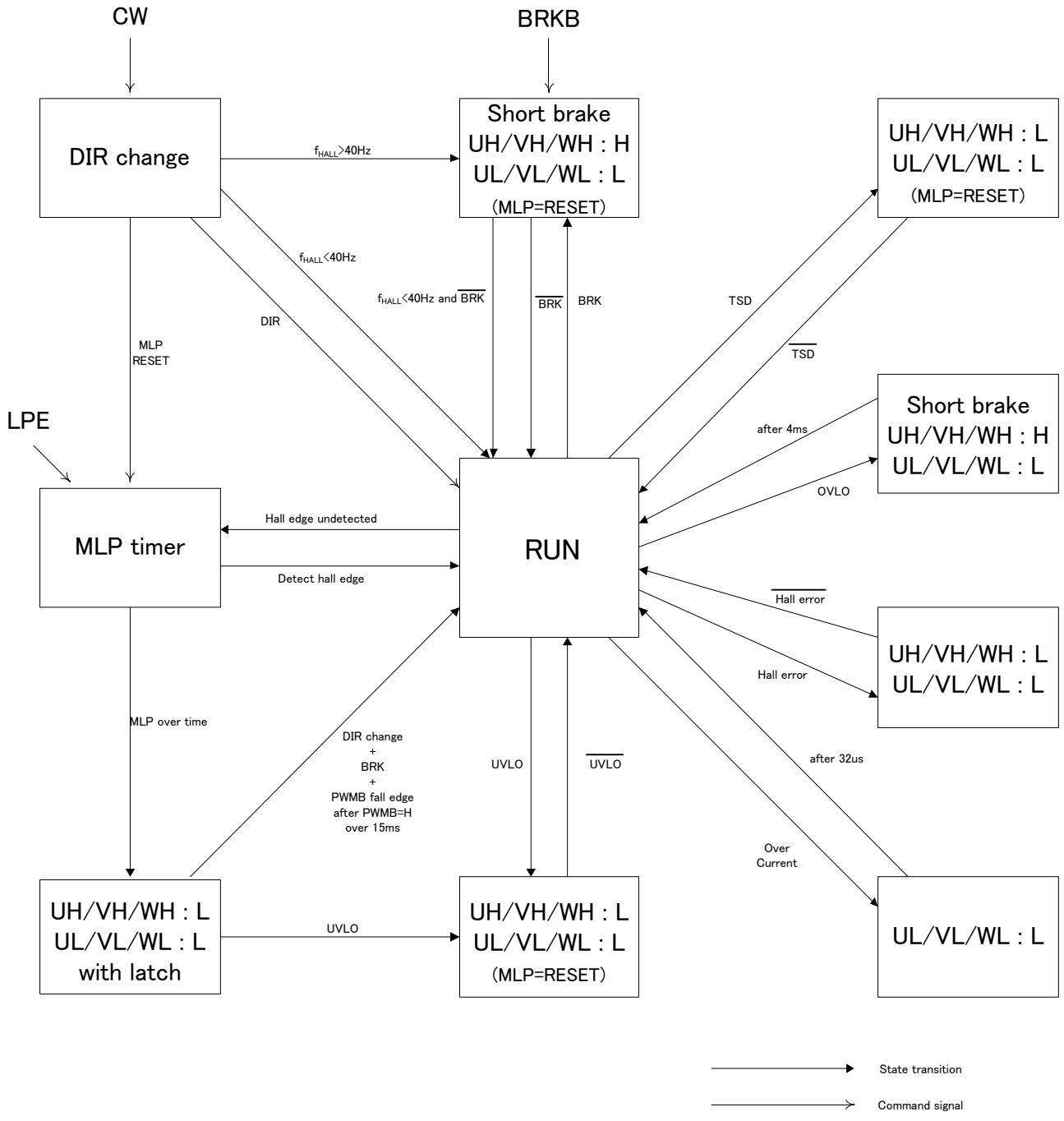


Figure 9. State Transition Diagram

*In HLSW="L", the output H/L of UH, VH, WH become the reverse.

Legend:
DIR: motor rotational direction
MLP: motor lock protection
State transition
f_{HALL}: hall signal frequency
Hall error: HU=HV=HW
&: logical "AND"
+: logical "OR"

(Note) all values are typical

I/O Equivalent Circuits

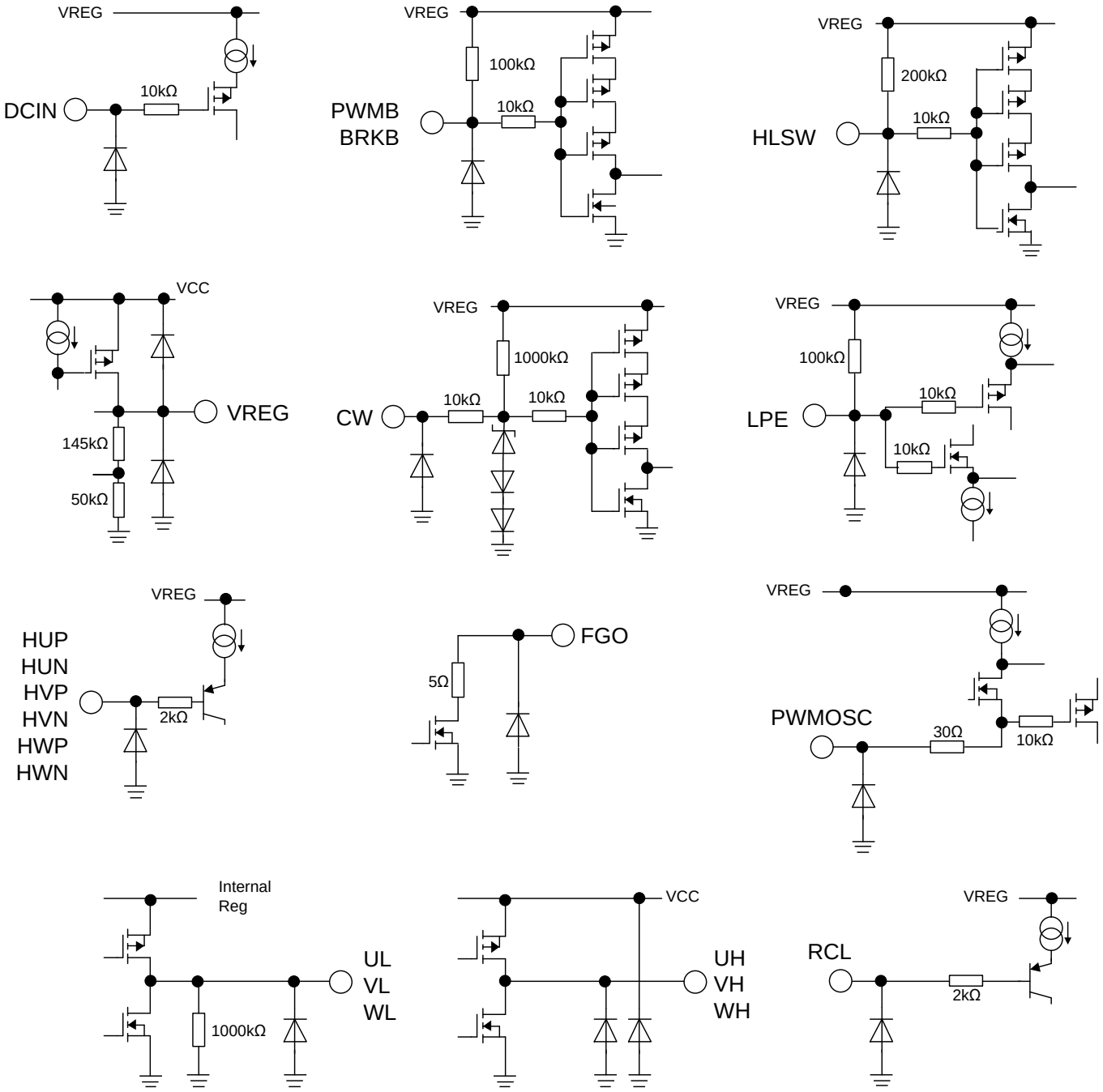


Figure 10. I/O Equivalence Circuits

Attention for Operation

1. Precaution when Current is Pulled from VREG
When current-feed is performed in HALL from VREG, please be careful about the temperature. When the temperature greatly increases, high current flows to HALL, please consider the following circuitry.

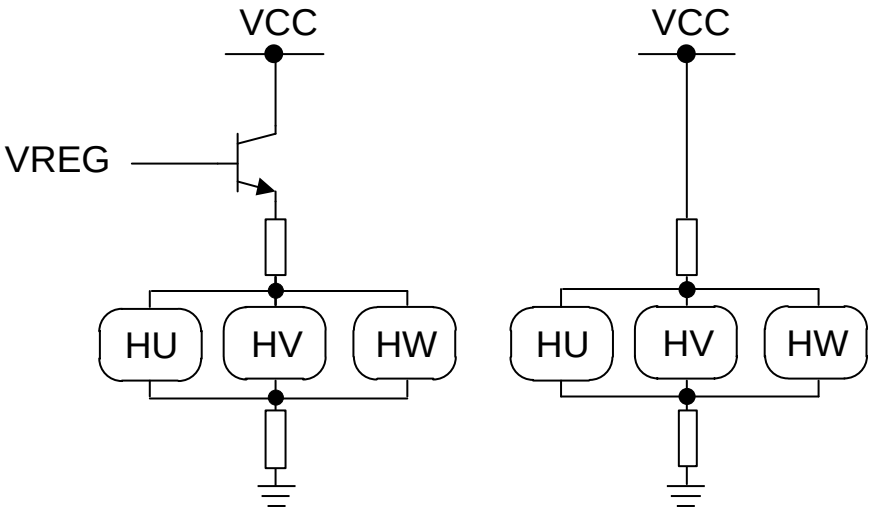


Figure 11. HALL Supply Voltage Reference

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

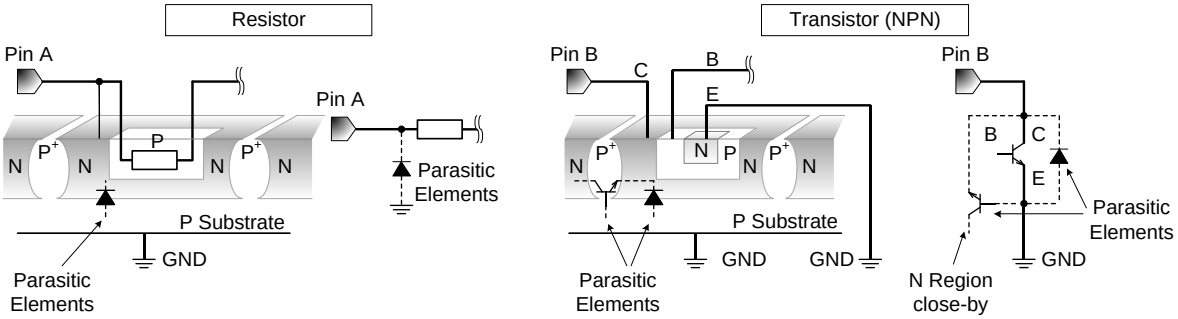


Figure 12. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

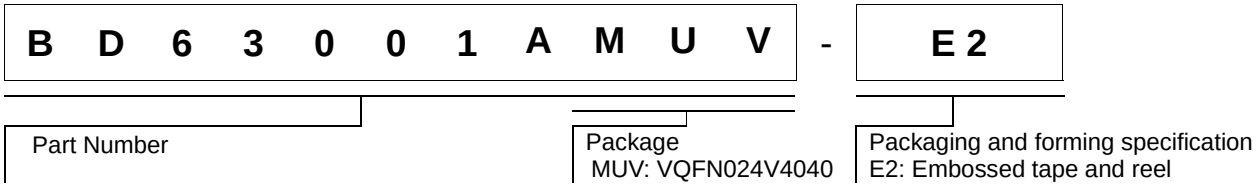
16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

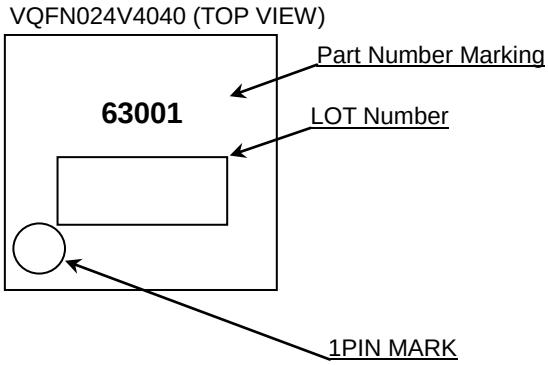
17. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information



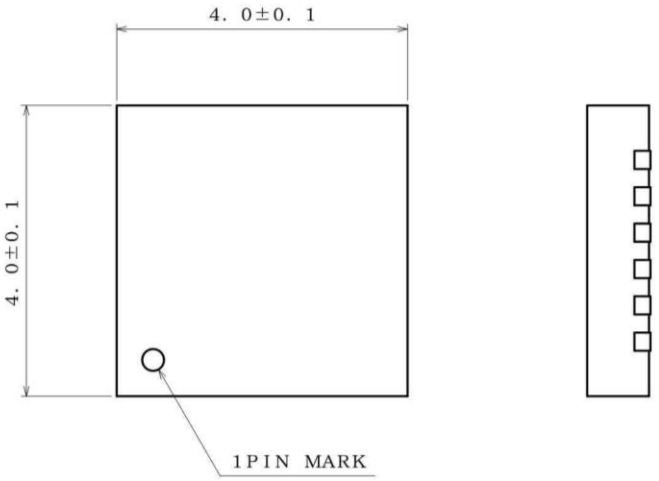
Marking Diagram

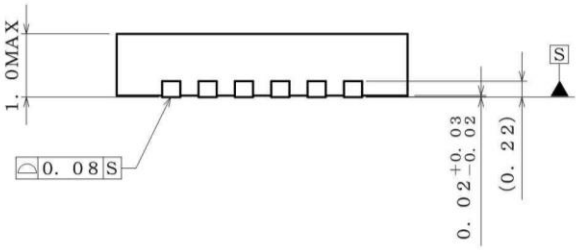


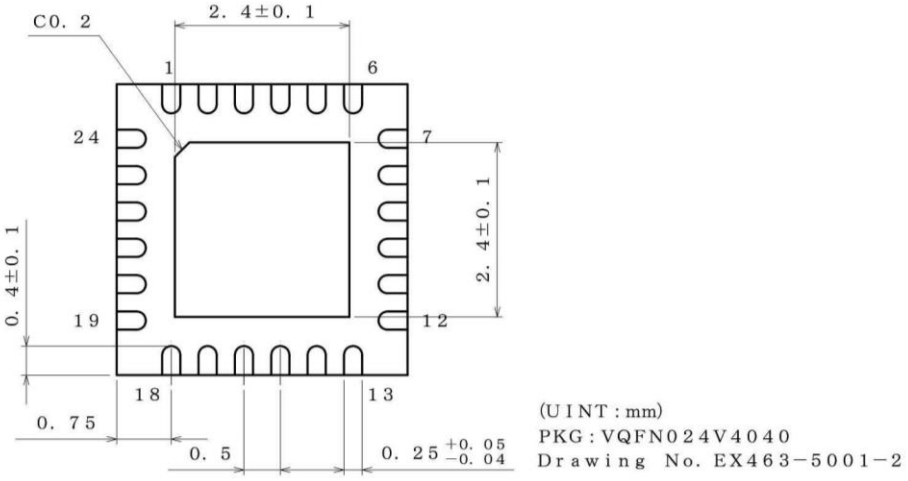
Part Number Marking	Package	Orderable Part Number
63001	VQFN024V4040	BD63001AMUV-E2

Physical Dimension, Tape and Reel Information

Package Name	VQFN024V4040

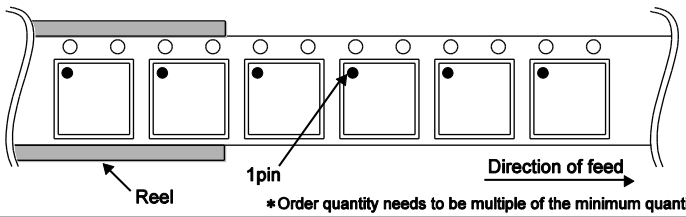






<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
23.Mar.2016	001	New Release
30.May.2016	002	P6 Notation change of Thermal resistance "Footprints and Traces" $74.2mm^2$ (Square) ⇒ 74.2mm x 74.2mm P18 Thermal Consideration Pd ⇒ maximum junction temperature

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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