DELKIN DEVICES®

Utility+

SATA III Industrial MLC 2.5” Solid State Drive

Engineering Specification

Document Number: 404-0002-00

Revision: G

Product Overview

- **Capacity**
  - 64GB up to 2TB
- **SATA Interface**
  - SATA Revision 3.2
  - SATA 1.5Gbps, 3Gbps, and 6Gbps interface
- **Flash Interface**
  - Flash type: MLC
- **Performance**
  - Read: up to 520 MB/s
  - Write: up to 500 MB/s
- **Power Consumption**[Note1]
  - Write: < 5,400mW
  - Read: < 3,200mW
  - Idle: < 450mW
- **TBW (Terabytes Written)** [Note2]
  - 1860 TBW for 2TB
- **MTBF**
  - More than 2,000,000 hours
- **Features**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - NCQ
  - SMART
  - Over-Provisioning
  - Firmware Update Capability
  - Temperature Sensor
- **Low Power Management**
  - DIPM/HIPM Mode
- **Temperature Range**
  - Operation: -40°C ~ 85°C
  - Storage: -40°C ~ 85°C
- **RoHS compliant**

Notes:

1. Please see "4.2 Power Consumption" for details.
2. Please see "TBW (Terabytes Written)" in Chapter 2" for details.

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1. INTRODUCTION

1.1. General Description

Delkin’s Utility+ Industrial MLC 2.5” Solid State Drive (SSD) delivers all the advantages of flash disk technology with the performance of the Serial ATA III interface and is fully compliant with the standard 2.5” form factor. Delkin’s SSD draws significantly less power compared to traditional hard drives and is also hot swappable. The drive is available in capacities from 32GB to 2TB and can reach speeds up to 520MB/s read as well as 500MB/s write (measured by CrystalDiskMark v3.0).

1.2. Product Block Diagram

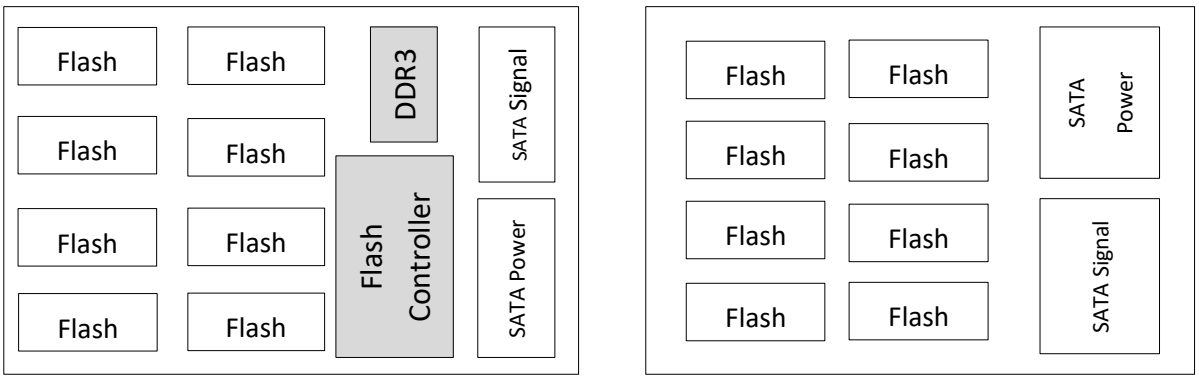

Figure 1-1 SSD Product Block Diagram

1.3. Flash Management

1.3.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, Delkin’s 2.5” SSD applies the BCH ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.3.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas are updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND flash by evenly distributing write and erase cycles across the media.

Delkin utilizes advanced Wear Leveling algorithms, which can efficiently distribute flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.3.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during usage of the flash are named “Later Bad Blocks”. Delkin implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves data reliability.

1.3.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform an erase action, which prevents unused data from occupying blocks.

1.3.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.3.6. Over-Provisioning

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible or usable by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.3.7. Firmware Upgrades

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware can be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved, as controlled by the user.

1.4. Low Power Management

1.4.1. DIPM/HIPM Mode

SATA interfaces contain two low power management states for power saving: Partial and Slumber modes. In Partial mode, the device must resume full operation within 10 microseconds, whereas in Slumber mode, the device has 10 milliseconds to become fully operational. SATA interfaces allow low power modes to be initiated by Host (HIPM, Host Initiated Power Management) or Device (DIPM, Device Initiated Power Management). As for HIPM, Partial or Slumber mode can be invoked directly by the software. For DIPM, the device will send requests to enter Partial or Slumber mode.

1.5. Power Loss Protection: Flushing Mechanism

Power Loss Protection is a mechanism to prevent data loss during unexpected power failures. DRAM is volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve SSD performance. However, one major concern of the DRAM is that data could be lost in the event of a power failure. Accordingly, the Delkin SATA controller applies the ***GuaranteedFlush*** technology, which requests the controller to transfer data to the cache. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, Delkin’s controller applies an algorithm to reduce the amount of data residing in the cache to provide better performance. This ***SmartCacheFlush*** technology allows incoming data to have only a brief “pit stop” in the cache and then move straight to the NAND flash. If the flash is jammed due to particular file sizes (such as random 4KB data), the cache will be treated as an “organizer”, consolidating incoming data into groups before written into the flash to improve write amplification.

In summary, with this advanced Flush Mechanism, Delkin’s controller provides the reliability and data protection required by today’s applications and hosts.

1.6. Advanced Device Security Features

1.6.1. Secure Erase

Secure Erase is a standard ATA command and will write "0xFF" to all cells, to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will erase its storage blocks and return to its factory default settings.

1.6.2. Write Protect

When a SSD contains too many bad blocks and data is continuously written in, then the SSD may no longer be usable. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

1.7. SSD Lifetime Management

1.7.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity) x (WLE)] / WAF

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle rating of NAND flash, per the manufacturer's specification.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WLE: Wear Leveling Efficiency (WLE) represents the ratio of the average amount of erases on all the blocks to the erases on any block at maximum.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller writes to the flash and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

1.7.2. Thermal Monitor

Thermal monitors are devices for measuring temperature, and can be found in SSDs in order to issue warnings when SSDs go beyond a certain temperature. The higher temperature the thermal monitor detects, the more power the SSD consumes, causing the SSD to age quickly. Hence, the processing speed of a SSD should be under control to prevent temperature from exceeding a certain range. Temperature can be monitored via SMART, as referenced in Section 6.3.

1.8. An Adaptive Approach to Performance Tuning

1.8.1. Throughput

Based on the available space of the disk, Delkin SSD controller will regulate the read/write speed and manage the throughput performance. When significant free space remains, the firmware will continuously perform read/write activity. At this stage, there is still no need to implement garbage collection to allocate and release memory, which will accelerate read/write processing to improve the performance. However, when free space is used up, the controller will slow down the read/write processing, and implement garbage collection to release memory blocks. Hence, read/write performance will become slower.

1.8.2. Predict & Fetch

Normally, when the host tries to read data from the SSD, the SSD will only perform one read action after receiving one command. However, Delkin’s controller applies ***Predict & Fetch*** to improve the read speed. When the host issues sequential read commands to the SSD, the SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait as long to receive data.

2. PRODUCT SPECIFICATIONS

• Capacity

- From 64GB up to 2TB

• Electrical/Physical Interface

- SATA Interface
  - Compliant with SATA Revision 3.2
  - Compatible with SATA 1.5Gbps, 3Gbps and 6Gbps interface
  - NCQ support up to queue depth = 32
  - Supports power management
  - Supports expanded register for SATA protocol 48 bit addressing mode

• ECC Scheme

- Capable of correcting up to 120 bits per 2K Bytes of data

• Supports SMART and TRIM commands

• Performance and Power Consumption

Capacity	Performance		Power Consumption	
	CrystalDiskMark		Read (mW)	Write (mW)
	Read (MB/s)	Write (MB/s)		
64GB	520	95	2000	2300
128GB	520	200	2060	2330
256GB	520	400	2150	3600
512GB	520	500	2235	4370
1TB	520	500	2520	4450
2TB	550	530	3200	5400

NOTE:

For more details on Power Consumption, please refer to Chapter 4.2.

- **Endurance - TBW (Terabytes Written)**

Capacity	TBW
64GB	64
128GB	120
256GB	214
512GB	480
1TB	930
2TB	1860

NOTES:

1. Many factors affect drive endurance / TBW, including flash configuration, SDR configuration, host platform, usage model, write amplification factor, etc. The figures above are estimates and are not guarantees.

- **Part Numbers**

Industrial MLC 2.5” SSD (-40 to 85°C Operating Temperature)

Capacity	Part Number
64GB	DE64APR6P-35000-2
128GB	DE1HAPR6P-35000-2
256GB	DE2HAPC6P-35000-2
512GB	DE5HAPW6P-35000-2
1TB	DE1TAPX6P-35000-2
2TB	DE2TAPX7R-35000-2

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational: -40°C to 85°C

- Humidity:
  - RH 95% under 55°C (operational)

3.1.2. Shock & Vibration

- Shock Specification
  - 1500G, 0.5ms duration, 3 axes

- Vibration Specification
  - 20Hz ~80Hz/1.52mm displacement, 80Hz~2000Hz / 20G Acceleration, 3 axes

3.1.3. Electrostatic Discharge (ESD)

- +/- 4KV

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device’s reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Delkin’s 2.5” SSD is more than 2,000,000 hours at 0°C.

3.3. Certification & Compliance

- RoHS
- SATA III (SATA Rev. 3.2)
- Up to ATA/ATAPI-8 (Including S.M.A.R.T)

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage

Parameter	Rating
Operating Voltage	5V ± 5% (Option)
Maximum Ripple	100mV, 0 ~ 30MHz

4.2. Power Consumption

Table 4-2 Power Consumption

Capacity	Read	Write	Partial	Slumber	Idle
64GB	2000	2300	200	200	200
128GB	2060	2330	260	260	360
256GB	2150	3600	260	255	365
512GB	2235	4370	265	265	375
1TB	2520	4450	285	280	400
2TB	3200	5400	280	260	400

Unit: mW

NOTES:

1. The average value of power consumption is achieved based on 100% conversion efficiency.
2. The measured power voltage is 5V.
3. Sequential R/W is measured while testing 4000MB sequential R/W 5 times by CrystalDiskMark. DEVSLP is measured while entering device sleep mode for 5 minutes.
4. Power Consumption may differ according to flash configuration, SDR configuration, and host platform.

5. INTERFACE

5.1. Pin Assignment and Descriptions

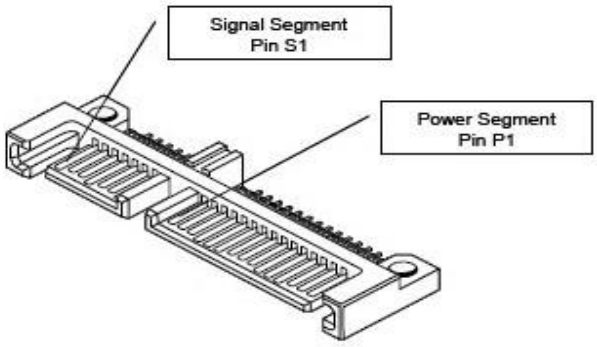

Table 5-1 Signal Segment Pin Assignment and Descriptions

PIN NUMBER	FUNCTION
S1	GND
S2	A+ (DIFFERENTIAL SIGNAL PAIR A)
S3	A- (DIFFERENTIAL SIGNAL PAIR A)
S4	GND
S5	B- (DIFFERENTIAL SIGNAL PAIR B)
S6	B+ (DIFFERENTIAL SIGNAL PAIR B)
S7	GND

Table 0-2 Power Segment Pin Assignment and Descriptions

PIN NUMBER	FUNCTION
P1	NOT USED (3.3V)
P2	NOT USED (3.3V)
P3	DEVSLP
P4	GND
P5	GND
P6	GND
P7	5V PRE-CHARGE
P8	5V
P9	5V
P10	GND
P11	RESERVED
P12	GND
P13	NOT USED (12V PRE-CHARGE)
P14	NOT USED (12V)
P15	NOT USED (12V)

6. SUPPORTED COMMANDS

6.1. ATA Command List

Table 6-1 ATA Command List

Op Code	Description	Op Code	Description
00h	NOP	97h	IDLE
06h	Data Set Management	98h	CHECK POWER MODE
10h-1Fh	Recalibrate	99h	SLEEP
20h	Read Sectors	B0h	SMART
21h	Read Sectors without Retry	B1h	DEVICE CONFIGURATION
24h	Read Sectors EXT	C4h	Read Multiple
25h	Read DMA EXT	C5h	Write Multiple
27h	Read Native Max Address EXT	C6h	Set Multiple Mode
29h	Read Multiple EXT	C8h	Read DMA
2Fh	Read Log EXT	C9h	Read DMA without Retry
30h	Write Sectors	CAh	Write DMA
31h	Write Sectors without Retry	CBh	Write DMA without Retry
34h	Write Sectors EXT	CEh	Write Multiple FUA EXT
35h	Write DMA EXT	E0h	Standby Immediate
37h	Set Native Max Address EXT	E1h	Idle Immediate
38h	CFA WRITE SECTORS WITHOUT ERASE	E2h	Standby
39h	Write Multiple EXT	E3h	Idle
3Dh	Write DMA FUA EXT	E4h	Read Buffer
3Fh	Write Long EXT	E5h	Check Power Mode
40h	Read Verify Sectors	E6h	Sleep
41h	Read Verify Sectors without Retry	E7h	Flush Cache
42h	Read Verify Sectors EXT	E8h	Write Buffer
45h	WRITE UNCORRECTABLE EXT	EAh	Flush Cache EXT
60h	Read FPDMA Queued	ECh	Identify Device
61h	Write FPDMA Queued	EFh	Set Features
70h-7Fh	Seek	F1h	Security Set Password
90h	Execute Device Diagnostic	F2h	Security Unlock
91h	Initialize Device Parameters	F3h	Security Erase Prepare
92h	Download Microcode	F4h	Security Erase Unit
93h	DOWNLOAD MICROCODE DMA	F5h	Security Freeze Lock
94h	STANDBY IMMEDIATE	F6h	Security Disable Password
95h	IDLE IMMEDIATE	F8h	Read Native Max Address
96h	STANDBY	F9h	Set Max Address

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-2 List of Device Identification

Word	F: Fixed V: Variable X: Both	Default Value	Description
0	F	0040h	General configuration bit-significant information
1	X	***1**	Obsolete – Number of logical cylinders
2	V	C837h	Specific configuration
3	X	0010h	Obsolete – Number of logical heads (16)
4-5	X	00000000h	Retired
6	X	003Fh	Obsolete – Number of logical sectors per logical track (63)
7-8	V	00000000h	Reserved for assignment by the Compact Flash Association
9	X	0000h	Retired
10-19	F	Varies	Serial number (20 ASCII characters)
20-21	X	0000h	Retired
22	X	0000h	Obsolete
23-26	F	Varies	Firmware revision (8 ASCII characters)
27-46	F	Varies	Model number
47	F	8010h	7:0- Maximum number of sectors transferred per interrupt on MULTIPLE commands
48	F	4000h	Trusted Computing feature set options(not support)
49	F	2F00h	Capabilities
50	F	4000h	Capabilities
51-52	X	000000000h	Obsolete
53	F	0007h	Words 88 and 70:64 valid
54	X	***1**	Obsolete – Number of logical cylinders
55	X	0010h	Obsolete – Number of logical heads (16)
56	X	003Fh	Obsolete – Number of logical sectors per track (63)
57-58	X	***2**	Obsolete – Current capacity in sectors
59	F	0110h	Number of sectors transferred per interrupt on MULTIPLE commands
60-61	F	***3**	Maximum number of sector (28bit LBA mode)
62	X	0000h	Obsolete
63	F	0407h	Multi-word DMA modes supported/selected
64	F	0003h	PIO modes supported
65	F	0078h	Minimum Multiword DMA transfer cycle time per word

Word	F: Fixed V: Variable X: Both	Default Value	Description
66	F	0078h	Manufacturer’s recommended Multiword DMA transfer cycle time
67	F	0078h	Minimum PIO transfer cycle time without flow control
68	F	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	F	0100h	Additional Supported (support download microcode DMA)
70	F	0000h	Reserved
71-74	F	0000000000000000h	Reserved for the IDENTIFY PACKET DEVICE command
75	F	001Fh	Queue depth
76	F	670eh	Serial SATA capabilities
77	F	0084h	Serial ATA Additional Capabilities
78	F	014Ch	Serial ATA features supported
79	V	0040h	Serial ATA features enabled
80	F	07F8h	Major Version Number
81	F	0000h	Minor Version Number
82	F	346bh	Command set supported
83	F	7d09h	Command set supported
84	F	6063h	Command set/feature supported extension
85	V	3469h	Command set/feature enabled
86	V	bc01h	Command set/feature enabled
87	V	6063h	Command set/feature default
88	V	003Fh	Ultra DMA Modes
89	F	0001h	Time required for security erase unit completion
90	F	001Eh	Time required for Enhanced security erase completion
91	V	0000h	Current advanced power management value
92	V	FFFEh	Master Password Revision Code
93	F	0000h	Hardware reset result. The contents of the bits (12:0) of this word can be changed only during the execution of hardware reset.
94	V	0000h	Vendor’s recommended and actual acoustic management value
95	F	0000h	Stream Minimum Request Size
96	V	0000h	Streaming Transfer Time – DMA
97	V	0000h	Streaming Access Latency – DMA and PIO
98-99	F	0000h	Streaming Performance Granularity
100-103	V	***4**	Maximum user LBA for 48 bit Address feature set

Word	F: Fixed V: Variable X: Both	Default Value	Description
104	V	0000h	Streaming Transfer Time – PIO
105	F	0008h	Maximum number of 512-byte blocks per DATA SET MANAGEMENT command
106	F	4000h	Physical sector size/Logical sector size
107	F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108-111	F	0000000000000000h	Unique ID
112-115	F	0000000000000000h	Reserved
116	V	0000h	Reserved
117-118	F	00000000h	Words per logical Sector
119	F	4014h	Supported settings
120	F	4014h	Command set/Feature Enabled/Supported
121-126	F	0h	Reserved
127	F	0h	Removable Media Status Notification feature set support
128	V	0021h	Security status
129-140	X	0h	Vendor specific
141	X	0001h	Vendor specific
142-159	X	0h	Vendor specific
160	F	0h	Compact Flash Association (CFA) power mode 1
161-167	X	0h	Reserved for assignment by the CFA
168	F	3h 2.5” 4h 1.8” 5h Less than 1.8”	Device Nominal Form Factor
169	F	0001h	DATA SET MANAGEMENT command is supported
170-173	F	0h	Additional Product Identifier
174-175		0h	Reserve
176-205	V	0h	Current media serial number
206	F	0h	SCT Command Transport
207-208	F	0h	Reserved
209	F	4000h	Alignment of logical blocks within a physical block
210-211	V	0000h	Write-Read-Verify Sector Count Mode 3 (not supported)
212-213	F	0000h	Write-Read-Verify Sector Count Mode 2 (not supported)
214-216		0000h	NV Cache relate (not supported)
217	F	0001h	Non-rotating media device
218	F	0h	Reserved

Word	F: Fixed V: Variable X: Both	Default Value	Description
219	F	0h	NV Cache relate (not supported)
220	V	0h	Write read verify feature set current mode
221		0h	Reserved
222	F	107Fh	Transport major version number
223	F	0h	Transport minor version number
224-229		0h	reserved
230-233		0h	Extend number of user addressable sectors
234		0001h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235		0080h	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	F	0h	Reserved
255	X	XXA5h XX is variable	Integrity word (Checksum and Signature)

Table 6-3 List of Device Identification for Each Capacity

Capacity (GB)	*1 (Word 1/Word 54)	*2 (Word 57 - 58)	*3 (Word 60 - 61)	*4 (Word 100 - 103)
64	3FFFh	FBFC10h	7740AB0h	7740AB0h
128	3FFFh	FBFC10h	EE7C2B0h	EE7C2B0h
256	3FFFh	FBFC10h	FFFFFFFh	1DCF32B0h
512	3FFFh	FBFC10h	0FFFFFFF	3B9E12B0
1024	3FFFh	FBFC10h	FFFFFFFh	6FC81AB0h

6.3. SMART

6.3.1. Command Description

6.3.1.1. I/O Registers

Communication to or from device through Data register and 7 Command Block registers (28bits command format), include Feature register, Error register, Sector Count register, Sector Number register, Cylinder Low register, Cylinder High register, Drive Head register, Status register, Command register.

Table 6-4 Command Block Registers Addressing

Offset address	Read	Write	Value Type
0x00	Data	Data	WORD
0x01	Error	Feature	BYTE
0x02	Sector Count	Sector Count	BYTE
0x03	Sector Number (LBA low current)	Sector Number (LBA low current)	BYTE
0x04	Cylinder Low (LBA Mid current)	Cylinder Low (LBA Mid current)	BYTE
0x05	Cylinder High (LBA High current)	Cylinder High (LBA High current)	BYTE
0x06	Drive Head	Drive Head	BYTE
0x07	Status	Command	BYTE

Direction: Input means from Host to Device, Output means from Device to Host

6.3.1.2. SMART Command Table

Vender Command	Feature	Sector Count	Sector Number	Cylinder Low	Cylinder High	Drive Head	Command
Smart Read Attribute	0xD0	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Read Attribute Thresholds	0xD1	0x01	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Attribute Auto Save	0xD2	0xF1	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Attribute Auto Save	0xD2	0x00	XX	0x4F	0xC2	0xA0	0xB0
SMART SAVE ATTRIBUTE VALUES	0xD3	XX	XX	0x4F	0xC2	0xA0	0xB0
SMART EXECUTE OFF-LINE IMMEDIATE	0xD4	XX	XX	0x4F	0xC2	0xA0	0xB0
SMART READ LOG	0xD5	Depends on Log Address	XX	0x4F	0xC2	0xA0	0xB0
SMART WRITE LOG	0xD6	Depends on Log Address	XX	0x4F	0xC2	0xA0	0xB0
Smart Enable Operations	0xD8	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Disable Operation	0xD9	XX	XX	0x4F	0xC2	0xA0	0xB0
Smart Return Status	0xDA	XX	XX	0x4F	0xC2	0xA0	0xB0
SMART ENABLE AUTOMATIC OFF-LINE	0xDB	XX	XX	0x4F	0xC2	0xA0	0xB0
SMART DISABLE AUTOMATIC OFF-LINE	0xDB	XX	XX	0x4F	0xC2	0xA0	0xB0

6.3.1.3. SMART Read Attribute

[Protocol] PIO Data In

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD0							
Sector Count	0x01							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

This command will return 1 sector of SMART Read Attribute information.

Attribute Table

Attribute ID	Description
01h	Number of accumulation of uncorrectable error. (Range 0~255)
09h	Power on hours count. (Range 0-4294967295)
0Ch	Drive power cycle count (Number of accumulation of power on/off cycles)
A8h	Sata PHY error count (only record from power on, when power off this value will clear to zero) this value include all PHY error count, ex data FIS CRC code error, disparity error ,command FIS crc…..)
AAh	Bad block count.
ADh	Erase count
C0h	Number of unexpected power loss count
C2h	Temperature
DAh	Number of accumulation CRC error (read/write data FIS CRC error)
E7h	SSD life remaining
F1h	Lifetime write from host

Smart attribute actual data

0	1	2	3	4	5	6	7	8	9	10	11	
ID	Flag	flag	value	worse	DATA							threshold
01h	0Bh	00h	64h	64h	0	0	ECC error	0	0	0	0	32h
09h	12h	00h	64h	64h	power on hour		0	0	0	0	0	00h
0Ch	12h	00h	64h	64h	power on/off cycles				0	0	0	00h
A8h	12h	00h	64h	64h	SATA PHY error count				0	0	0	00h
AAh	03h	00h	note 1	note 1	early bad block NO		0	0	later bad block NO		0	0ah
ADh	12h	00h	64h	64h	max erase count (MAX 65535)		average erase count (MAX 65535)		0	0	0	00h
C0h	12h	00h	64h	64h	number of accidental power loss count				0	0	0	00h
C2h	23h	00h	100-Current Temp	100-Highest value	Current Temp		Lowest Temp		Highest Temp		0	1Eh
DAh	0Bh	00h	64h	64h	number of CRC Error				0	0	0	32h
E7h	13h	00h	64h	64h	*Note	0	0	0	0	0	0	00h
F1h	32h	00h	0h	0h	Host write 1GB count				0	0	0	0

*Note: 100 - (average erase count /MAX erase count (slc 20,000, mlc 3,000) *100

Note1: Note 1 = (100*(A-B))/A, Max = 100, Min = 1

A: Maximum Acceptable Number of Bad Block (Plane)

B: Current Number of Maximum Bad Block (Plane)

6.3.1.4. SMART Read Attribute Thresholds

[Protocol] PIO Data In

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD1							
Sector Count	0x01							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	**0**	**1**	**0**	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

This command will return 1 sector of SMART Read Attribute Thresholds information.

6.3.1.5. SMART Enable Attribute Auto Save

[Protocol] PIO Non-data

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD2							
Sector Count	0XF1							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART ENABLE ATTRIBUTE AUTOSAVE command enables the attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attributes to non-volatile memory or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature, either enabled or disabled, shall be preserved by the device during all power and reset events. The COUNT field cleared to zero shall cause the device to disable the attribute autosave

feature. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation (e.g., during a power-on or power-off sequence or during an error recovery sequence).

The COUNT field set to F1h shall cause the device to enable the attribute autosave feature. If the COUNT field is not set to 00h or F1h, then the actions taken by a device are vendor specific. If the device receives a command while processing the autosave routine the device shall begin processing the command within 2 s.

6.3.1.6. SMART Disable Attribute Auto Save

[Protocol] PIO Non-data

[Input]

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Feature	0xD2							
Sector Count	0x00							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART DISABLE ATTRIBUTE AUTOSAVE command disables the attribute autosave feature of the device. This command may either allow the device, after some vendor specified event, to save the device updated attributes to non-volatile memory or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature, either enabled or disabled, shall be preserved by the device during all power and reset events.

The COUNT field cleared to zero shall cause the device to disable the attribute autosave feature. Disabling this feature does not preclude the device from saving SMART data to non-volatile memory during some other normal operation (e.g., during a power-on or power-off sequence or during an error recovery sequence).

The COUNT field set to F1h shall cause the device to enable the attribute autosave feature. If the COUNT field is not set to 00h or F1h, then the actions taken by a device are vendor specific.

If the device receives a command while processing the autosave routine the device shall begin processing the command within 2 s.

6.3.1.7. SMART Execute Off-Line Immediate

[Protocol] PIO Non-data

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD4							
Sector Count	0x00							
Sector Number (LBA LOW current)	subcommand							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	**0**	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART EXECUTE OFF-LINE IMMEDIATE command causes the device to initiate the optional set of activities that collect SMART data in an off-line mode and then preserve this data across power and reset events, or process a vendor specific self-diagnostic test routine in either captive or off-line mode.

Value	Description of subcommand to be processed
00h	Execute SMART off-line routine in off-line mode
01h	Execute SMART Short self-test routine in off-line mode
02h	Execute SMART Extended self-test routine in off-line mode
03h (not supported)	Execute SMART Conveyance self-test routine in off-line mode
04h	Execute SMART Selective self-test routine in off-line mode
05h-3Fh	Reserved
40h-7Eh	Vendor specific
7Fh	Abort off-line mode self-test routine
80h	Reserved
81h	Execute SMART Short self-test routine in captive mode
82h	Execute SMART Extended self-test routine in captive mode
83h (not supported)	Execute SMART Conveyance self-test routine in captive mode
84h	Execute SMART Selective self-test routine in captive mode
85h-8Fh	Reserved
90h-FFh	Vendor specific

6.3.1.8. SMART Read Log

[Protocol] PO Data-In

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD5							
Sector Count	Depend on Log Address							
Sector Number (LBA LOW current)	Log Address							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART READ LOG command returns the specified log to the host.

6.3.1.9. SMART Write Log

[Protocol] PO Data-Out

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD6							
Sector Count	Depend on Log Address							
Sector Number (LBA LOW current)	Log Address							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	**0**	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART WRITE LOG command returns the specified log to the host.

6.3.1.10. SMART Enable Operations

[Protocol] PIO Non-data

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD8							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	**0**	**0**	**0**	**0**	**0**
Command	0xB0							

[Normal Output]

Register	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART ENABLE OPERATIONS command enables access to all available SMART capabilities within the device. The state of SMART, either enabled or disabled, shall be preserved by the device during all power and reset events. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

6.3.1.11. SMART Disable Operations

[Protocol] PIO Non-data

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xD9							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART DISABLE OPERATIONS command shall disable all SMART operations. After completion of this command without error the device shall report command aborted for all other SMART commands (e.g., SMART DISABLE OPERATIONS commands), except for the SMART ENABLE OPERATIONS command and the SCT Command Transport commands, which shall be processed as defined. The state of SMART (i.e., enabled or disabled) shall be preserved by the device during all power-on reset events.

6.3.1.12. SMART Return Status

[Protocol] PIO Non-data

[Input]

Register	7	6	5	4	3	2	1	0
Feature	0xDA							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	0x4F							
Cylinder High (LBA HIGH current)	0xC2							
Drive Head	1	0	1	0	0	0	0	0
Command	0xB0							

[Normal Output]

Register	7	6	5	4	3	2	1	0
Error	N/A							
Sector Count	N/A							
Sector Number (LBA LOW current)	N/A							
Cylinder Low (LBA MID current)	N/A							
Cylinder High (LBA HIGH current)	N/A							
Drive Head	0xE0							
Status	0x50							

[Description]

The SMART RETURN STATUS command causes the device to communicate the reliability status of the device to the host.

Status Return:

If Current Reserved Block > 3, return 0x4F, 0xC2

If Current Reserved Block <= 3, detected a threshold exceeded condition, return 0xF4, 0x2C

7. PHYSICAL DIMENSIONS

Dimension: 100.00mm (L) x 69.85mm (W) x 7mm (H)