

# Spartan-6 FPGA Connectivity Kit

## *Getting Started Guide*

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## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/8/2009	1.0	Initial Xilinx release.
12/18/2009	1.1	Changed <a href="#">Figure 1</a> . Added <a href="#">step 3, page 13</a> . Added introduction to the Hardware Setup instructions under <a href="#">Figure 2</a> . Under <a href="#">step 5, page 14</a> , changed the jumper to J27 in <a href="#">step b</a> and indicated that ON is down in <a href="#">step c</a> . Replaced photograph in <a href="#">Figure 3</a> , <a href="#">Figure 4</a> , and <a href="#">Figure 63</a> . Added introductory paragraphs prior to <a href="#">step 2, page 16</a> and <a href="#">step 5, page 19</a> . Updated <a href="#">Figure 15</a> . Revised the MAC address example in <a href="#">step d, page 22</a> . Added introductory paragraph to <a href="#">Evaluating the Spartan-6 FPGA Connectivity Targeted Reference Design</a> . Changed the Data Transmission and Packet Size options in <a href="#">step 1, page 37</a> . Added <a href="#">step 4, page 43</a> . Under <a href="#">step 5, page 43</a> , changed <a href="#">step a</a> and added <a href="#">step c</a> and <a href="#">step d</a> . Changed the directory path in <a href="#">step b, page 44</a> . Removed IBERT example designs bullet from <a href="#">Getting Started with the Spartan-6 FPGA IBERT Reference Design</a> . Appended a sentence to the introductory paragraph of <a href="#">IBERT Hardware Demonstration Setup Instructions</a> . Added <a href="#">Reference Design Files</a> .
06/14/2010	1.2	Removed references to specific release numbers for the ISE Design Suite, where applicable. Removed update DVD from <a href="#">Connectivity Kit Contents</a> . Updated the DDR3 link speed in <a href="#">Figure 1</a> . Replaced the “Installing the Tools” section with two new paragraphs under <a href="#">Installation and Licensing of ISE Design Suite</a> . In <a href="#">step 7, page 42</a> , removed the ISE Design Suite release number from the path. Changed the command in <a href="#">step 4c on page 43</a> . Removed “double-click” from the Windows based script in <a href="#">step 7d on page 44</a> . Added the <a href="#">Next Steps</a> section.
08/10/2010	1.3	In <a href="#">step 4c on page 43</a> , <a href="#">Table 1</a> , and <a href="#">Figure 54</a> , changed <code>mig_v3_4</code> to <code>mig_v3_5</code> . In <a href="#">Table 1</a> and <a href="#">Figure 56</a> , changed <code>gig_eth_pcs_pma_v10_4</code> to <code>gig_eth_pcs_pma_v10_5</code> .
10/05/2010	1.4	Added information for AXI protocol.

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Date	Version	Revision
01/18/2012	2.0	<p>Added reference to the Windows XP operating system on <a href="#">page 13</a>. Revised procedure to support both Linux and Windows XP by adding the heading <a href="#">Testing with Linux Operating System, page 15</a>, updating <a href="#">Figure 6, page 17</a>, updating <a href="#">Figure 8, page 18</a>, and adding the section <a href="#">Testing with the Windows XP Operating System, page 23</a> through <a href="#">page 35</a>. Revised procedure to support both Linux and Windows XP by adding the heading <a href="#">On the Linux Operating System, page 36</a> and adding the section <a href="#">On the Windows Operating System, page 37</a>. Added note on <a href="#">page 41</a>. Revised procedure to support both Linux and Windows XP by adding the heading <a href="#">Linux Operating System, page 45</a> and adding the section <a href="#">Windows Operating System, page 46</a>. Updated <a href="#">Software Device Driver</a> directory names in <a href="#">Table 1, page 47</a>. Updated <a href="#">Figure 56</a> and <a href="#">Figure 57</a> on <a href="#">page 51</a>.</p>
06/14/2013	2.0.1	<p>Updated the Northwest Logic link in <a href="#">Reusing the DMA IP from Northwest Logic, page 52</a>.</p>



# Table of Contents

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Revision History .....	2
<b>Preface: About This Guide</b>	
Additional Resources .....	7
Additional Support .....	7
<b>Spartan-6 FPGA Connectivity Kit</b>	
Introduction .....	9
Connectivity Kit Contents .....	9
What is Inside the Box .....	9
What is Available Online .....	10
Getting Started with the Connectivity Targeted Reference Design Demo .....	11
Board and Connectivity Targeted Reference Design Features .....	11
Connectivity Targeted Reference Design Hardware Demonstration Setup .....	13
Testing with Linux Operating System .....	15
Testing with the Windows XP Operating System .....	23
Configuration .....	32
Evaluating the Spartan-6 FPGA Connectivity Targeted Reference Design .....	36
On the Linux Operating System .....	36
On the Windows Operating System .....	37
Installation and Licensing of ISE Design Suite .....	40
Downloading and Installing Tool and IP Licenses .....	40
The Connectivity Design is Ready for Modification .....	42
Modifying the Spartan-6 FPGA Connectivity Targeted Reference Design .....	43
Hardware Modifications .....	43
Test Setup .....	45
Software Modifications .....	45
Linux Operating System .....	45
Windows Operating System .....	46
Next Steps .....	46
Connectivity TRD Modules .....	46
PCI Express .....	48
Packet DMA (with AXI4 Interface Wrapper) .....	49
Multiport Virtual FIFO and Memory Controller Block .....	50
Ethernet .....	50
Software Device Driver and Software Application/GUI Files and Scripts .....	51
Simulating the Connectivity TRD .....	51
Reusing the DMA IP from Northwest Logic .....	52
Modifications to the Connectivity TRD .....	52
Getting Started with the Spartan-6 FPGA IBERT Reference Design .....	53
IBERT Hardware Demonstration Setup Instructions .....	54
Reference Design Files .....	62
Installation is Complete .....	62
Warranty .....	63



# About This Guide

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This Getting Started Guide describes the contents of the Spartan®-6 FPGA Connectivity Kit and provides instructions on how to start developing connectivity systems using GTP transceivers and LogiCORE™ IP in Spartan-6 FPGAs.

## Additional Resources

To find additional documentation, see the Xilinx website at:

<http://www.xilinx.com/support/documentation/index.htm>.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

Use this site for technical support regarding the installation and use of the product license file. Resources include:

- WebCase for contacting Technical Support via the Internet. Phone support information is also available.
- Answer Browser for quickly scanning titles of Answers Database categories.
- Forums for discussing topics of interest in user communities.
- Training for selecting instructor-led classes and recorded e-learning options.

## Additional Support

For questions regarding products within your online Product Entitlement Account, send an email message to your regional Customer Service Representative:

- Canada, USA, and South America: [isscs\\_cases@xilinx.com](mailto:isscs_cases@xilinx.com)
- Europe, Middle East, and Africa: [eucases@xilinx.com](mailto:eucases@xilinx.com)
- Asia Pacific including Japan: [apaccase@xilinx.com](mailto:apaccase@xilinx.com)





# Spartan-6 FPGA Connectivity Kit

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## Introduction

The Spartan®-6 FPGA Connectivity Kit helps designers quickly and efficiently develop connectivity systems. This complete, easy-to-use connectivity development and demonstration environment uses the Spartan-6 family for designing with very common standards based protocols, such as the PCI Express® and Ethernet protocols. This kit implements low-cost protocol bridging, provides higher efficiency alternative to LVDS communication, and so forth for use in multiple market segments.

**Note:** The screen captures in this document are conceptual representatives of their subjects and provide general information only. For the latest information, see the Xilinx® ISE® Design Suite.

## Connectivity Kit Contents

This section describes the kit deliverables provided in the box and indicates what can be found on the Xilinx website.

### What is Inside the Box

- Spartan-6 FPGA XC6SLX45T-3 based SP605 Evaluation Board along with:
  - Universal 12V power supply
  - Two USB A/Mini-B cables (used for download and debug)
  - One Ethernet Cat5 cable
  - One DVI-to-VGA adapter
  - Four SMA cables
  - One CompactFlash card (512 MB)
- Xilinx ISE Design Suite DVD, including:
  - ISE Foundation™ software with ISE Simulator
  - PlanAhead™ Design and Analysis Tool
  - Embedded Development Kit (EDK)
  - Xilinx Platform Studio (XPS)
  - Software Development Kit (SDK)
  - ChipScope™ Pro Tool
- One USB stick containing reference designs, documentation, and demonstrations
- Operating System: Fedora 10 LiveCD

- A single seat of production netlist licenses for the Northwest Logic x1 PCIe Packet DMA IP Core for Spartan-6 LXT FPGAs (node-locked license)
- Spartan-6 FPGA Connectivity Kit documentation:
  - Welcome letter
  - Hardware Setup Guide
  - This Getting Started Guide

## What is Available Online

Refer to the Xilinx website for this information:

- License for ISE Design Suite: Embedded Edition
  - <http://www.xilinx.com/getproduct>
  - <http://www.xilinx.com/tools/faq.htm>
- License for Northwest Logic's DMA IP core for Spartan-6 FPGAs
  - License delivered by Xilinx: <http://www.xilinx.com/getproduct>
  - License agreement: Northwest Logic's IP license agreement
- Development Kit home page with documentation and reference designs:
  - <http://www.xilinx.com/s6connkit>
  - This home page includes information on:
    - USB stick contents (the current version of the data on the USB stick is available here)
    - Schematics, Gerber, and board bill of materials (BOM)
    - Additional detailed documentation
- Technical Support
  - <http://www.xilinx.com/support>

## Getting Started with the Connectivity Targeted Reference Design Demo

The Spartan-6 FPGA Connectivity Kit comes with a pre-built demonstration of the connectivity targeted reference design (TRD) available on the SPI x4 flash. The demo can be run before any additional tools are installed for an overview of the features of the SP605 Evaluation Board using a connectivity targeted reference design in the Spartan-6 FPGA LX45T.

### Board and Connectivity Targeted Reference Design Features

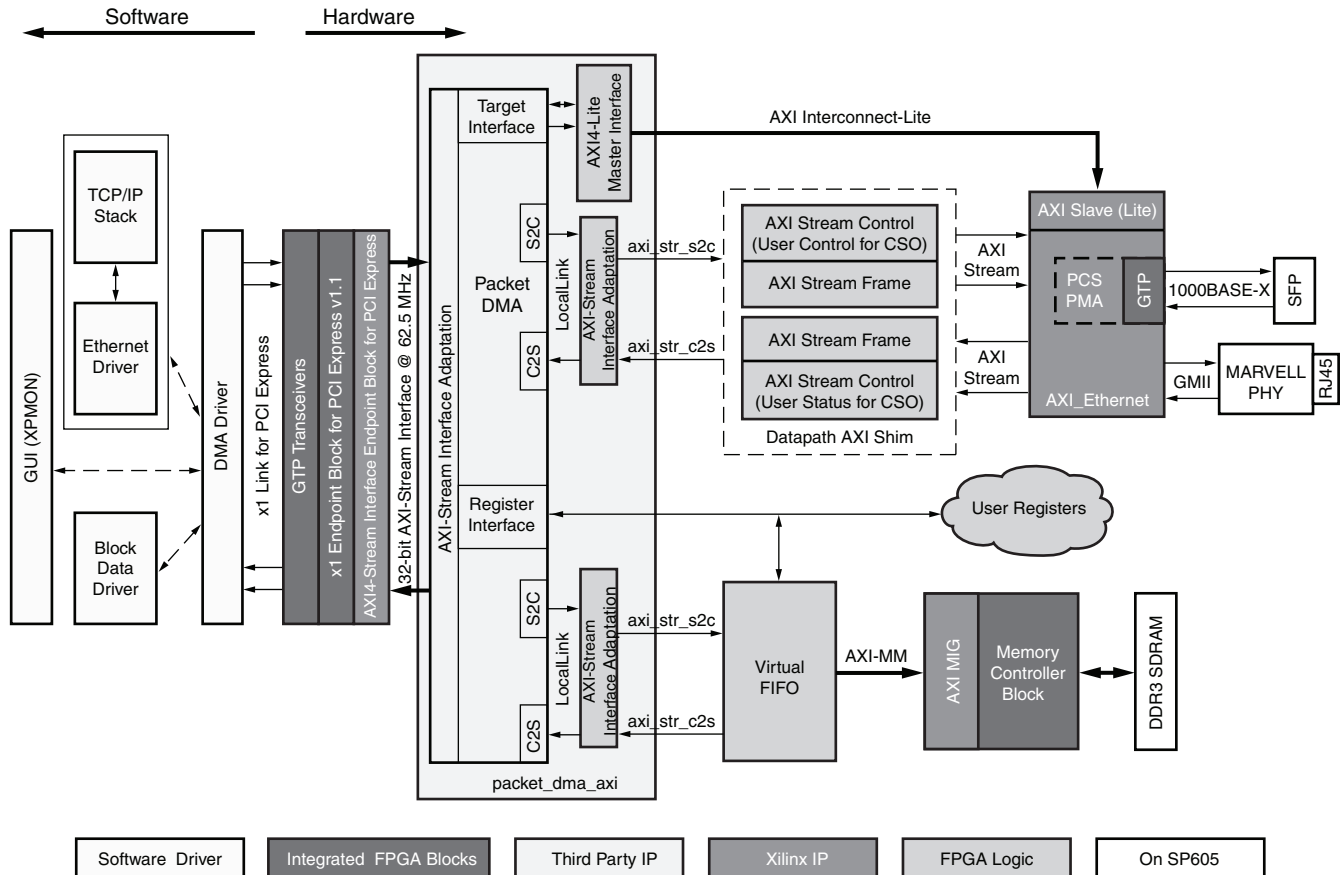
The Spartan-6 FPGA connectivity reference design (see [Figure 1](#)) demonstrates the main integrated components in a Spartan-6 FPGA—the endpoint block for PCI Express, the GTP transceivers, and the memory controller block working together in an application with additional third party and in-house IP cores.

The connectivity targeted reference design is delivered in two versions— one using AXI4 protocol IP cores, and the other using IP cores with legacy interfaces (such as LocalLink).

The AXI4 protocol version of the design uses IP cores all with AXI4 interfaces, namely, LogiCORE™ IP Spartan-6 FPGA Integrated Endpoint Block for PCI Express with AXI4-Stream user interface, Northwest Logic Packet DMA with AXI4 interface, AXI\_Ethernet IP core, and Memory Interface Generator with AXI4 user interface.

The version of the design without AXI4 protocol uses LogiCORE IP Spartan-6 FPGA Integrated Endpoint Block for PCI Express with transaction layer (TRN) user interface, Northwest Logic Packet DMA, XPS-LL-TEMAC IP core (using Tri-mode Ethernet MAC IP) and Memory Interface Generator IP for Spartan-6 Memory Controller Block.

**Note:** This document refers to the AXI4 protocol version of the TRD. Differences for versions without AXI4 protocol are pointed out, as required.



UG665\_01\_092810

Figure 1: Block Diagram of the Spartan-6 FPGA Connectivity Reference Design

The Spartan-6 FPGA connectivity targeted reference design features these components:

- 1-lane LogiCORE IP Spartan-6 FPGA Integrated Endpoint Block for PCI Express
- A performance monitor tracks the PCIe® data bandwidth through the transaction layer packet (TLP) utilization.
- Packet DMA for PCI Express from Northwest Logic, a multichannel DMA that:
  - Supports full-duplex operation with independent receive (card to system: C2S channel) and transmit (system to card: S2C) paths
  - Provides a packetized interface on the backend similar to LocalLink
  - Monitors data transfers in the receive and transmit directions
  - Provides a control plane interface to access user-defined registers

An adaptation layer is built around the Packet DMA to make it AXI4 interface compliant. The LocalLink based user streaming interface is now the AXI4-Stream interface and the target interface for control plane is AXI4-Lite Master.

- Multi-port Virtual FIFO

A highly efficient layer using the Spartan-6 FPGA memory controller block and an external DDR3 memory device.

- AXI\_Ethernet (using the Tri-Mode Ethernet MAC) IP core along with an AXI4-Lite slave interface.

The Ethernet application is demonstrated in two modes:

- GMII mode using an external PHY on-board.
- 1000BASE-X mode using the GTP transceivers in the Spartan-6 FPGA through an additional 1000BASE-X PCS-PMA LogiCORE IP enabled through a parameter option in the AXI\_Ethernet IP core.
- In the non-AXI4 protocol version, this IP is connected externally and is not a part of the XPS-LL-TEMAC IP core.

In the AXI4 protocol version of the TRD, AXI4-Lite is the control plane interface for register programming. In the version without AXI4 protocol, PLBv46 is the control plane interface for register programming.

## Connectivity Targeted Reference Design Hardware Demonstration Setup

This section describes how to set up the hardware for the connectivity targeted reference design demonstration.

1. This demonstration outlines a bridging function between PCIe and Gigabit Ethernet protocols. It also provides accesses to an onboard DDR3 memory device.

Here is a list of the equipment needed to run the hardware demonstration:

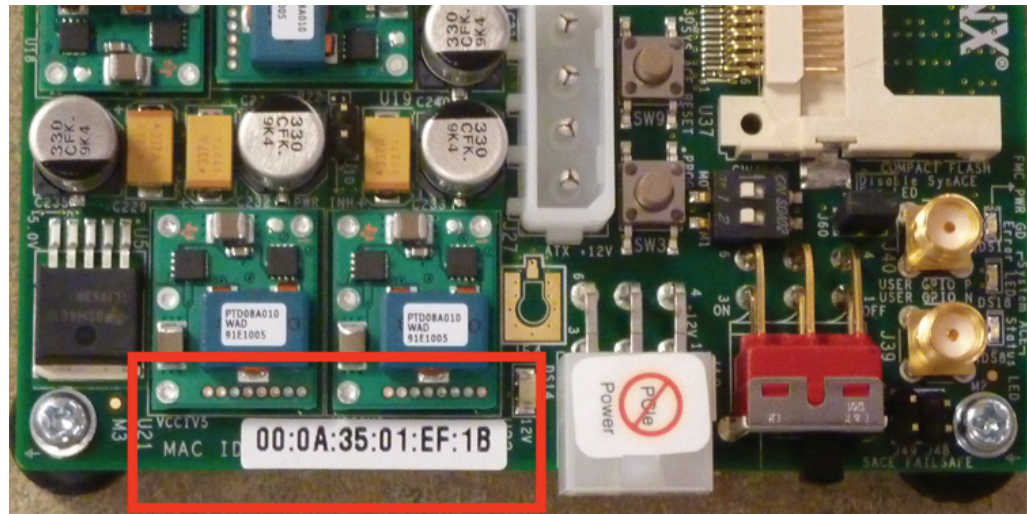
- Spartan-6 FPGA Connectivity Kit
- PC system with a x1 PCIe slot on the motherboard, CD ROM drive, and a USB port
- Monitor, keyboard, and mouse
- Live Ethernet connection (preferably Gigabit Ethernet)
- Operating System: Linux-based Fedora 10 LiveCD or Windows XP with Service Pack 3

2. Run the alternate demonstration.

If there is no access to any of the elements in [step 1](#), refer to [Getting Started with the Spartan-6 FPGA IBERT Reference Design, page 53](#) to alternately bring up the SP605 board included in the Spartan-6 FPGA Connectivity Kit. Otherwise, continue with the PCIe to Gigabit Ethernet protocol demonstration in [step 3](#).

3. If the instructions in the Spartan-6 FPGA Connectivity Kit Hardware Setup Guide have already been completed to bring up the Spartan-6 FPGA Connectivity Kit, proceed to [Evaluating the Spartan-6 FPGA Connectivity Targeted Reference Design, page 36](#); otherwise, continue to [step 4](#).

4. Fill in the MAC address for the demonstration here:  
The MAC address, available on the SP605 board, is \_\_\_\_:\_\_\_\_:\_\_\_\_:\_\_\_\_:\_\_\_\_:\_\_\_\_:  
(see [Figure 2](#)).

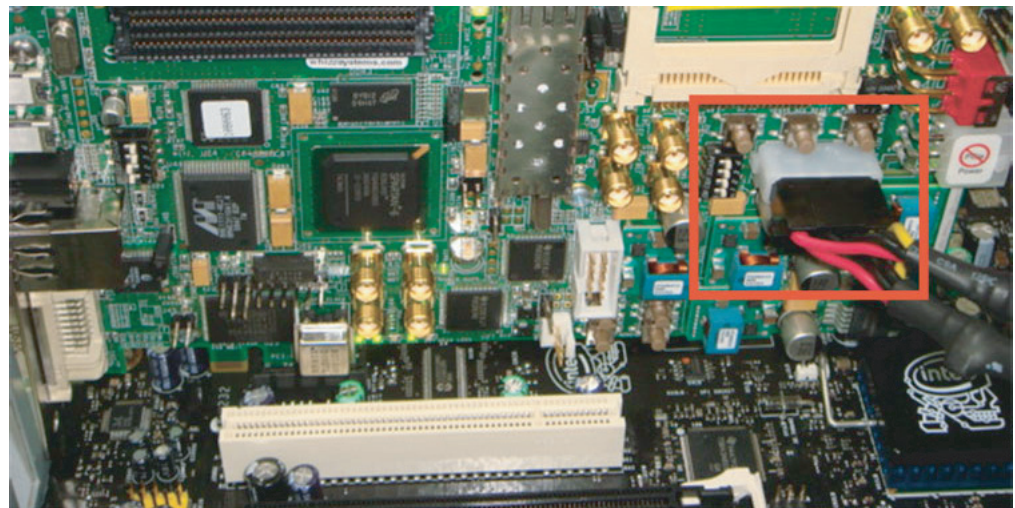


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*Figure 2:* **MAC Address of the SP605 Board**

The next two steps configure the SP605 board to utilize the Spartan-6 FPGA Connectivity Targeted Reference Design with a Network Interface Controller function enabled.

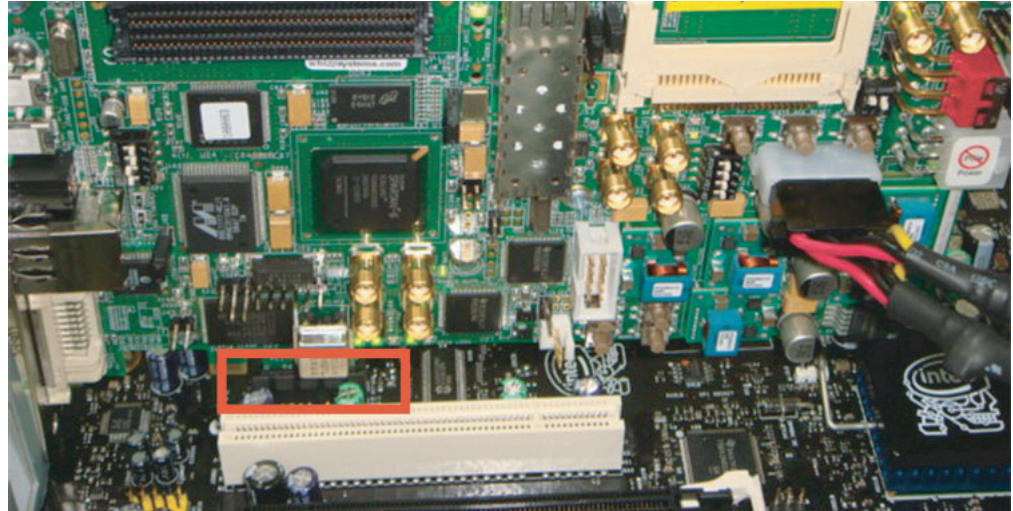
5. Hardware Setup I – Connect the power connector:
  - a. Turn the PC system off.
  - b. Connect the PC system's 12V ATX power supply's available 4-pin power connector (similar to the one attached to a CD ROM) to the board (J27). See [Figure 3](#).
  - c. The power switch SW2 should be switched to the ON (down) position.



UG665\_03\_121509

*Figure 3:* **12V ATX Power Supply Connector**

6. Hardware Setup II – Insert the SP605 board into an empty PCI Express slot:
  - a. Identify the slot on the motherboard of the PC system.
  - b. Insert the SP605 board into the PCI Express slot through the PCIe x1 edge connector (see [Figure 4](#)).



UG665\_04\_121509

**Figure 4: Identify and Insert the SP605 Board in the Slot for PCI Express**

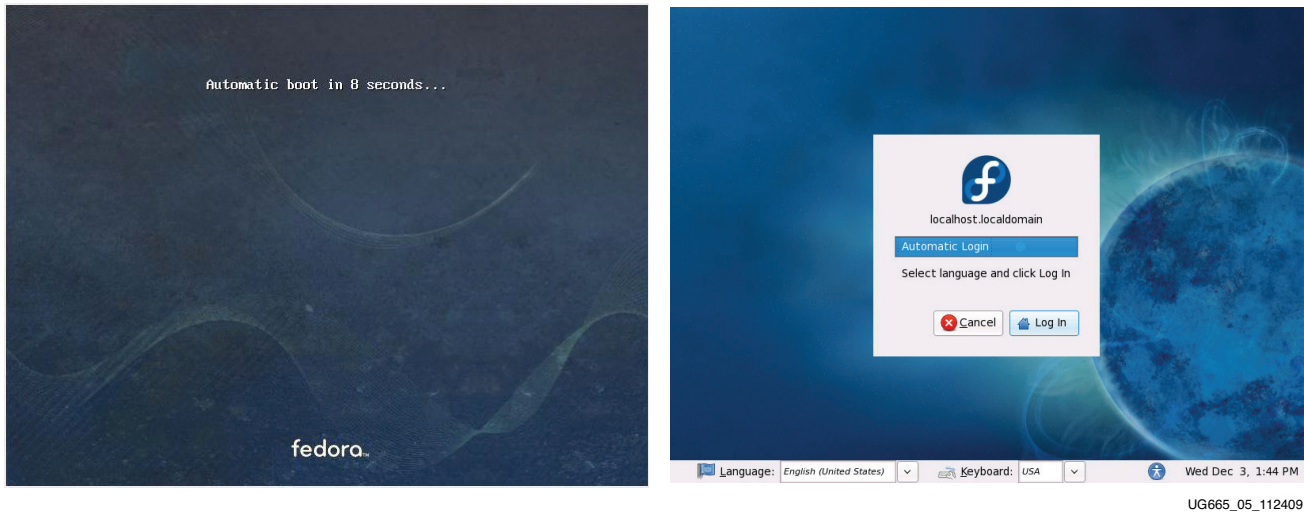
- c. Connect an Ethernet LAN cable in the RJ-45 slot. Connect the other end to an Ethernet wall socket. Disconnect or disable any existing Ethernet connections on the PC system.
- d. For this demo, the FPGA is programmed by a PCIe to Gigabit Ethernet design preloaded on the SPI x4 flash at power on.

## Testing with Linux Operating System

1. Configure the desktop PC to boot from the CD ROM:
  - a. Power the PC system on, and watch the initial BIOS screen for a prompt that indicates which key to use for either:
    - A boot menu or
    - The BIOS setup utility
  - b. If such a prompt is not visible, refer to the manufacturer's documentation for the PC system. On many systems, the required key is F12, F2, F1, or Delete.
  - c. Adjust the boot menu or BIOS boot order settings to make sure that the CD ROM is the first drive in the boot order.
  - d. Eject the CD ROM bay and load *Fedora 10 LiveCD*.
  - e. Save changes and exit the boot menu or BIOS setup.
  - f. The PC system will boot from the CD ROM.

In the next three steps, the PC system is booted with a Linux operating system (Fedora 10 LiveCD) and the device drivers are loaded to make the connection between the hardware SP605 board and the software application.

2. Boot *Fedora OS Live* and automatically log in:
  - a. The images in [Figure 5](#) are displayed on power up. Wait two to three minutes, depending on the system configuration.



*Figure 5: Fedora Screens*

- b. Click **Login** to enter. Wait one to two minutes, depending on the system configuration.
3. Copy the contents of the USB flash drive:
  - a. The reference design files are provided on the USB flash drive delivered with the kit.
  - b. Insert the USB flash drive into a USB connector of the PC system.
  - c. Wait for the Fedora 10 operating system to mount the USB flash. When the flash is mounted, an icon pops up on the desktop.
  - d. Double-click on the USB flash drive icon and copy the `s6_pcie_dma_ddr3_gbe_axi` folder into the liveuser's home folder/directory. Note that the design folder for the version of the TRD without AXI4 protocol is called `s6_pcie_dma_ddr3_gbe`. However, the directory structure and general setup instructions are common between the two designs.
  - e. To unmount the USB flash, right-click on the USB flash drive icon and select **Unmount Volume**.



4. Compile the driver and insert the kernel module:
  - a. Navigate to the `s6_pcie_dma_ddr3_gbe_axi` folder.
  - b. Double-click **s6\_trd\_driver\_build** to build the kernel objects and a GUI (see [Figure 6](#)). Wait one to two minutes for this step to complete.

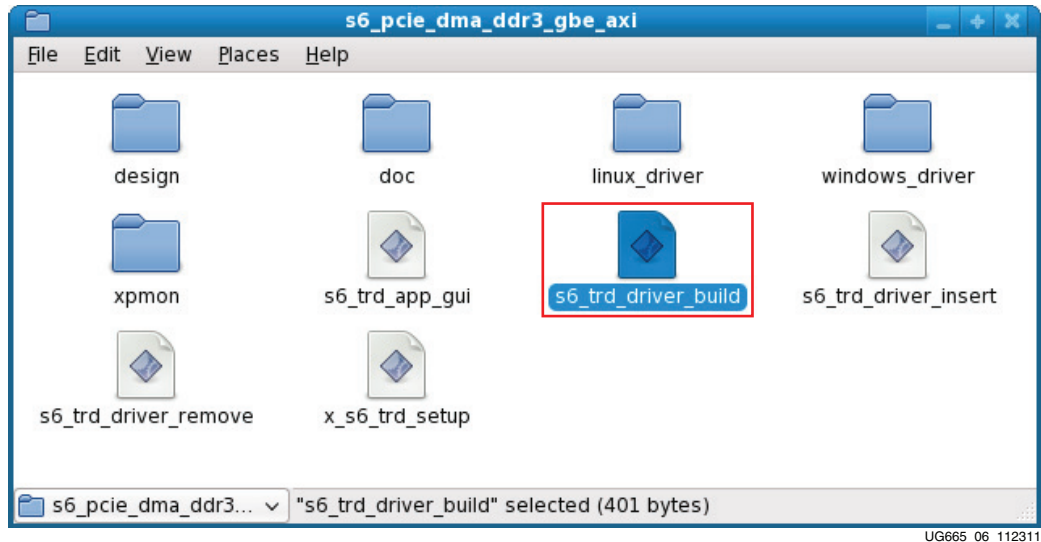


Figure 6: Build and Insert the Spartan-6 FPGA PCIe to Gigabit Ethernet Driver

- c. A window prompt appears as shown in [Figure 7](#).
  - Click **Run in Terminal** to proceed.
  - Wait approximately one to two minutes for this step to complete.

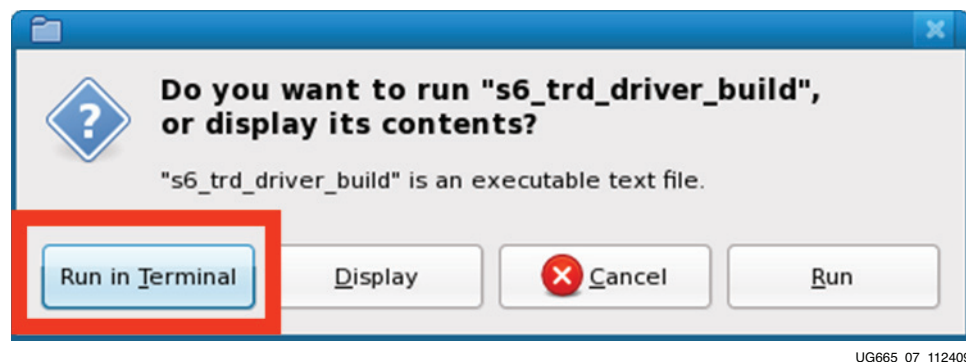
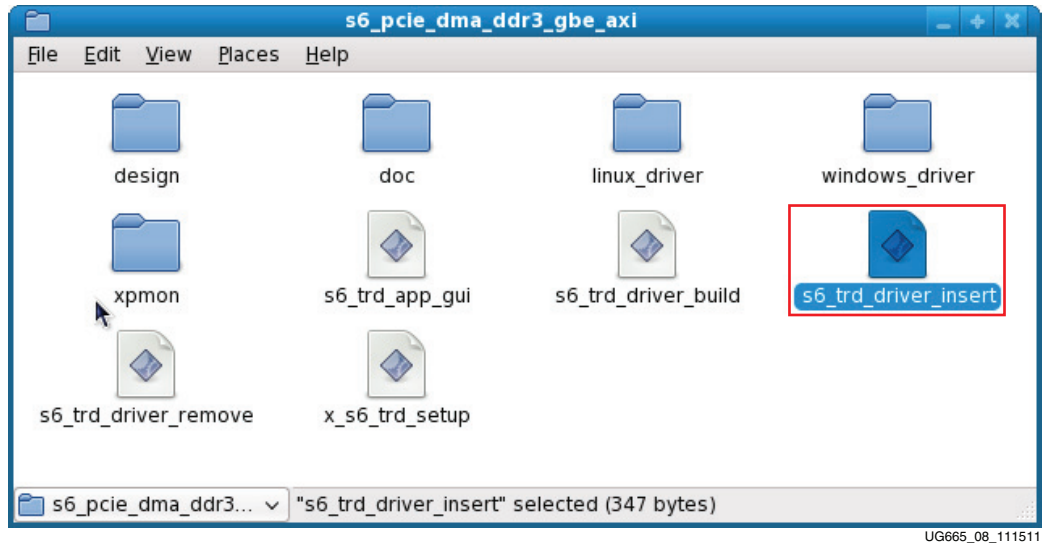


Figure 7: Run `s6_trd_driver_build`

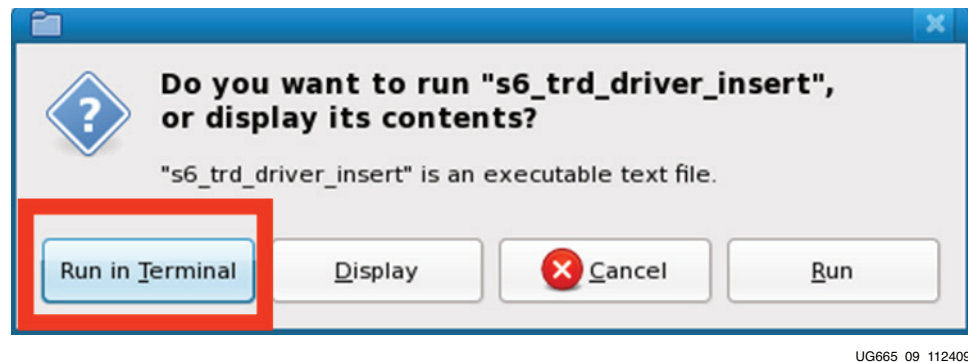
- d. Scroll and check the terminal for errors. If there are none, press any key to exit the terminal window.

- e. Double-click **s6\_trd\_driver\_insert** to insert the driver modules into the kernel (see [Figure 8](#)).



*Figure 8:* File to Insert the Driver Modules into the Kernel

- f. A window prompt appears as shown in [Figure 7](#). Click **Run in Terminal** to proceed.



*Figure 9:* Run s6\_trd\_driver\_insert

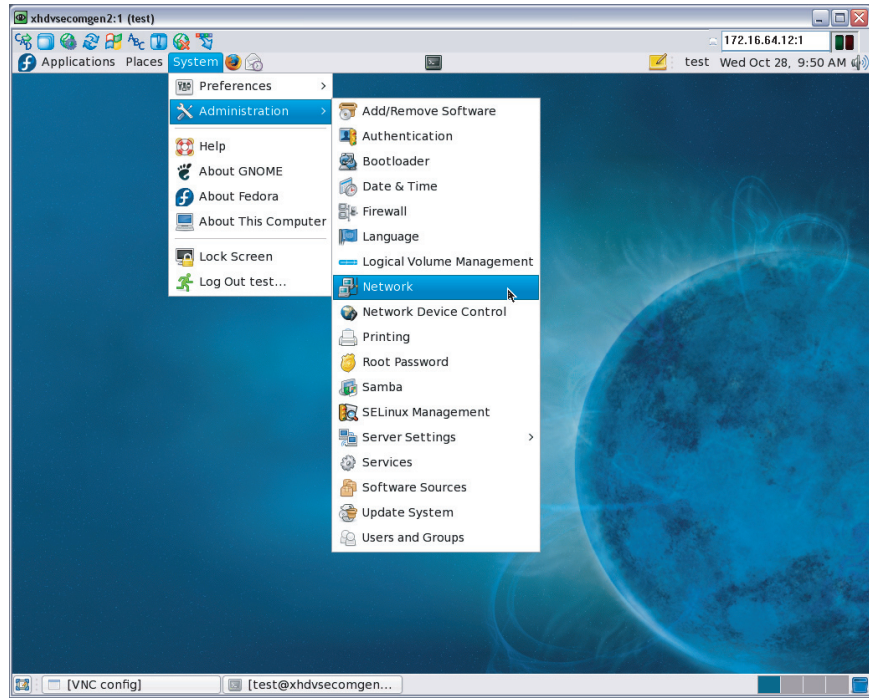
- g. Scroll and check the terminal for errors. If there are none, press any key to exit the terminal window.

In the next five steps, the Ethernet LAN connection to the SP605 board is set up and configured to enable and perform the Network Interface Controller function.

5. Network Setup I – Configure the network:

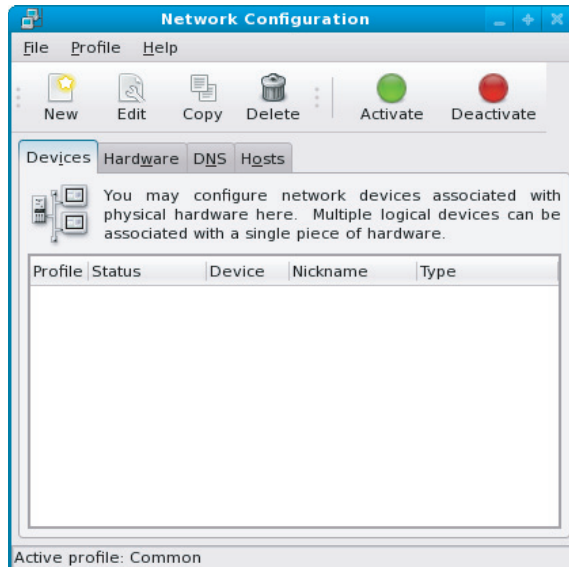
Add a new network device:

- Open the Network Configuration GUI.
- Select **System** → **Administration** → **Network** (see Figure 10).



UG665\_10\_121709

Figure 10: Navigate to Open the Network Configuration GUI



UG665\_11\_121709

Figure 11: Network Configuration Dialog

6. Network Setup II – Create a new device:

The Hardware tab shows the hardware devices present. For the example flow in this document, the SP605 board is identified as *eth1* as shown in Figure 12.

**Note:** The SP605 board might not always be eth1. It depends on the existing Ethernet interfaces on the system.

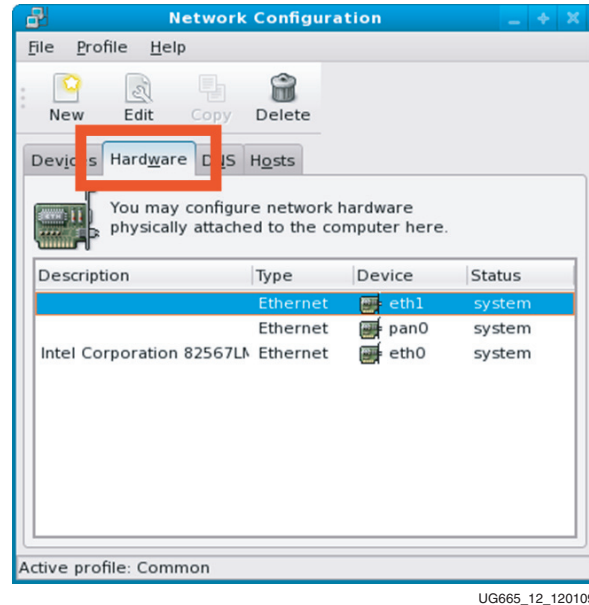


Figure 12: Hardware Tab

a. The Devices tab is empty.

To get the SP605 board to appear in the Devices tab (see Figure 13), a new Ethernet connection needs to be created:

- Click the Devices tab.
- Select **New** → **Create New Ethernet Connection**.

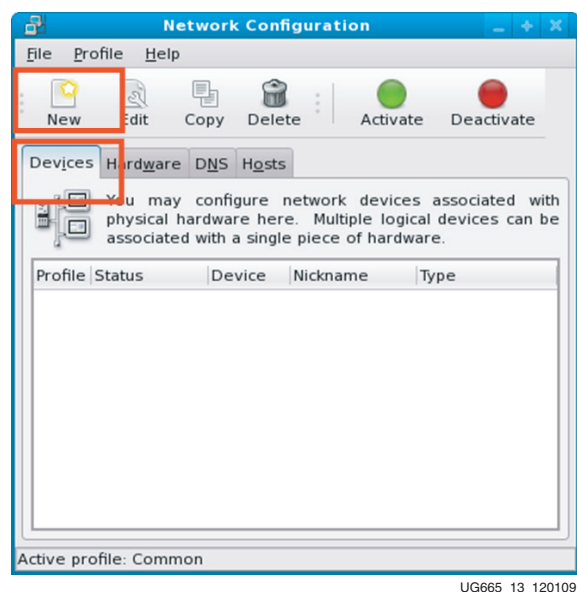
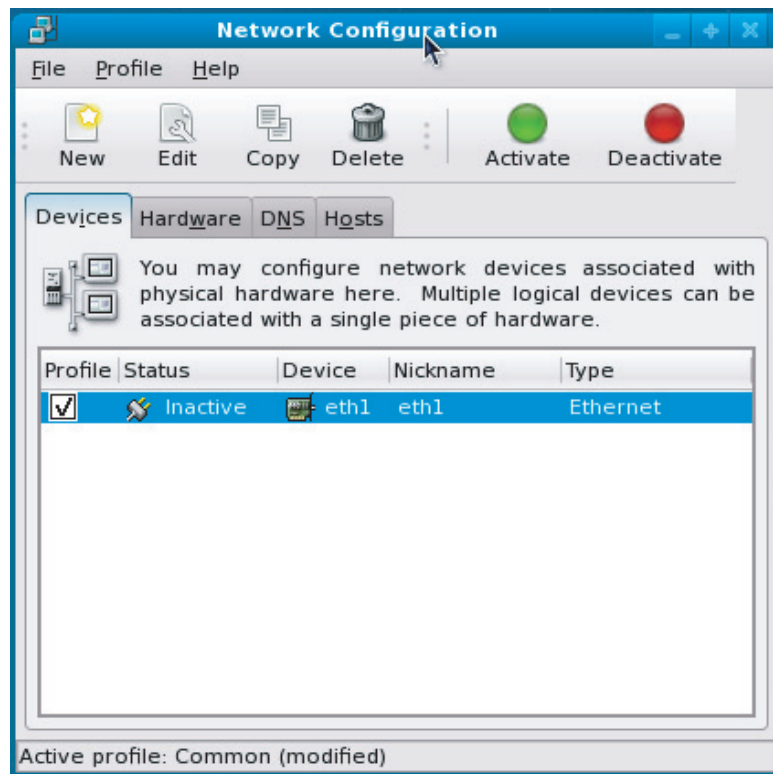


Figure 13: Devices Tab

7. Network Setup III – Create a new Ethernet connection:
  - a. Follow the instructions on the screen to complete the setup process. If the Ethernet connection is already working, this NIC is detected as the eth1 interface. Select **eth1**.

**Note:** The SP605 board might not always be eth1. It depends on the existing Ethernet interfaces on the system.
  - b. IP address assignment can be static or dynamic depending on the network setup.
    - Contact your network administrator to understand the IP address assignment on the network and to obtain the necessary settings for network configuration.
    - Enter the appropriate DNS settings for DHCP configuration as per the network administrator's instructions.
  - c. Save changes by selecting **File** → **Save**, and click **OK** to accept the changes.
  - d. When this step is complete, the screen in [Figure 14](#) appears.



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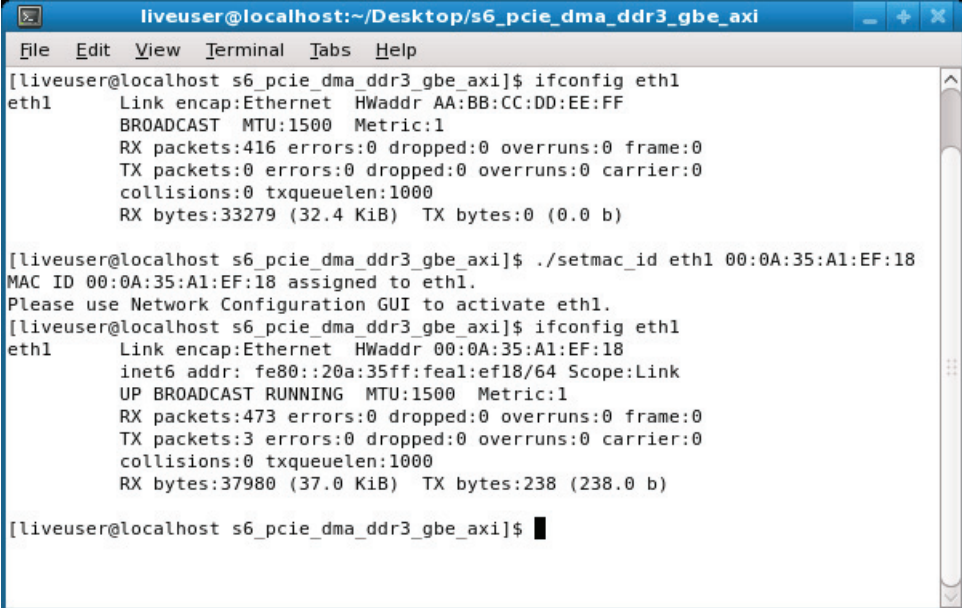
Figure 14: New Ethernet Connection

8. Network Setup IV – Assign the MAC address:
  - a. Open a terminal by selecting **Applications** → **System Tools** → **Terminal**.
  - b. Navigate and change the directory to `s6_pcie_dma_ddr3_gbe_axi`.

```
$ cd s6_pcie_dma_ddr3_gbe_axi
```

- c. Use the `ifconfig` utility to check the device (see [Figure 15](#)).

```
$ /sbin/ifconfig eth1
```



```
liveuser@localhost:~/Desktop/s6_pcie_dma_ddr3_gbe_axi
File Edit View Terminal Tabs Help
[liveuser@localhost s6_pcie_dma_ddr3_gbe_axi]$ ifconfig eth1
eth1      Link encap:Ethernet  HWaddr AA:BB:CC:DD:EE:FF
          BROADCAST  MTU:1500  Metric:1
          RX packets:416 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:33279 (32.4 KiB)  TX bytes:0 (0.0 b)

[liveuser@localhost s6_pcie_dma_ddr3_gbe_axi]$ ./setmac_id eth1 00:0A:35:A1:EF:18
MAC ID 00:0A:35:A1:EF:18 assigned to eth1.
Please use Network Configuration GUI to activate eth1.
[liveuser@localhost s6_pcie_dma_ddr3_gbe_axi]$ ifconfig eth1
eth1      Link encap:Ethernet  HWaddr 00:0A:35:A1:EF:18
          inet6 addr: fe80::20a:35ff:fe18/64 Scope:Link
          UP BROADCAST RUNNING  MTU:1500  Metric:1
          RX packets:473 errors:0 dropped:0 overruns:0 frame:0
          TX packets:3 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:37980 (37.0 KiB)  TX bytes:238 (238.0 b)

[liveuser@localhost s6_pcie_dma_ddr3_gbe_axi]$
```

UG665\_15\_090810

**Figure 15: Assigning the MAC Address to the NIC**

- d. Set the MAC address for the Ethernet MAC in the design using the provided script. Use the MAC address obtained in [step 3, page 13](#).

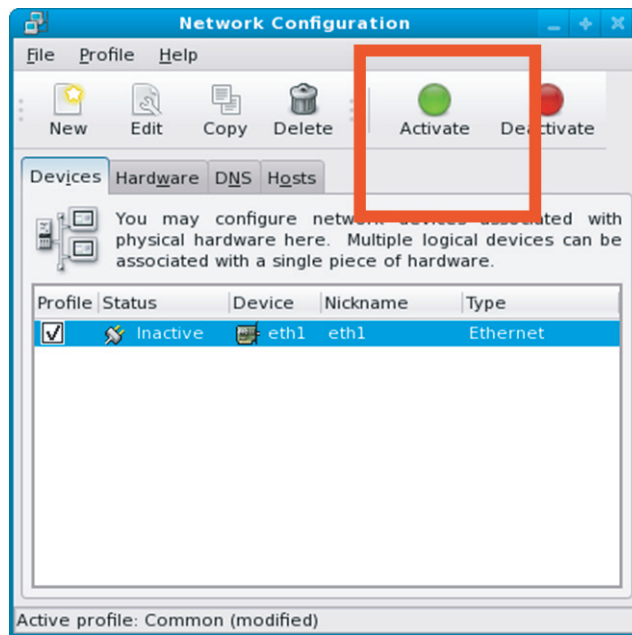
```
$ ./setmac_id eth1 <SP605_MAC_ID>
```

e.g., `./setmac_id eth1 00:01:02:03:04:05`

- e. When the MAC ID is assigned, retry the `ifconfig` utility to verify that the MAC ID is assigned to the NIC.

```
$ /sbin/ifconfig eth1
```

9. Network Setup V – Activate the Ethernet connection:
  - a. Open the Network Configuration GUI.
  - b. Activate the Ethernet interface by clicking the **Activate** button (see Figure 16).



UG665\_16\_112409

Figure 16: Activating the Spartan-6 FPGA NIC

- c. Set the Internet preferences:
  - Click on **System** → **Preferences** → **Internet and Network Proxy** → **Network Proxy**.
  - Contact your network administrator for more details on these settings.
- d. Now the Internet can be browsed.
  - To launch the web browser, select **Applications** → **Internet** → **Firefox Web Browser**.
  - Wait for one to two minutes for the browser window to display on the screen, depending on the system configuration.

## Testing with the Windows XP Operating System

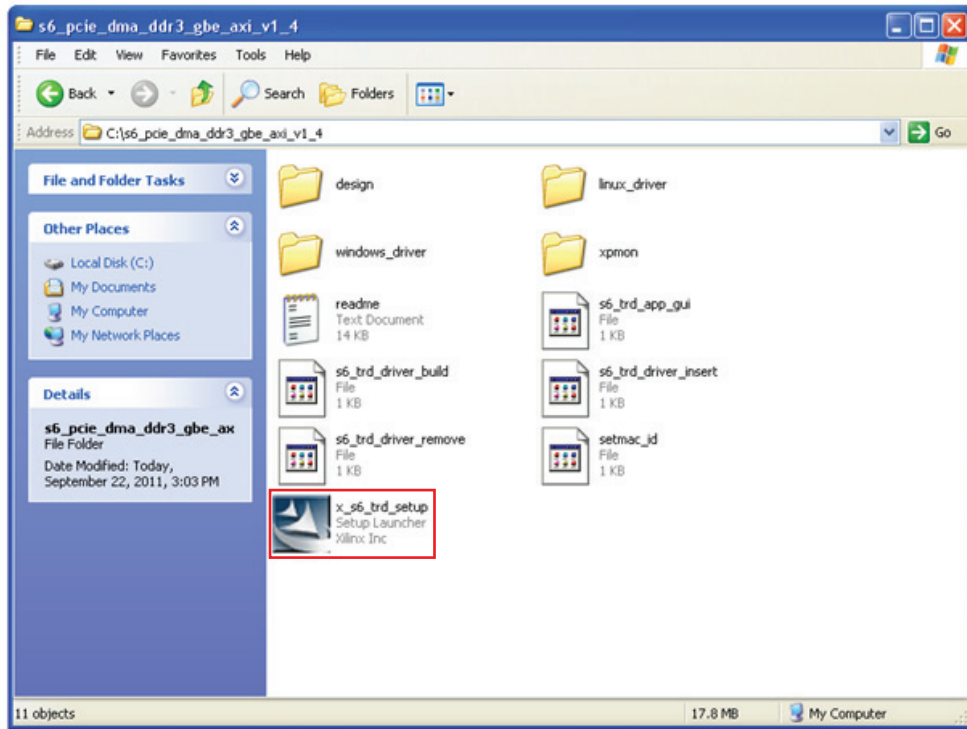
### Copy the contents of the USB flash drive

The reference design files are provided on the USB flash drive delivered with the connectivity kit. Insert the flash drive into a USB connector on the PC system and copy the `s6_pcie_dma_ddr3_gbe_axi` directory to the PC system.

**Note:** Ensure that the path where the `s6_pcie_dma_ddr3_gbe_axi` directory is located does not have spaces.

### Install the Drivers and GUI

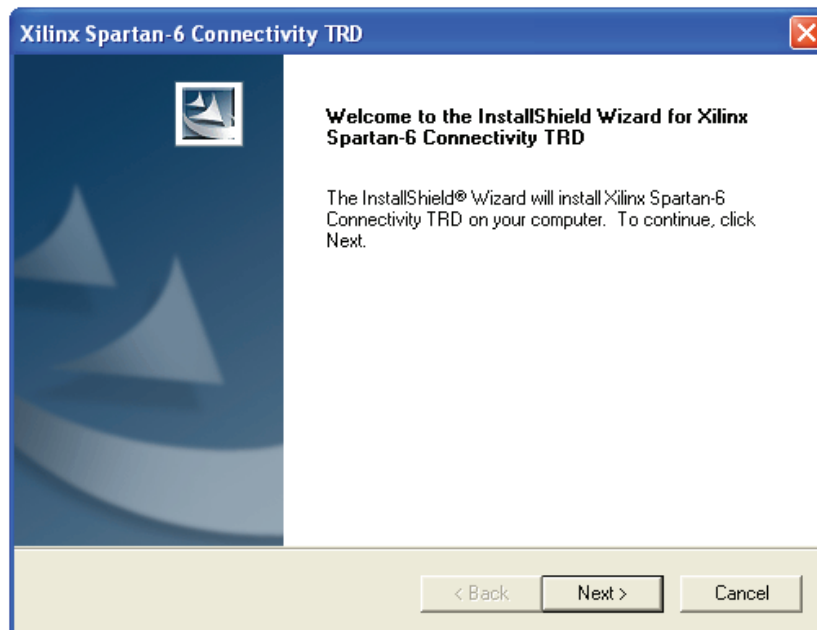
1. Navigate to the `s6_pcie_dma_ddr3_gbe_axi` directory. Double click `x_s6_trd_setup.exe` (Figure 17).



UG665\_53\_111511

Figure 17: Location of x\_s6\_trd\_setup.exe

2. When the InstallShield Wizard dialog box opens, click **Next** (Figure 18).

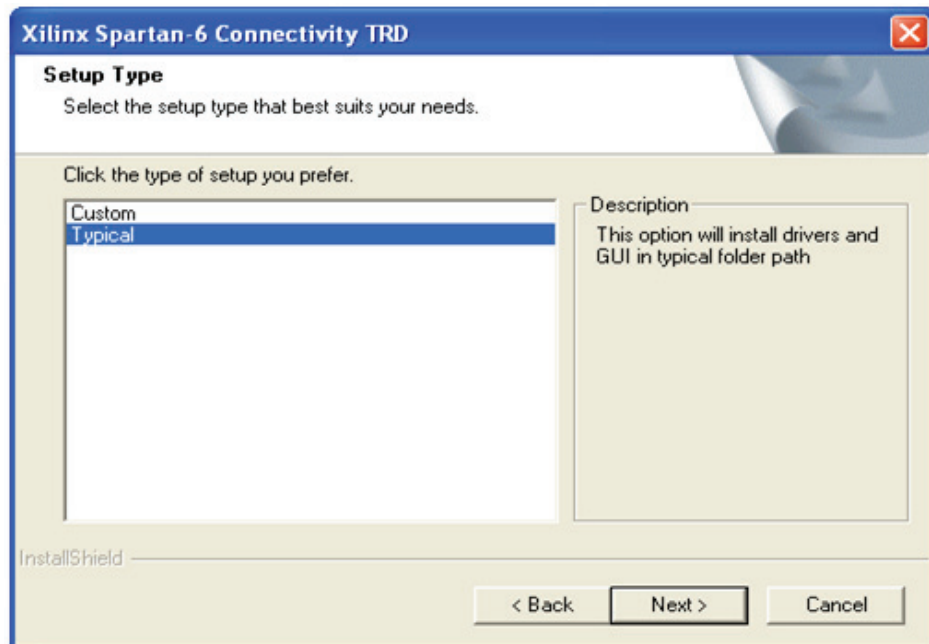


UG665\_54\_111511

Figure 18: InstallShield Wizard



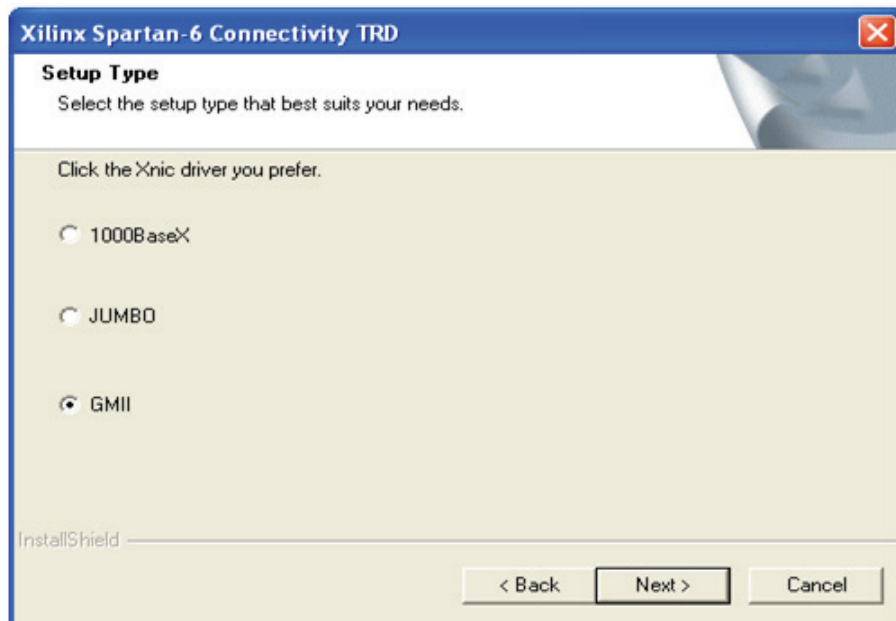
- When the Setup Type dialog box opens, select **Typical** (Figure 19). This option installs the driver files and directories to the C:\Program Files directory. Click **Next**.



UG665\_55\_102511

Figure 19: Typical Setup Selected

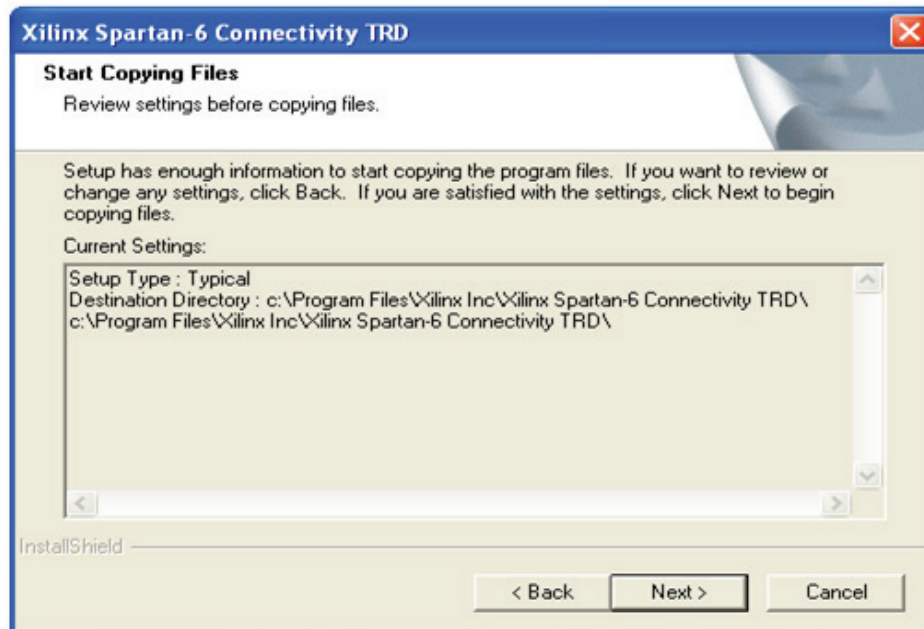
- When the XNIC driver selection dialog box opens (Figure 20), select the driver type that matches the MAC to PHY interface used by the SP605 board. For example, if the bitfile programs the SP605 board to use GMII, select **GMII**. Click **Next**.



UG665\_56\_102511

Figure 20: XNIC Driver Selection

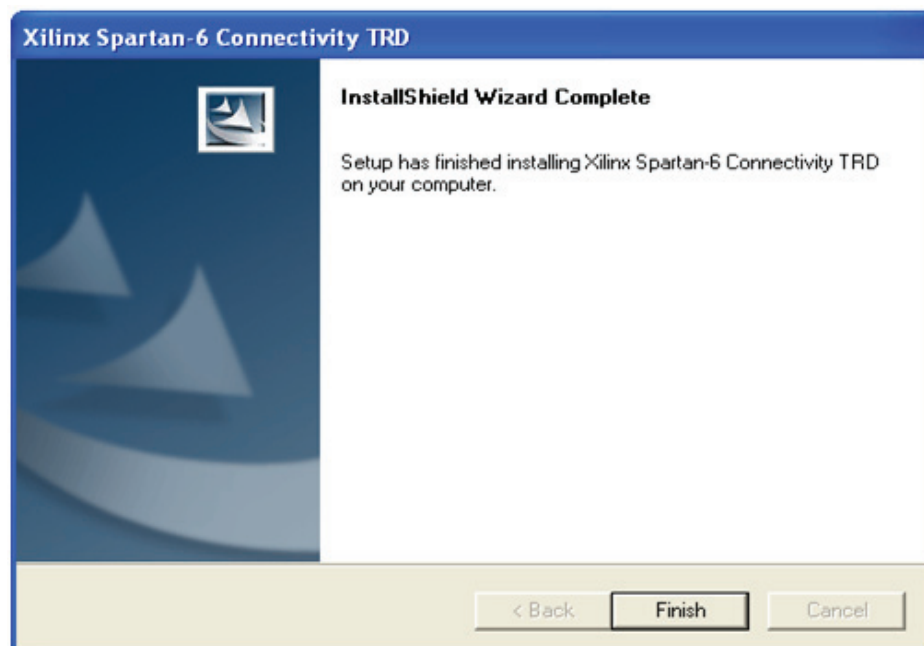
- The current settings show the destination directory where the program files will be located (Figure 21). Review and click **Next**.



UG665\_57\_102511

Figure 21: Review Settings Window

- When the InstallShield Wizard Complete dialog box opens (Figure 22), click **Finish**.



UG399\_58\_102511

Figure 22: Installation Complete

## Add Hardware Wizard

After the drivers are detected by Windows, the Add Hardware Wizard opens (Figure 23). Click **Next**.



Figure 23: Add new Hardware Wizard

## Add Xilinx DMA Driver Device

1. When the Found New Hardware Wizard opens (Figure 24). Select **Install the software automatically** and click **Next**.

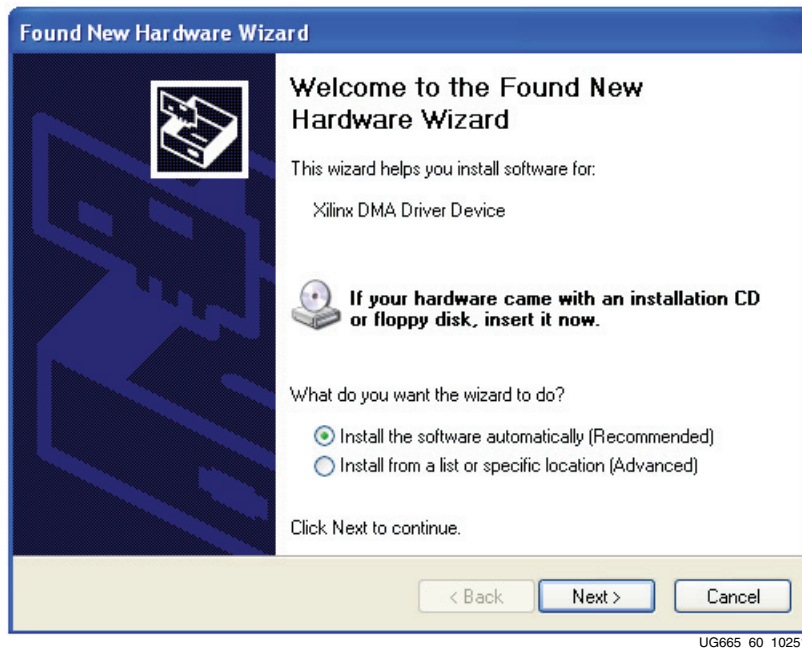


Figure 24: Found XDMA Hardware

- When the XDMA driver is installed [Figure 25](#) opens. Click **Finish**.

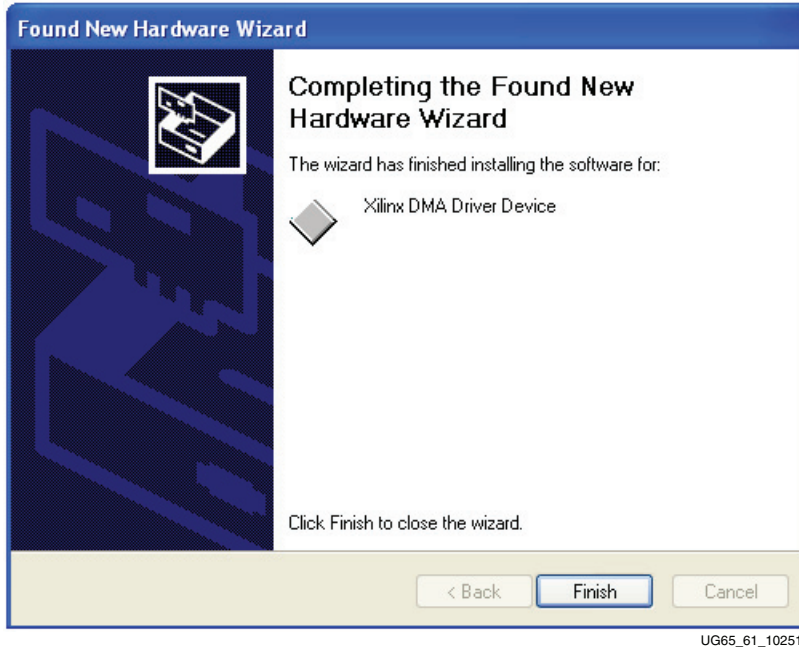


Figure 25: XDMA Driver Installation Complete

#### Add Xilinx Ethernet Adapter

- [Figure 26](#) indicates the Add Hardware Wizard detects the XNIC driver must be installed. Select **Install the software automatically** and click **Next**.

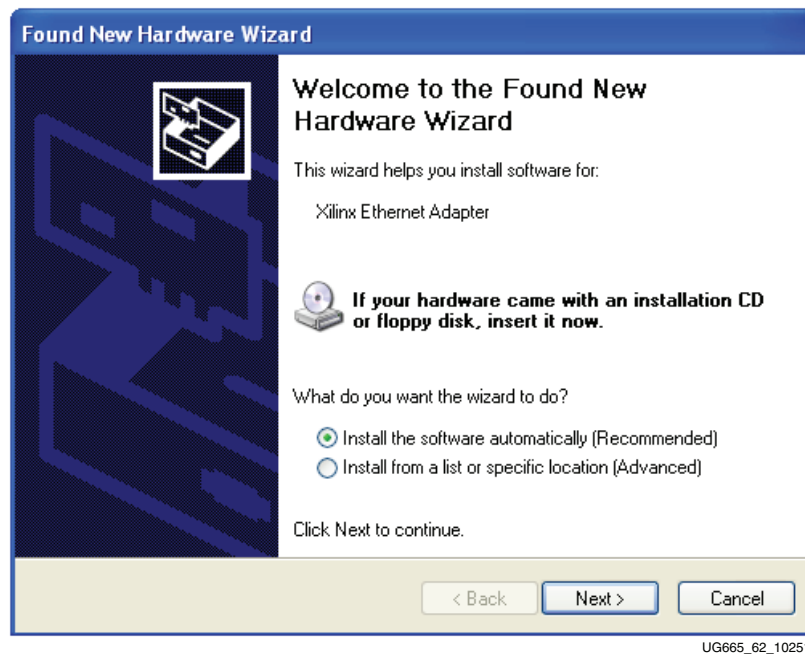
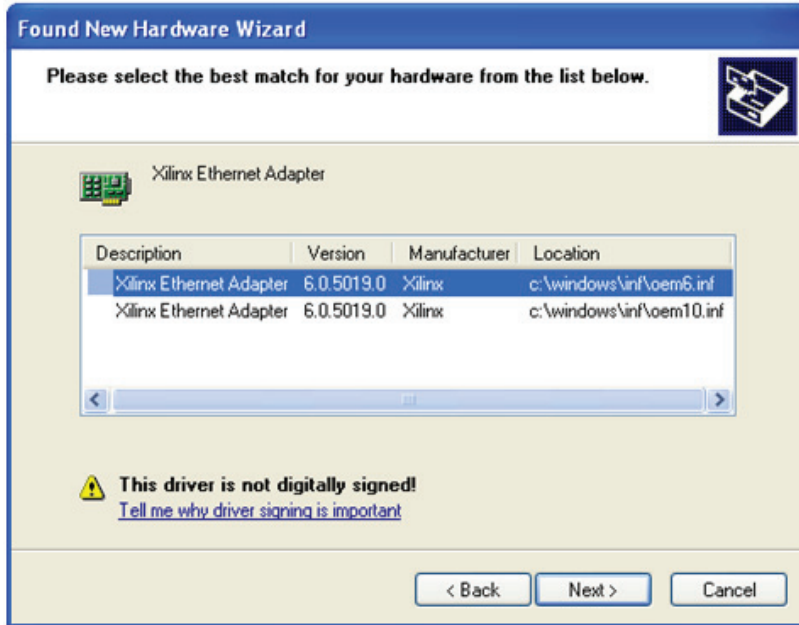


Figure 26: Found XNIC Hardware

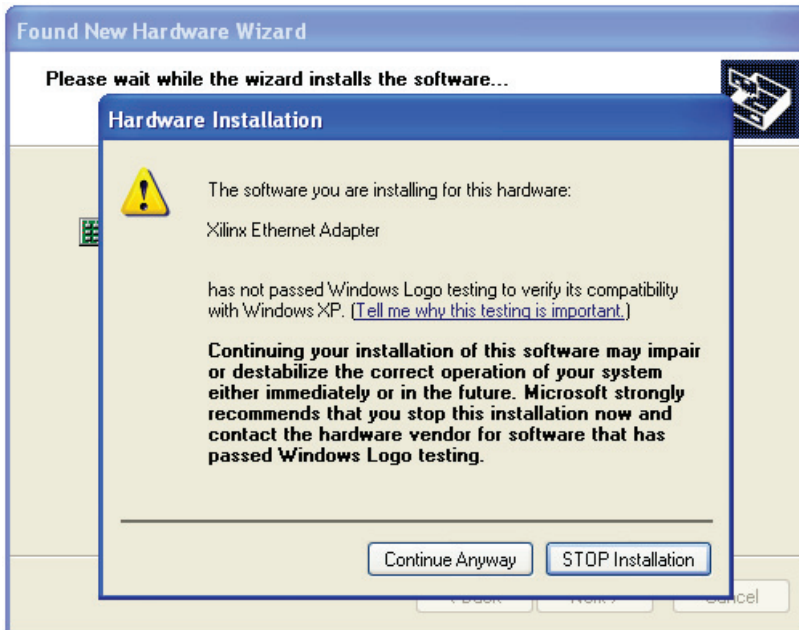
2. Select the appropriate Xilinx Ethernet Adapter and click **Next** (Figure 27).



UG665\_63\_102511

Figure 27: Ethernet Adapter Selection

3. If the dialog box shown in Figure 28 opens, click **Continue Anyway**.



UG665\_64\_102511

Figure 28: Windows Compatibility Test Dialog Box

4. When the XNIC driver is installed [Figure 29](#) opens. Click **Finish**.

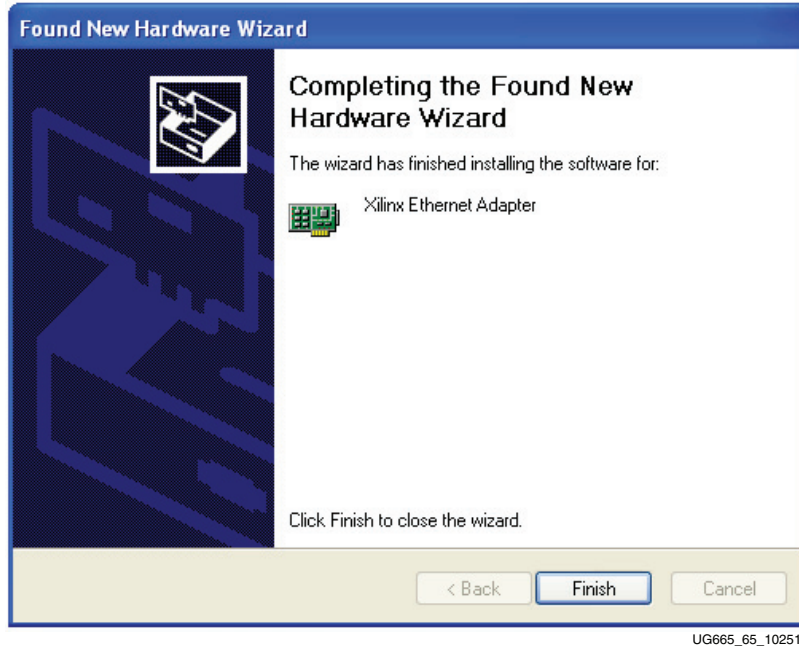


Figure 29: XNIC Driver Installation Complete

#### Add Xilinx Block Driver Device

1. [Figure 30](#) indicates the Add Hardware Wizard detects the XBLOCK driver must be installed. Select **Install the software automatically** and click **Next**.

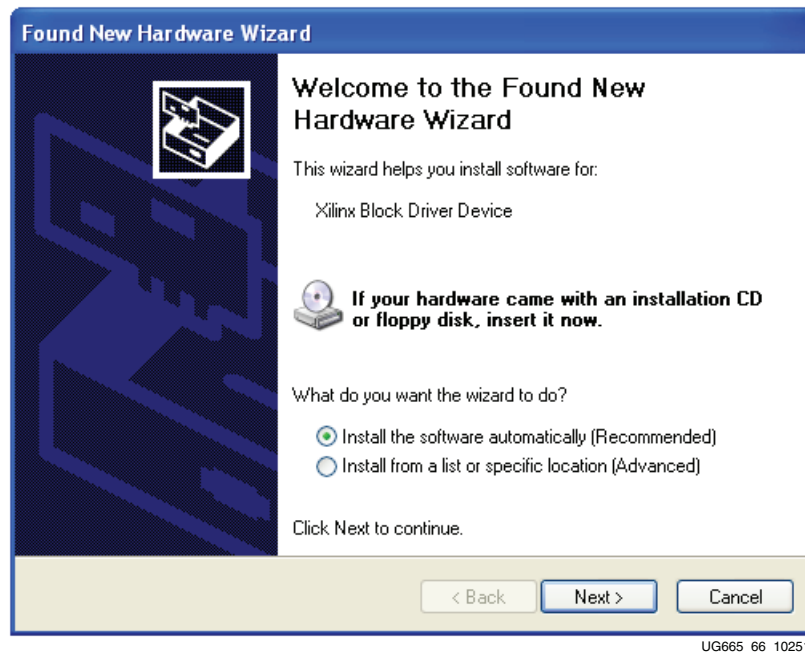


Figure 30: Found XBLOCK Hardware

- When the XBLOCK driver is installed [Figure 31](#) opens. Click **Finish**.

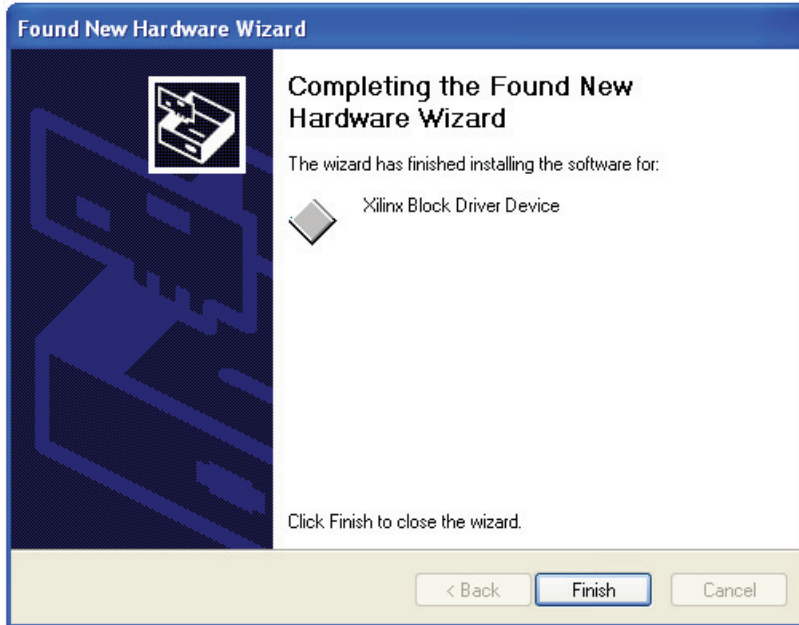


Figure 31: XBLOCK Driver Installation Complete

- Upon completion, the Add Hardware Wizard lists the devices installed. Click **Finish** ([Figure 32](#)).

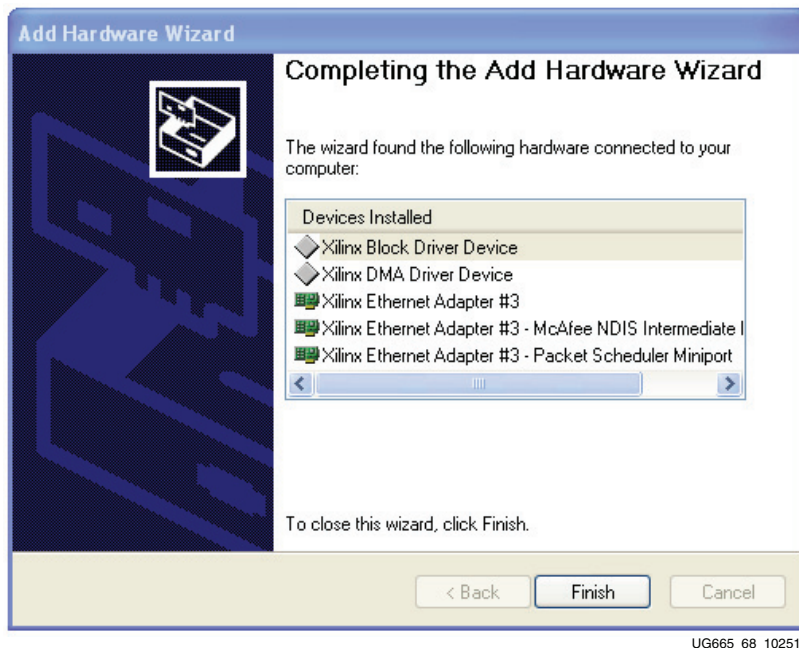


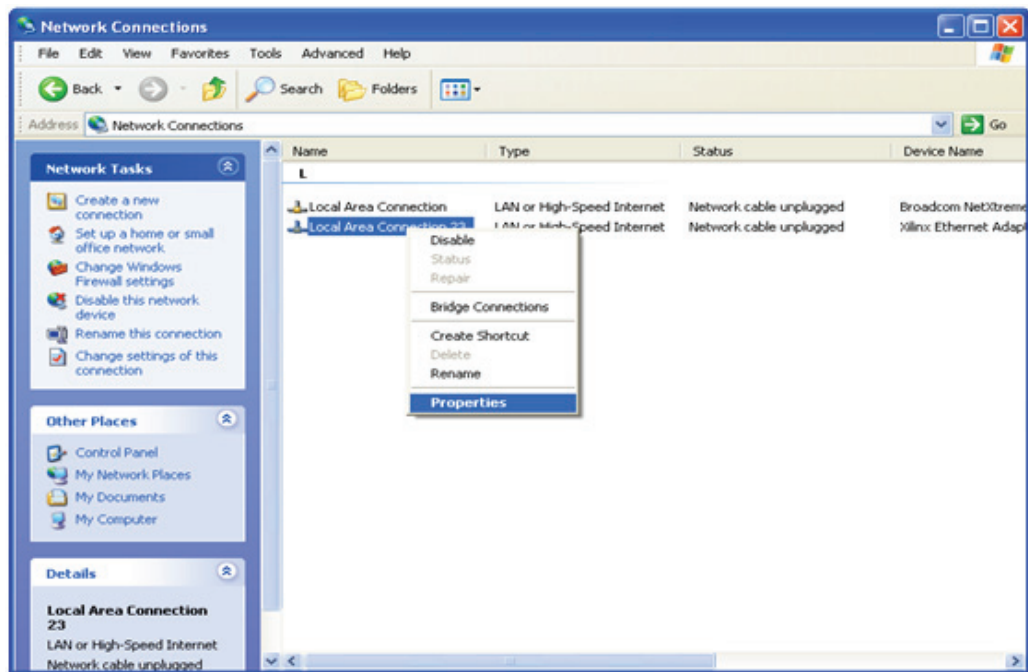
Figure 32: List of Installed Drivers

**Note:** Running `x_s6_trd_setup.exe` after the drivers are installed will uninstall the drivers and clean the install folders. Do not run `x_s6_trd_setup.exe` except when installing new versions of the drivers.

## Configuration

After the drivers are installed, Configure the Xilinx Ethernet Adapter as follows:

1. Browse to Network Connections and click **Set up a home or small office network**.
2. Right click on the **Local Area Connection  $n$** , where  $n$  depends on the number of LAN ports supported in the PC that has Xilinx Ethernet Adapter in the Device Name field.
3. Click Properties as shown in [Figure 33](#).

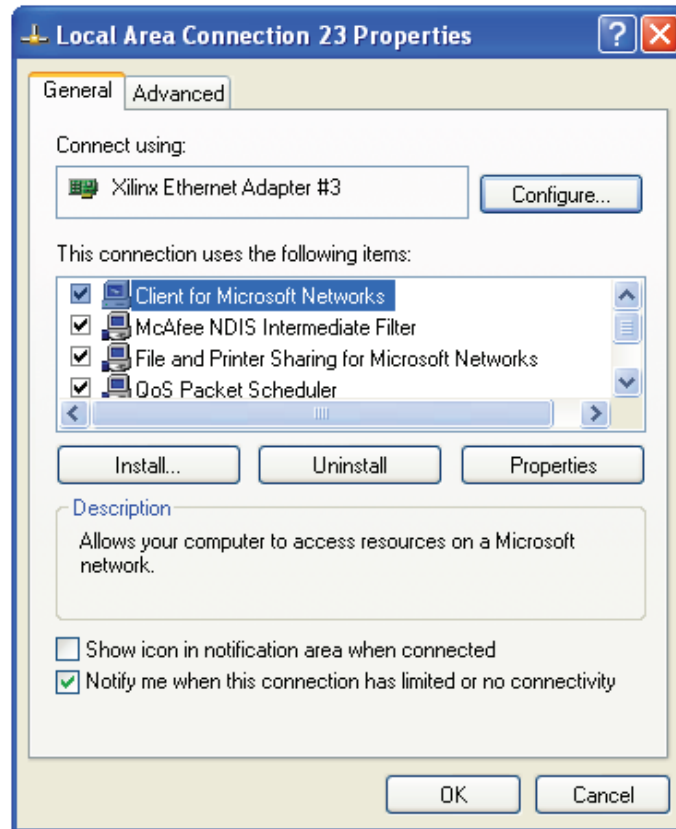


UG665\_71\_102511

Figure 33: Local Area Connection Properties



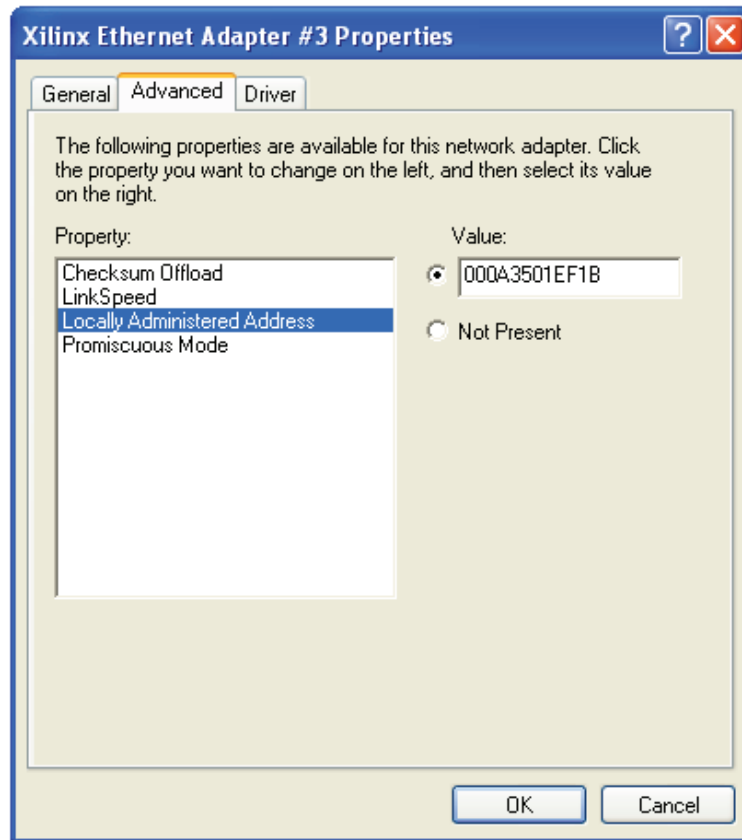
- When the Local Area Connection  $n$  properties window opens (Figure 34), select the **General** tab and click **Configure**.



UG665\_72\_121411

Figure 34: Local Area Connection Properties

- Click the **Advanced** tab. Select **Locally Administered Address** as shown in [Figure 35](#). Enter a value that matches with one written on the edge of your SP605 board (as shown in [Figure 2, page 14](#)). Click **OK**.



UG665\_73\_121411

Figure 35: Advanced Configuration Option

6. On the Local Area Connection Properties window, select **Internet Protocol (TCP/IP)** selection as shown in Figure 36 to configure the IP address of you Xilinx Ethernet Adapter.

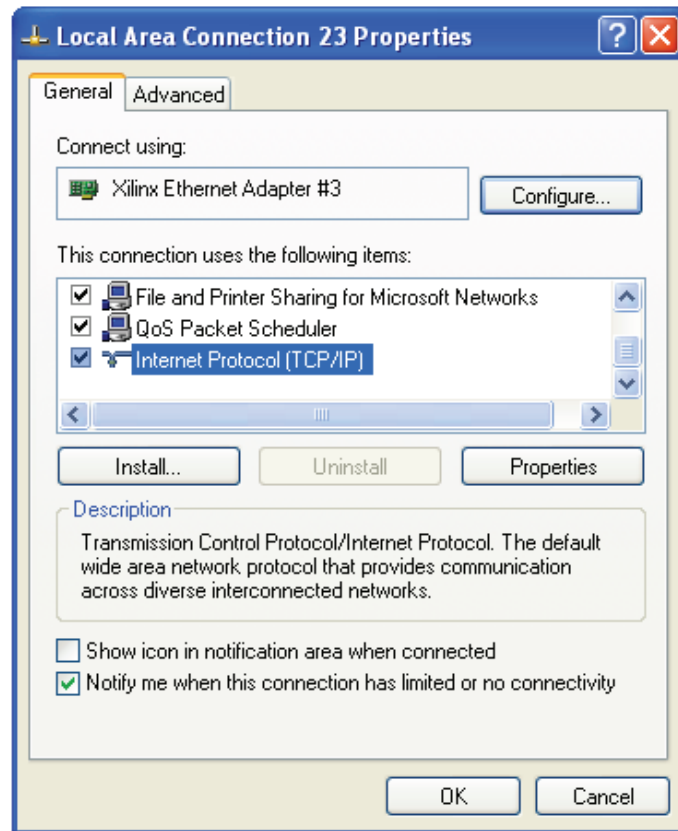


Figure 36: Internet Protocol Properties

**Note:** IP address allocation varies based on the network connection. Contact the network administrator to obtain network connection details on type of network connection (for example, whether IP address allocation is static or dynamic) and proxy settings requirements, if any.

The Spartan-6 FPGA Connectivity Kit is now set up. The pre-built connectivity targeted reference design demonstration has been tested, using the built-in block for PCI Express (x1 PCI Express v1.1 specification configuration), Ethernet LogiCORE IP module, a Virtual FIFO memory controller designed around the built-in memory controller block, which interfaces to the onboard DDR3 memory, and a third-party DMA controller for PCI Express.

## Evaluating the Spartan-6 FPGA Connectivity Targeted Reference Design

The Spartan-6 FPGA Connectivity Targeted Reference Design provides a Performance and Status monitor application and GUI. The application enables customers to evaluate different system parameter optimizations. This section demonstrates key performance criteria for the Memory and the PCI Express interfaces.

To evaluate the Spartan-6 FPGA connectivity targeted reference design:

### On the Linux Operating System

1. Launch the connectivity targeted reference design in the Performance Monitor:
  - a. Navigate to the `s6_pcie_dma_ddr3_gbe_axi` folder.
  - b. Double-click **s6\_trd\_app\_gui** to launch the Xilinx Performance Monitor and Status GUI.

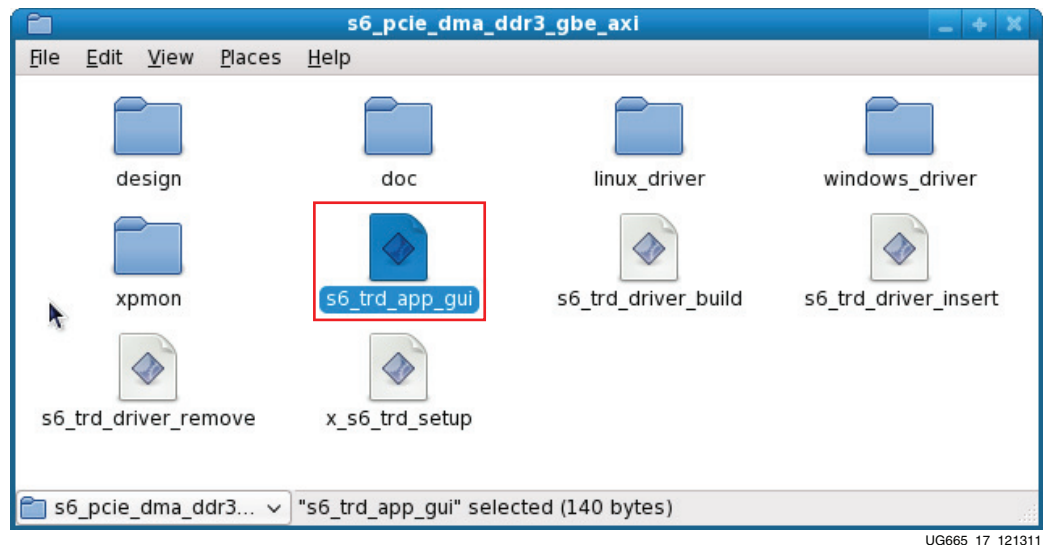


Figure 37: File to Launch the Xilinx Performance and Status Monitor GUI

- c. A window prompt appears as shown in Figure 38. Click **Run in Terminal** to proceed.



Figure 38: Run s6\_trd\_app\_gui

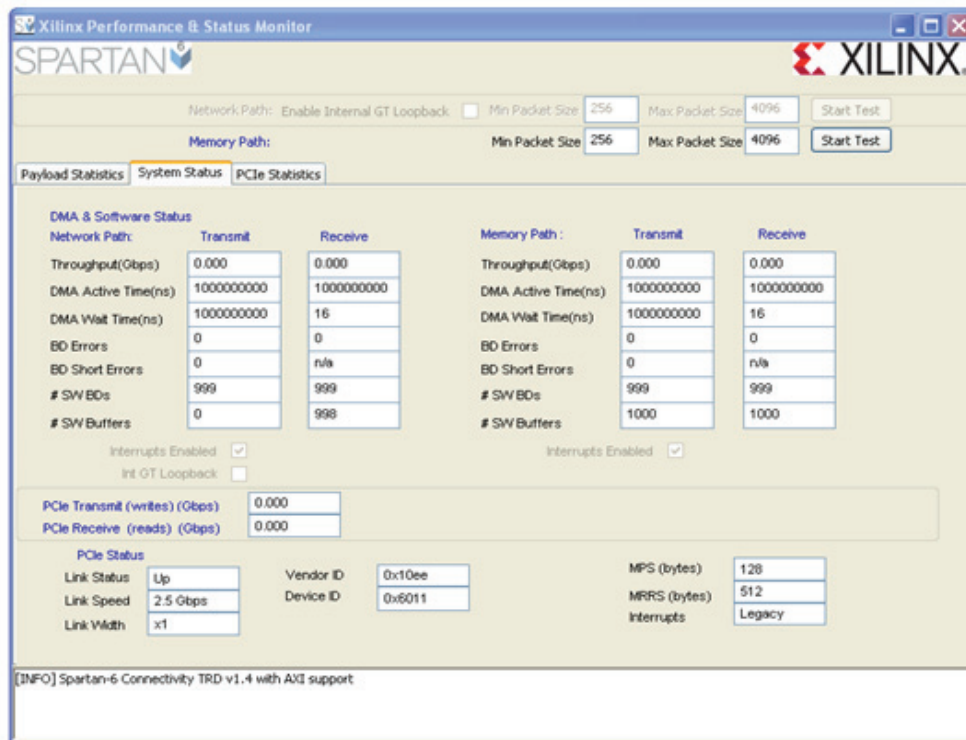
## On the Windows Operating System

To launch the Performance and Status Monitor application (Figure 40) from the desktop, double-click the **xpmon** icon (Figure 39). The xpmon icon is also available in the C:\ProgramFiles\XilinxInc\Xilinx Spartan-6 Connectivity Kit-SP605 directory.



UG665\_69\_112811

Figure 39: Xilinx Performance and Status Monitor Icon

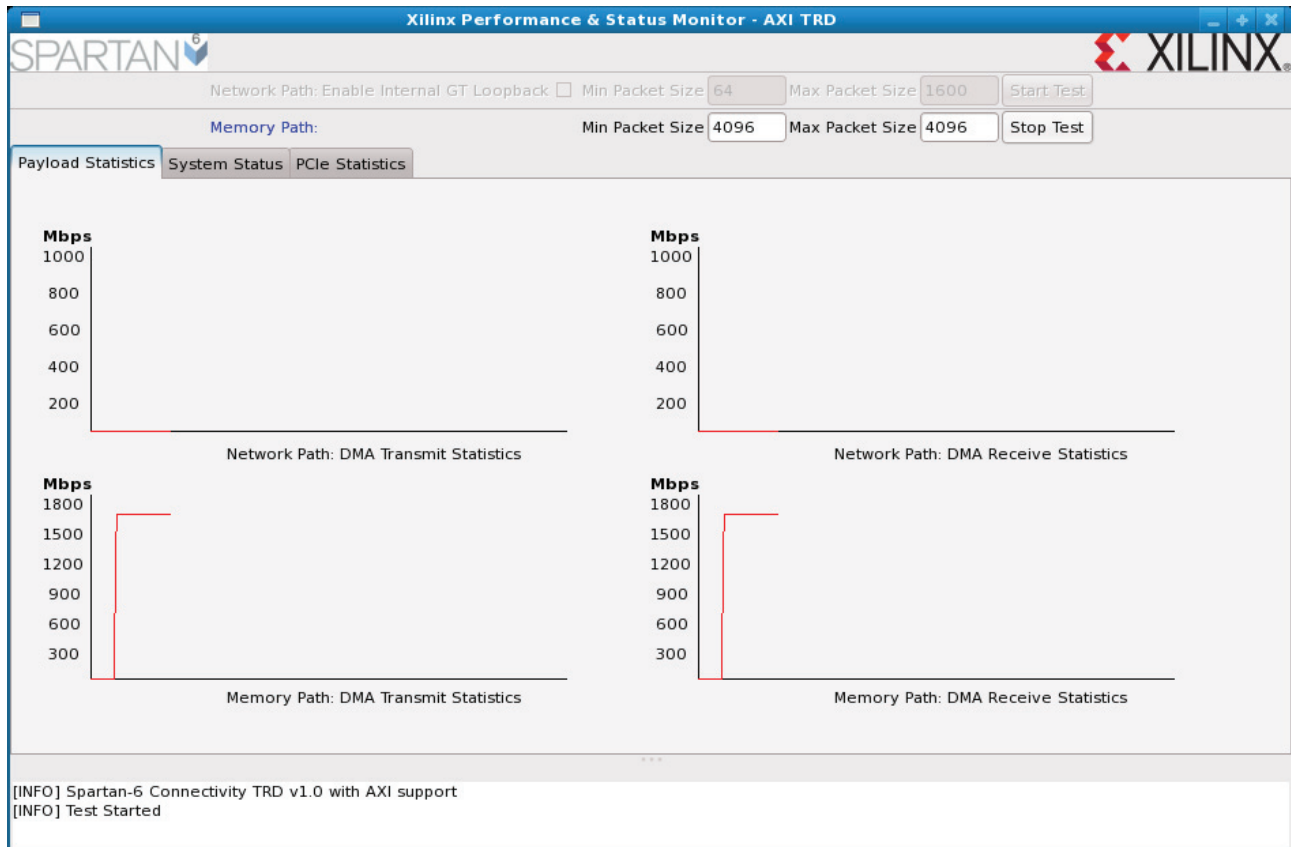


UG665\_70\_112811

Figure 40: Xilinx Performance Monitor GUI

1. Set up the test in the Performance Monitor:
  - a. Two *Data Transmission* options are provided:
    - Network Path  
Because there is already a connection to the Ethernet, setting Network Path (Ethernet) options is not available through the GUI interface.
    - Memory Path (DDR3)

- b. This *Packet Size* option is provided:
  - Memory Path (DDR3)  
Minimum Packet Size: Choose a value between 256 – 4096  
Maximum Packet Size: Choose a value between 256 – 4096
2. Execute the test and view payload statistics in Performance Monitor:
  - a. Click **Start Test** to start the performance test.
  - b. View the payload statistics to review data transfers on the Network Path (Ethernet) and Memory Path (DDR3) channels of the DMA engine (see [Figure 41](#)).



UG665\_19\_090810

Figure 41: DDR3 Memory Interface Performance

- View the PCIe statistics in Performance Monitor (see [Figure 42](#)).  
Click **PCIe Statistics** to view data transfer numbers on the PCIe interface.

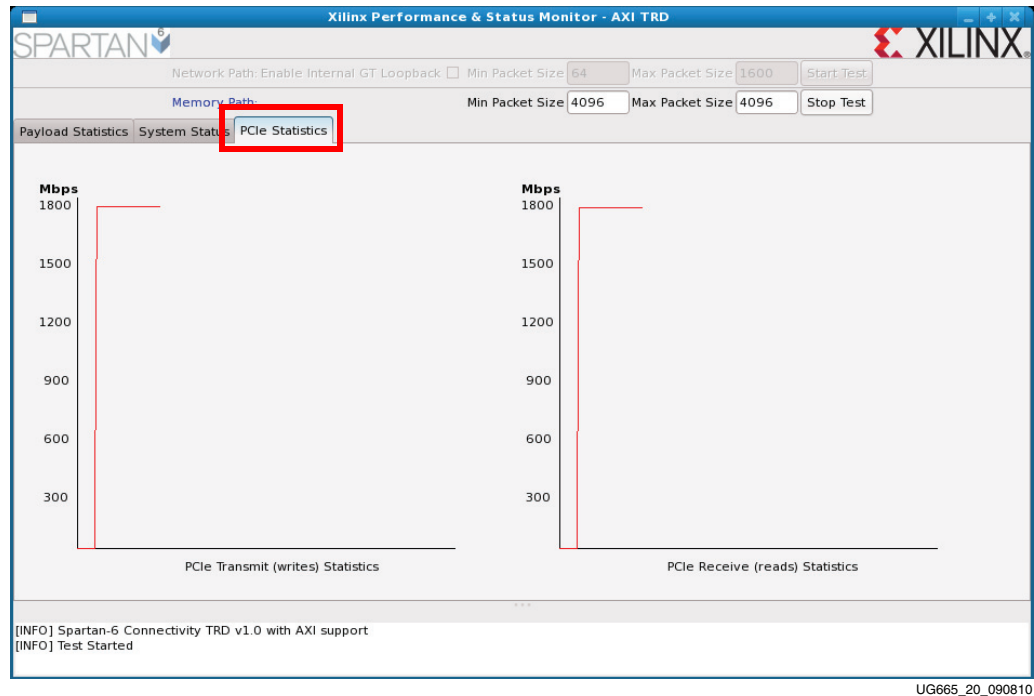


Figure 42: PCIe Interface Performance

- Review the system status (see [Figure 43](#)):  
Click **System Status** to review:
  - PCIe link status, Vendor ID, and Device ID information
  - DMA data/channel activity for the Ethernet and DDR3 interfaces

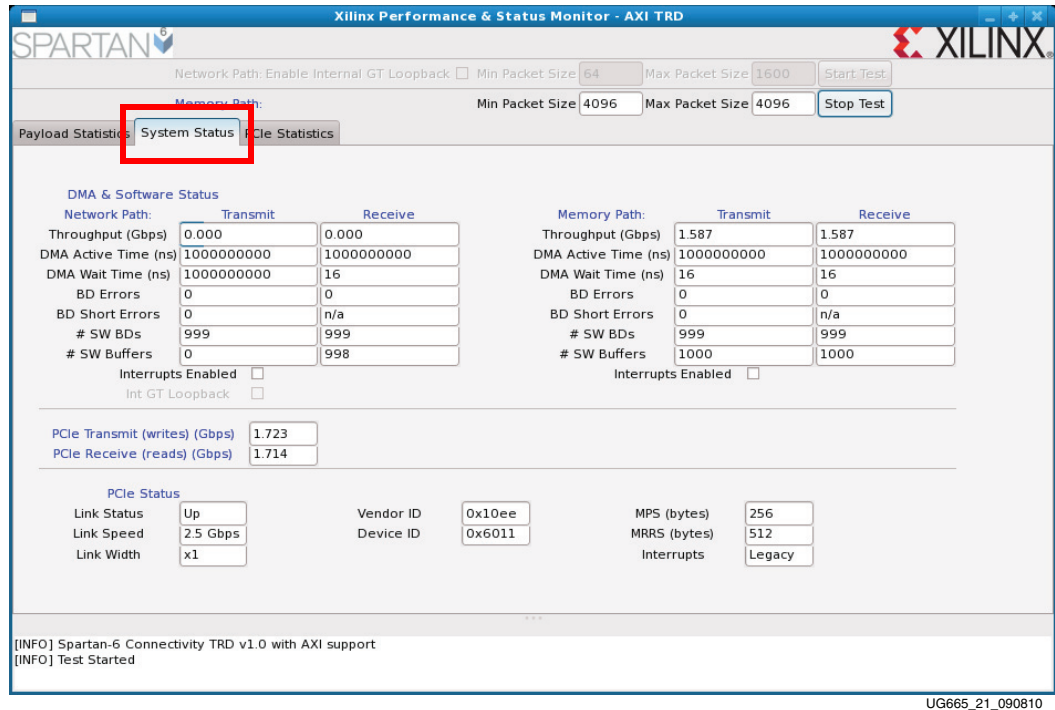


Figure 43: System Status Information

Congratulations! The system performance of the Spartan-6 FPGA Connectivity Kit has been evaluated using the pre-built demonstration design. This design includes the built-in block for PCI Express (x1 PCI Express v1.1 specification configuration), Ethernet LogiCORE IP, a Virtual FIFO memory controller designed around the built-in memory controller block, which interfaces to the onboard DDR3 memory, and a third-party DMA controller for PCI Express.

## Installation and Licensing of ISE Design Suite

This Spartan-6 FPGA Connectivity Kit comes with an entitlement to a full seat of the ISE Design Suite: Embedded Edition that is device locked to a Spartan-6 LX45T FPGA. This software can be installed from the DVD or the Web installer can be downloaded from <http://www.xilinx.com/support/download/index.htm>.

For detailed information on licensing and installation, refer to UG631, *ISE Design Suite: Installation, Licensing, and Release Notes*, located on the Xilinx documentation site at <http://www.xilinx.com/support/documentation>.

### Downloading and Installing Tool and IP Licenses

This connectivity kit provides an entitlement to a node-locked license to the ISE Design Suite: Embedded Edition and all associated updates for a one-year period. This connectivity kit also provides an entitlement to a single seat of production netlist licenses for the Northwest Logic x1 PCIe Packet DMA IP Core for Spartan-6 LXT FPGAs (node-locked license), and all associated updates for a one-year period.

The files for the production netlist of Northwest Logic Packet DMA IP core for PCI Express are available on the USB stick included with the Spartan-6 FPGA Connectivity Kit. The

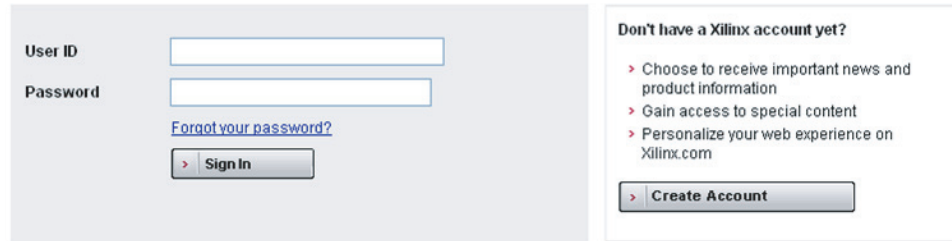


entitlement is activated after the licensing steps below are completed. With the Production Netlist, designers are entitled to target their designs to any Spartan-6 FPGA.

The key steps to download and install the ISE Design Suite and Northwest Logic IP licenses for the PC are:

1. Visit the Xilinx software registration and entitlement site at: <http://www.xilinx.com/getproduct>
2. Log in to an existing account or create a new account, if needed (see Figure 44).

### Sign in to Xilinx Product Download and Licensing Site



UG665\_22\_112409

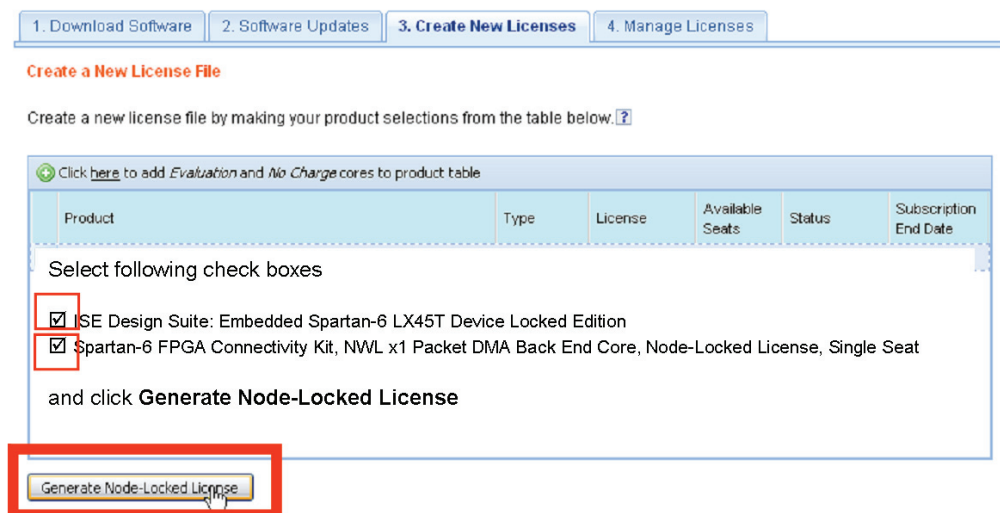
Figure 44: Xilinx Product Download and Licensing Site

3. After logging in, there might be a prompt to verify your shipping address. After the shipping address has been verified or updated, click **Next**.
4. Select these checkboxes (see Figure 45):

- ISE Design Suite: Embedded Spartan-6 LX45T Device Locked Edition
- Spartan-6 FPGA Connectivity Kit, NWL x1 Packet DMA Back End Core, Node-Locked License, Single Seat

**Note:** The delivered design is built with an evaluation version of the DMA netlist. To build a design with a full netlist, obtain the license and then refer to steps mentioned in the `readme.txt` file in the `s6_pcie_dma_ddr3_gbe_axi` directory.

Then click **Generate Node-Locked License**.



UG665\_23\_112409

Figure 45: Create a New License File

5. Follow the instructions to generate the license by providing your Host OS information and Host ID (disk serial number or Ethernet MAC address).
6. Click the **Manage Licenses** tab to download the license file or to check your email for the license file attachment.
7. To start the Xilinx License Manager, select **Start** → **Programs** → **ISE Design Suite** → **Manage Xilinx Licenses** and click **Copy License** to install the license on the computer (see Figure 46).

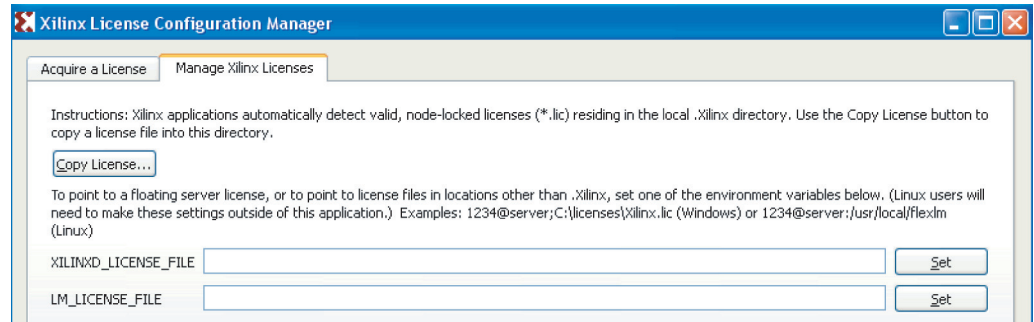


Figure 46: Manage Xilinx Licenses

The Xilinx ISE Design Suite: Embedded Edition can now be used to create or modify custom connectivity systems using the Spartan-6 LX45T FPGA resources.

For detailed information on licensing and installation, refer to UG631, *ISE Design Suite: Installation, Licensing, and Release Notes*, located on the Xilinx documentation site at <http://www.xilinx.com/support/documentation>.

Congratulations! The ISE Design Suite tools and the Northwest Logic DMA IP core are now installed and the licenses are set up for the Embedded Edition of the tools and the core.

## The Connectivity Design is Ready for Modification

Now that the FPGA-based connectivity demonstration has been set up and evaluated and installation is complete of the ISE Design Suite: Embedded Edition, the connectivity design for the Spartan-6 FPGA LX45T can be modified. This step provides an understanding of the simplified flow of the Xilinx tools and design methodologies as they apply to the Spartan-6 FPGA Connectivity Kit and the connectivity targeted reference design.

# Modifying the Spartan-6 FPGA Connectivity Targeted Reference Design

This section describes how to modify the design:

- Hardware and RTL modifications
- Software and driver modifications

## Hardware Modifications

This section describes how the hardware is modified. This exercise modifies the *PCI Express Vendor ID*.

To make RTL design changes and implement the design, follow these steps:

1. Use the PC system or laptop on which the Xilinx design tools were installed.
2. Copy the contents of the included USB stick into a local directory on this machine.
3. Make design changes:
  - a. Navigate to the `s6_pcie_dma_ddr3_gbe_axi/design/source/` directory.
  - b. Edit the `s6_pcie_dma_ddr3_gbe_axi.v` file.
  - c. Search for this string: `CFG_VEN_ID`.
  - d. Change the alphanumeric value `10EE` on this line to the Vendor ID assigned to your company by PCI-SIG (e.g., the Vendor ID for Xilinx is `10EE`). Change this value to `19AA`. With these changes, the line reads as:

```
localparam [15:0] CFG_VEN_ID = 16'h19AA;
```
  - e. Save changes and exit.
4. Build and implement the design:
  - a. Open a terminal window. Set up Xilinx environment for tools.
  - b. Navigate to the `s6_pcie_dma_ddr3_gbe_axi/design/implement/` directory.
  - c. Follow the implementation flow steps depending on the operating system:
    - For Linux: Navigate to the `lin` directory and execute this command on the command line:

```
$ ./implement_gmii.sh
```

(for a GMII design using the Marvell PHY)
    - For Windows: Navigate to the `nt` directory and execute **implement\_gmii.bat** (for a GMII design using the Marvell PHY)
  - d. After successful implementation of the design, a `results` folder with these FPGA programming files is generated:
    - FPGA programming bit file: `<filename>.bit` (in this case, it is `sp605_use_gmii.bit`)
    - SPI x4 flash programming MCS file: `<filename>.mcs` (in this case, it is `sp605_use_gmii.mcs`)
5. Program the FPGA:
  - a. If the SP605 board is still plugged into the PC system, shut down the PC system and remove the SP605 board.
  - b. To program the FPGA using SPI x4 flash, change the Mode switch (SW1) settings to: `M0 = 1` and `M1 = 0`.

- c. Ensure that jumper J46 is ON (the jumper is in place).
  - d. For all other SP605 switch and jumper settings, keep them at the factory default configuration as indicated in [UG526](#), *SP605 Hardware User Guide*.
6. Set up the board:
- a. Connect the mini USB cable to the USB-JTAG connector as shown in [Figure 47](#). The other end of the USB cable is connected to the PC system or laptop on which the Xilinx design tools were installed.

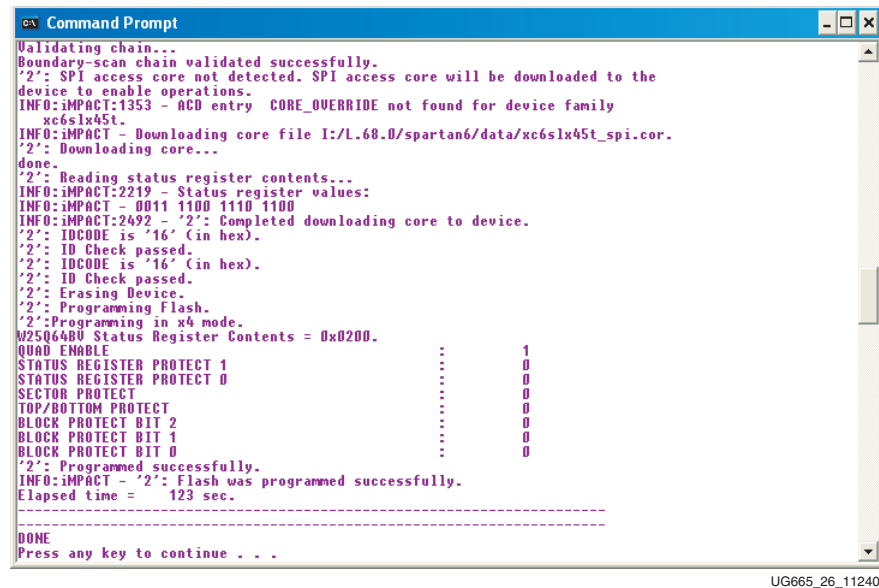


UG665\_25\_120109

**Figure 47: Connecting the USB Cable**

- b. Use the included wall power adapter to provide 12V power to the 6-pin connector.
7. Program the onboard SPI x4 flash:
- a. Open a terminal window.
  - b. Navigate to the `s6_pcie_dma_ddr3_gbe_axi/design/reference/configuration` directory.
  - c. Copy the FPGA programming files from the implementation directory to this directory.
    - FPGA programming bit file: `<filename>.bit`
    - SPI x4 flash programming MCS file: `<filename>.mcs`
  - d. Execute the FPGA programming script at the command prompt. This operation takes approximately 4 to 5 minutes to complete.
    - `$ impact -batch spi_program.cmd` (for Linux based machines)
    - `$ spi_program.bat` (for Windows based machines)

- e. A command shell is opened. After successful completion, the *Programmed successfully* message should appear (see [Figure 48](#)).



```

c:\> Command Prompt
Validating chain...
Boundary-scan chain validated successfully.
'2': SPI access core not detected. SPI access core will be downloaded to the
device to enable operations.
INFO:iMPACT:1353 - ACD entry CORE_OVERRIDE not found for device family
xc6s1x45t.
INFO:iMPACT - Downloading core file I:/L.68.0/spartan6/data/xc6s1x45t_spi.cor.
'2': Downloading core...
done.
'2': Reading status register contents...
INFO:iMPACT:2219 - Status register values:
INFO:iMPACT - 0011 1100 1110 1100
INFO:iMPACT:2492 - '2': Completed downloading core to device.
'2': IDCODE is '16' (in hex).
'2': ID Check passed.
'2': IDCODE is '16' (in hex).
'2': ID Check passed.
'2': Erasing Device.
'2': Programming Flash.
'2': Programming in x4 mode.
M25Q64B0 Status Register Contents = 0x0200.
QUAD ENABLE : 1
STATUS REGISTER PROTECT 1 : 0
STATUS REGISTER PROTECT 0 : 0
SECTOR PROTECT : 0
TOP/BOTTOM PROTECT : 0
BLOCK PROTECT BIT 2 : 0
BLOCK PROTECT BIT 1 : 0
BLOCK PROTECT BIT 0 : 0
'2': Programmed successfully.
INFO:iMPACT - '2': Flash was programmed successfully.
Elapsed time = 123 sec.
-----
DONE
Press any key to continue . . .
  
```

Figure 48: Programming the SP605 Board

- f. Turn off the power switch and remove the power connector.  
g. Carefully remove the mini USB cable.

The Spartan-6 FPGA connectivity targeted reference design is now modified and programmed into the SPI x4 flash and will automatically configure at power up.

## Test Setup

Follow [step 1](#) through [step 2](#) in [Connectivity Targeted Reference Design Hardware Demonstration Setup, page 13](#) to insert the board in the PC system and configure the FPGA with the design changes that were implemented.

## Software Modifications

This section describes how to modify the software on the [Linux Operating System](#) and on the [Windows Operating System](#). This exercise modifies the *PCI Express Vendor ID*.

### Linux Operating System

To make software design changes, follow these steps:

1. Use the PC system on which the SP605 Evaluation Board is installed.
2. Copy the contents of the included USB stick into a local directory on this machine.
  - a. Navigate to the `s6_pcie_dma_ddr3_gbe_axi/driver/xdma/` directory.
  - b. Edit the `xdma_base.c` file.
  - c. Search for this string: `#define PCI_VENDOR_ID_DMA`.
    - Change the alphanumeric value `10EE` found on this line, with the Vendor ID assigned to your company by PCI-SIG (e.g., the Vendor ID for Xilinx is `10EE`)
    - Change this value to `19AA`.

- Save the changes and exit.
- 3. Compile the driver and insert the kernel module:
  - a. Navigate to the `s6_pcie_dma_ddr3_gbe_axi` directory.
  - b. Double-click **s6\_trd\_driver\_build** to build the kernel objects and a GUI (see [Figure 6](#)).  
A window prompt appears as shown in [Figure 7](#). Click **Run in Terminal** to proceed.
  - c. Double-click **s6\_trd\_driver\_insert** to insert the driver modules into the kernel (see [Figure 8](#)).  
A window prompt appears as shown in [Figure 9](#). Click **Run in Terminal** to proceed.
- 4. Follow [step 5](#) through [step 9](#) in [Connectivity Targeted Reference Design Hardware Demonstration Setup, page 13](#) to completely evaluate the modified settings.
- 5. Follow [step 1](#) through [step 4](#) in [Evaluating the Spartan-6 FPGA Connectivity Targeted Reference Design, page 36](#) to evaluate the performance for the modified design.

## Windows Operating System

To change Vendor and Device ID:

1. navigate to the `windows_driver/xdma` directory.
2. Open the `xdma.inx` file in a text editor.
3. Search for the string `xdma_Inst` and add:  
**%xdma.DRVDESC%=xdma\_Inst, PCIIVEN\_19AA&DEV\_6011**  
This change allows the driver to support vendor ID 19AA
4. Save and close the file.
5. Recompile the drivers as described in Appendix F, [Compiling Windows Drivers in UG399, Spartan-6 FPGA Connectivity Targeted Reference Design with AXI4 Protocol User Guide](#).
6. From the desktop, double-click the **XPMON** icon to launch the Performance and Status Monitor.
7. Select the **System Status** tab to review PCIe link status, Vendor ID, and Device ID information. Confirm the vendor ID is 19AA corresponding to the change in [step 3](#).

The Spartan-6 FPGA Connectivity Kit using the connectivity targeted reference design is now fully set up and the system performance has been evaluated. The Xilinx design flow has been reviewed for modifying the connectivity targeted reference design. This design includes the built-in block for PCI Express (x1 PCI Express v1.1 specification configuration), Ethernet LogiCORE IP, a Virtual FIFO memory controller designed around the built-in memory controller block, which interfaces to the onboard DDR3 memory, and a third-party DMA controller for PCI Express.

## Next Steps

### Connectivity TRD Modules

This section outlines the correlation between the design modules and corresponding design source files for the various blocks of the design. Refer to [Figure 1, page 12](#) for the detailed block diagram of the Spartan-6 FPGA Connectivity TRD. [Table 1](#) shows the design

file organization per module.

**Table 1: Design File Organization for the Spartan-6 FPGA Connectivity TRD**

Module Name	Source Files / Directories	LogiCORE IP	Connectivity TRD Source
Top-Level Module: Spartan-6 FPGA Connectivity TRD	s6_pcie_dma_ddr3_gbe_axi (AXI4 protocol version) s6_pcie_dma_ddr3_gbe (version without AXI4 protocol)		?
PCI Express (x1)	s6_pcie_axi_st (AXI4 protocol version) s6_pcie_ip (version without AXI4 protocol)	? (Endpoint for PCIe core - CORE Generator output)	
Packet DMA	dma		Netlist deliverable only (from Northwest Logic)
Multiport Virtual FIFO	memory_app		?
Memory Controller Block	mig_axi_mm (AXI4 protocol version) mig_ip (version without AXI4 protocol)	? (MIG - CORE Generator output)	
Ethernet - GMII Interface	axi_ethernet_v1_00_a (AXI4 protocol version) xps_ll_temac_v2_03_a, network_app (version without AXI4 protocol)	? (Ethernet core - EDK IP output)	?
Ethernet 1000BASE-X	gig_eth_pcs_pma_ip (version without AXI4 protocol)	? (1000BASE-X PCS/PMA - CORE Generator output)	?
Clocking, Reset, Register Interface	common		?
Software Device Driver	linux_driver windows_driver		?
Software Application/ GUI	xpmon		?

For functional details on these modules, refer to the “Functional Description” chapter in UG 399, *Spartan-6 FPGA Connectivity Targeted Reference Design with AXI4 Protocol User Guide* for AXI4 protocol version, or [UG392](#), *Spartan-6 FPGA Connectivity Targeted Reference Design User Guide* for version without AXI4 protocol.

## PCI Express

Figure 49 shows the design module for PCI Express. Figure 50 shows the design file structure.

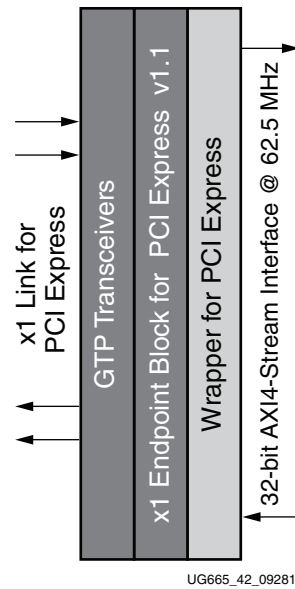


Figure 49: Design Module for PCI Express

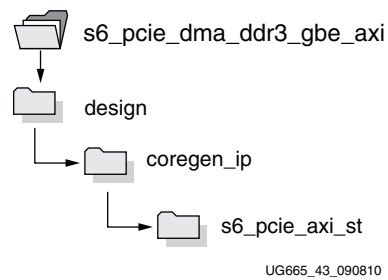


Figure 50: Design Files for PCI Express



## Packet DMA (with AXI4 Interface Wrapper)

Figure 51 shows the design module for Packet DMA. Figure 52 shows the design file structure.

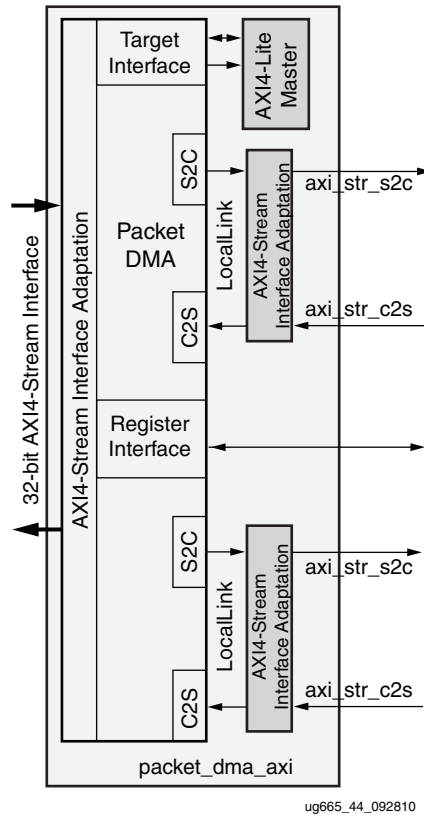


Figure 51: Packet DMA Design Module

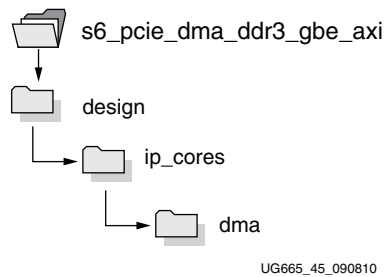


Figure 52: Packet DMA Design Files

## Multiport Virtual FIFO and Memory Controller Block

Figure 53 shows the design module for the multiport virtual FIFO and memory controller block. Figure 54 shows the design file structure.

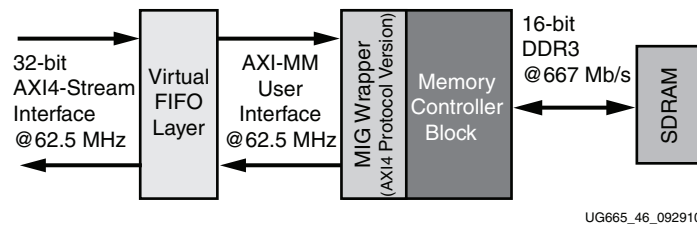


Figure 53: Multiport Virtual FIFO and Memory Controller Block Design Module

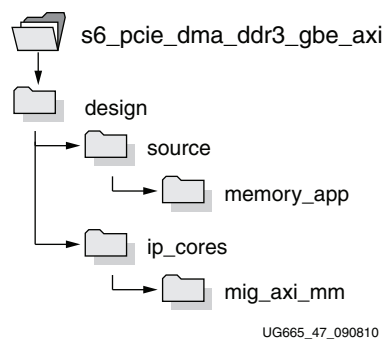


Figure 54: Multiport Virtual FIFO and Memory Controller Design Files

## Ethernet

Figure 55 shows the Ethernet design module.

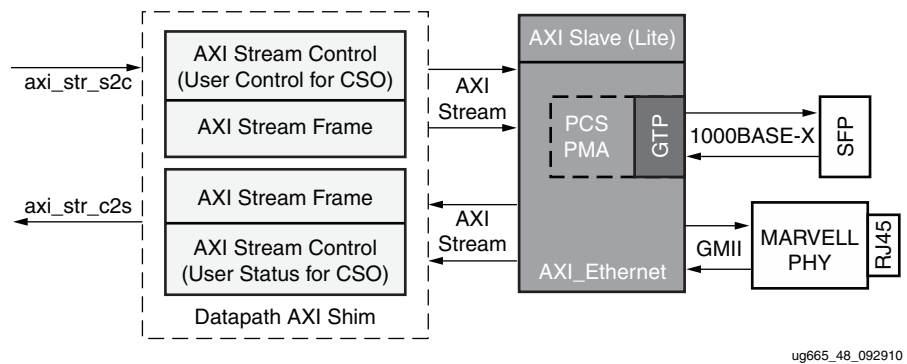


Figure 55: Ethernet Design Module

## Software Device Driver and Software Application/GUI Files and Scripts

Figure 56 shows the design module for the software device driver and the software application/GUI files and scripts. Figure 57 shows the design file structure for the software device driver and the software application and GUI.

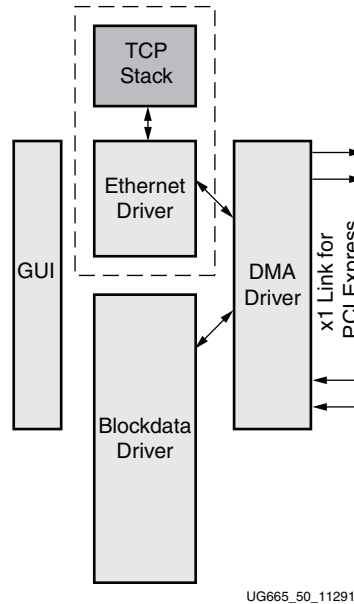


Figure 56: Software Device Driver and Software Application/GUI Design Module

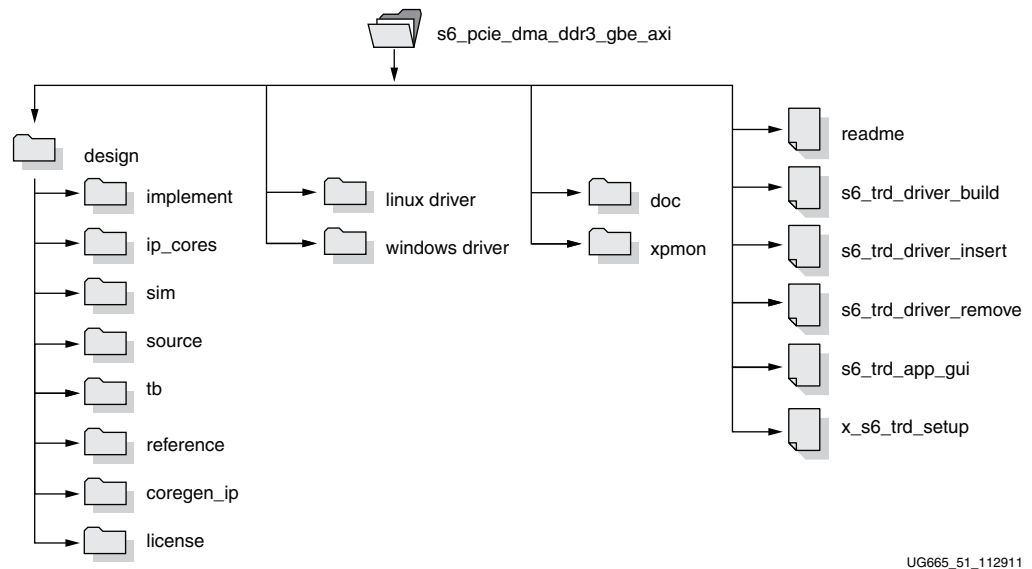


Figure 57: Software Device Driver and Software Application/GUI Files

## Simulating the Connectivity TRD

A complete simulation environment is provided with the Spartan-6 FPGA Connectivity TRD. For more details on the simulation environment and the associated simulation files, refer to the “Simulation” section in the “Getting Started” chapter in UG399, *Spartan-6*

*FPGA Connectivity Targeted Reference Design with AXI4 Protocol User Guide* for AXI4 protocol version, or [UG392](#), *Spartan-6 FPGA Connectivity Targeted Reference Design User Guide* for version without AXI4 protocol.

## Reusing the DMA IP from Northwest Logic

The Packet DMA Controller IP Core for PCI Express included in the Spartan-6 FPGA Connectivity Kit is a node-locked license of a full seat of a production netlist from Northwest Logic. This 32-bit DMA IP core is optimized for the Spartan-6 FPGA architecture and can be targeted to or reused in multiple projects for design using any Spartan-6 FPGA. The DMA controller design deliverables are:

- Simulation model
- Hardware evaluation netlist (time-limited to 12 hours)
- Production netlist files:
  - The license for the DMA Controller IP from Northwest Logic is a single-seat, node-locked license entitlement.
  - This entitlement to the full production netlist is fulfilled through the OMS licensing system. Customers receive an email upon kit purchase with specific instructions for downloading the license files associated with the product. The license file is a mandatory step to unlock these production netlist files.
  - The purchase of the Spartan-6 FPGA Connectivity Kit also entitles the customer to all associated updates of the DMA Controller IP for the lifetime of the Spartan-6 FPGA Connectivity Kit. When the Spartan-6 FPGA Connectivity Kit is obsolete, the customer must contact Northwest Logic directly to extend the licensing, maintenance, support, and upgrades for this DMA Controller IP.

For design modifications and/or additional licenses for the full production version of the Northwest Logic PCIe Packet DMA IP core, refer to <http://nwlogic.com/products/pci-express-solution/>.

## Modifications to the Connectivity TRD

The Spartan-6 FPGA Connectivity TRD is a framework for system designers to derive extensions or modify their designs. Additional possible design enhancements, modifications, and reconstructions with custom IPs and design blocks are described in the “Designing with the TRD Platform” chapter in UG399, *Spartan-6 FPGA Connectivity Targeted Reference Design with AXI4 Protocol User Guide* for AXI4 protocol version, or [UG392](#), *Spartan-6 FPGA Connectivity Targeted Reference Design User Guide* for version without AXI4 protocol.

## Getting Started with the Spartan-6 FPGA IBERT Reference Design

This Spartan-6 FPGA Connectivity Kit comes with an Integrated Bit Error Ratio Test (IBERT) reference design available on the CompactFlash. The demonstration shows the capabilities of the Spartan-6 LXT device using the GTP transceivers running at 2.5 Gb/s line rates.

The Spartan-6 FPGA IBERT reference design has these components:

- Spartan-6 FPGA GTP transceivers running at 2.5 Gb/s
- The IBERT v2.0 reference design available through the CORE Generator tool for IP delivery

The design also includes a pseudo-random bit sequence (PRBS) pattern generator and checker.

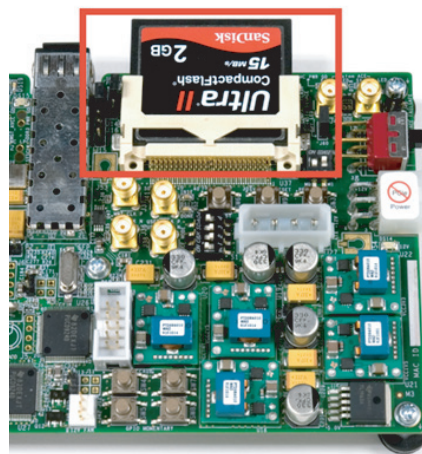
- All four GTP transceivers in the Spartan-6 FPGA LX45T are accessed through these channels in the IBERT reference design:
  - SFP
  - SMA
  - PCIe
  - FMC\_LPC (the transceiver is pinned out to the FMC-LPC connector)

**Note:** The demonstration is for an SMA external loopback scenario only.

## IBERT Hardware Demonstration Setup Instructions

This section describes how to set up the hardware for the IBERT reference design demonstration. The IBERT reference design is provided as an FPGA programming file on the CompactFlash.

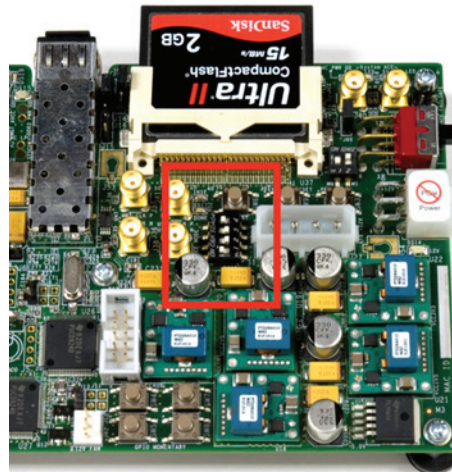
1. This equipment is needed to run the demonstration:
  - Spartan-6 FPGA Connectivity Kit
  - PC system with USB port
  - Monitor, keyboard, and mouse
  - ISE Design Suite installed on the PC system
2. Board Setup I – Install the CompactFlash on the SP605 board:  
Use the CompactFlash provided in the kit (see [Figure 58](#)).



UG665\_27\_120109

*Figure 58:* Installing the Included CompactFlash on the SP605 Board

3. Board Setup II – Configure DIP switch S1 settings to load the IBERT design from the CompactFlash (see Figure 59):
  - a. S1\_1: ON
  - b. S1\_2: OFF
  - c. S1\_3: OFF
  - d. S1\_4: ON



UG665\_28\_112909

*Figure 59:* **Configuring the FPGA with the IBERT Design from CompactFlash**

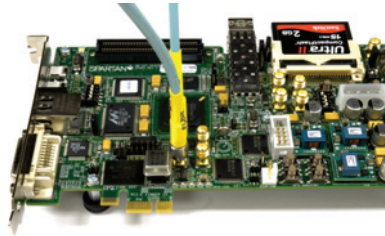
4. Board Setup III – Connect a USB cable to the SP605 board as shown in Figure 60:
  - a. Connect the included USB Type-A to Mini-B cable to the USB JTAG connector on the SP605 board.
  - b. Connect the other end of this cable to the PC system.



UG665\_29\_112909

*Figure 60:* **Connecting the USB Cable to the USB-JTAG Connector of the SP605 Board**

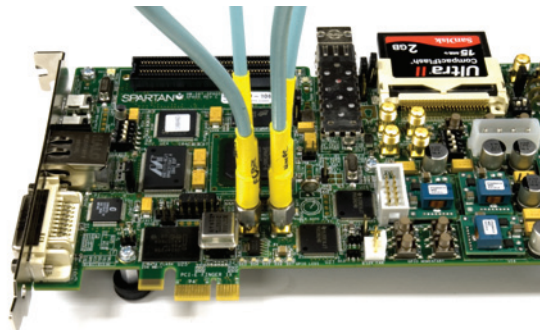
5. Board Setup IV – Use the SMA cables to loop back the transceiver channel pinned to the SMA:
  - a. Connect J32 to J34 (see [Figure 61](#)).



UG665\_30\_112909

*Figure 61:* **Configuring the SMA Transceiver Channel with External Loopback - I**

- b. Connect J33 to J35 (see [Figure 62](#)).

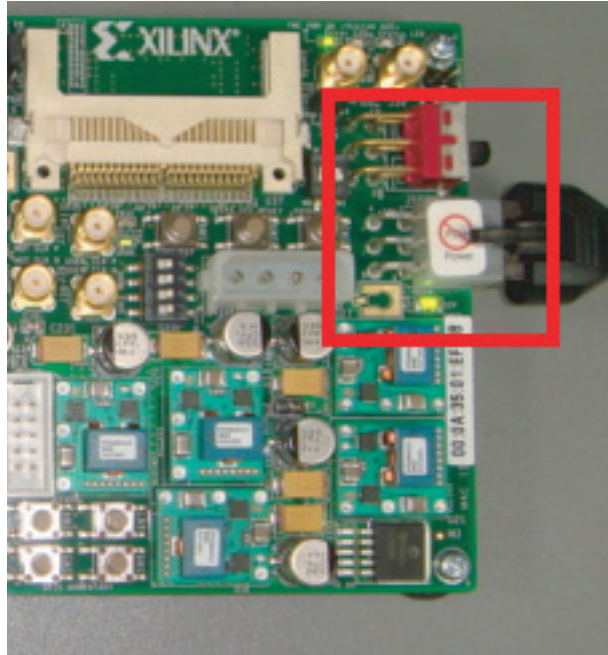


UG665\_31\_112909

*Figure 62:* **Configuring the SMA Transceiver Channel with External Loopback - II**



6. Board Setup V – Connect the power connector:
  - a. Using the included power supply, connect the power supply connector to the SP605 board as shown in Figure 63.
  - b. The power switch SW2 should be switched to the ON position.



UG665\_32\_121509

Figure 63: Powering Up the SP605 Board

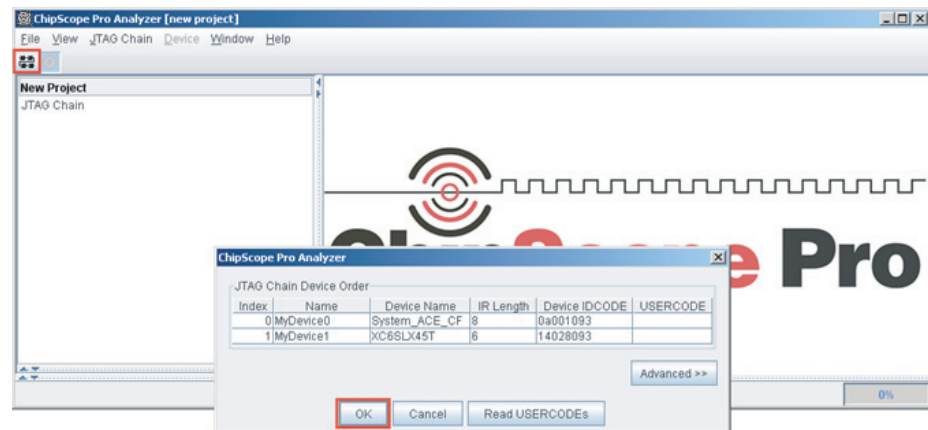
7. Board Setup VI – Load the FPGA with the IBERT design from the CompactFlash:
  - a. Press switch SW9 to configure from the CompactFlash.
  - b. Verify that the FPGA is loaded with the IBERT design. The DONE LED should be lit.



UG665\_33\_112909

Figure 64: FPGA Programmed with the IBERT Reference Design

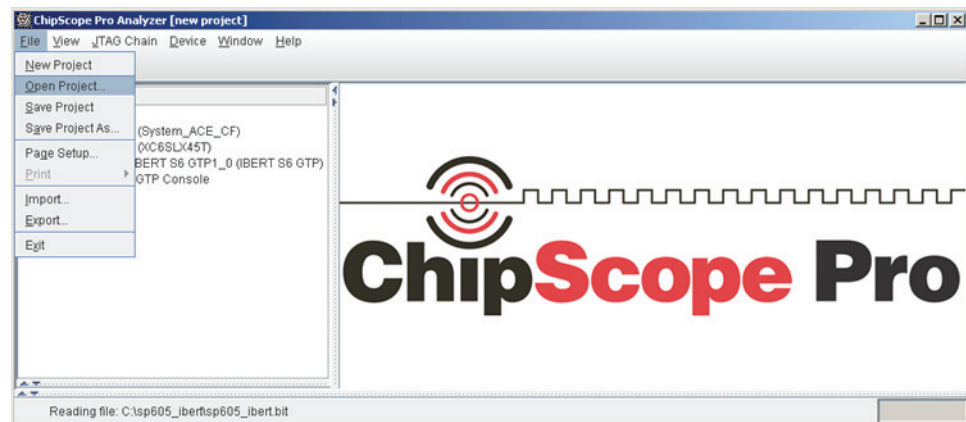
8. The IBERT Reference Design files are provided on a USB flash drive delivered as a part of the kit. Copy the contents of the included USB flash drive:
  - a. Insert the USB flash drive into a USB connector of the PC system.
  - b. Wait for the operating system to mount the USB flash. When the flash is mounted, an icon pops up on the desktop.
  - c. Navigate to the USB flash drive and copy the SP605\_Ibert\_Reference\_Design folder into a local directory.
  - d. Eject the USB flash drive.
9. Open the ChipScope Pro Analyzer window:
  - a. Click on **Programs** → **Xilinx ISE Design Suite** → **ChipScope Pro** → **Analyzer**.
  - b. Click on **Open Cable Button** as shown in [Figure 65](#).



UG665\_34\_120109

Figure 65: Launch the ChipScope Pro Analyzer Window

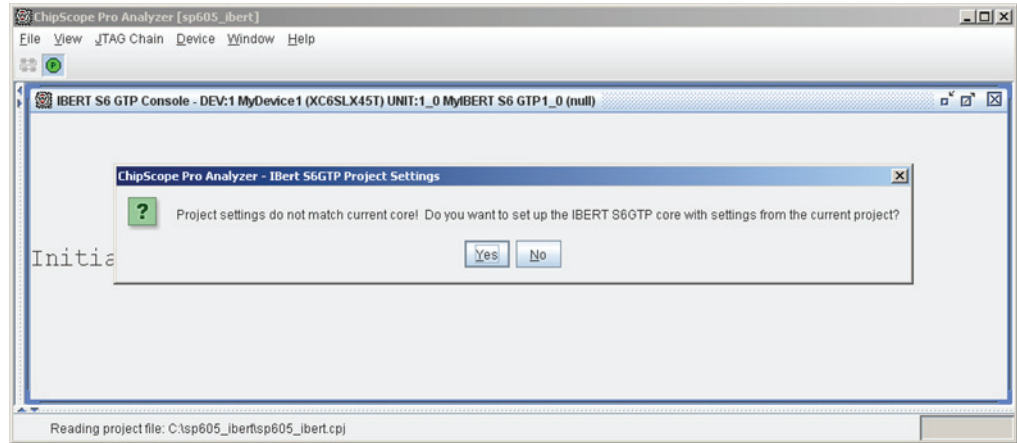
10. Open the ChipScope Pro analyzer project (see [Figure 66](#)):
  - a. Click **File** → **Open Project**.
  - b. Navigate to the SP605\_Ibert\_Reference\_Design folder.
  - c. Select **sp605\_ibert.cpj**.



UG665\_35\_112909

Figure 66: Open an Existing ChipScope Tool Project in the IBERT Design Package

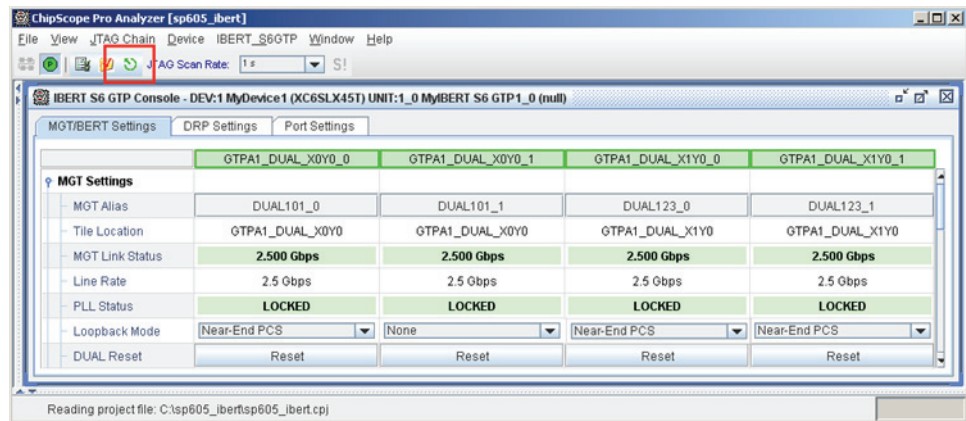
11. Load the ChipScope Pro analyzer project:
  - a. Click **Yes** on the dialog box shown in Figure 67.



UG665\_36\_112909

Figure 67: Load the ChipScope Tool Project and Communicate with the IBERT Reference Design

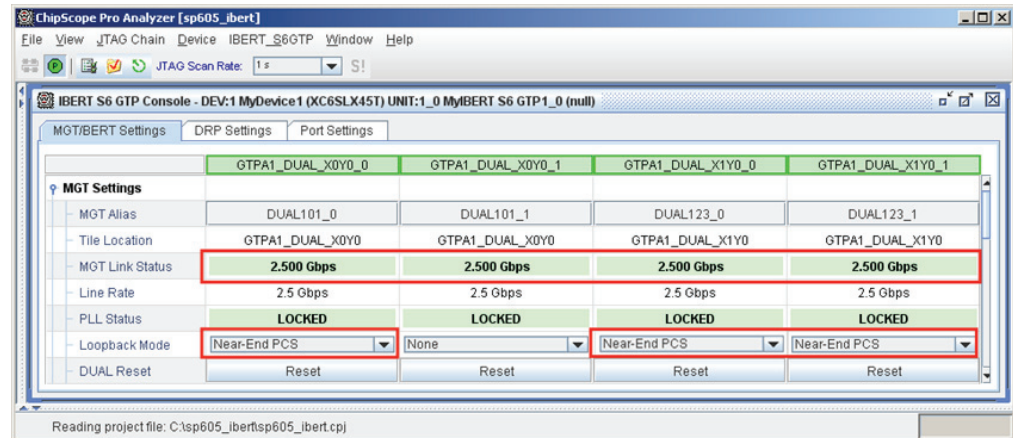
12. Load and reset the IBERT reference design through the GUI (see Figure 68).



UG665\_37\_112909

Figure 68: Load and Reset the IBERT Reference Design

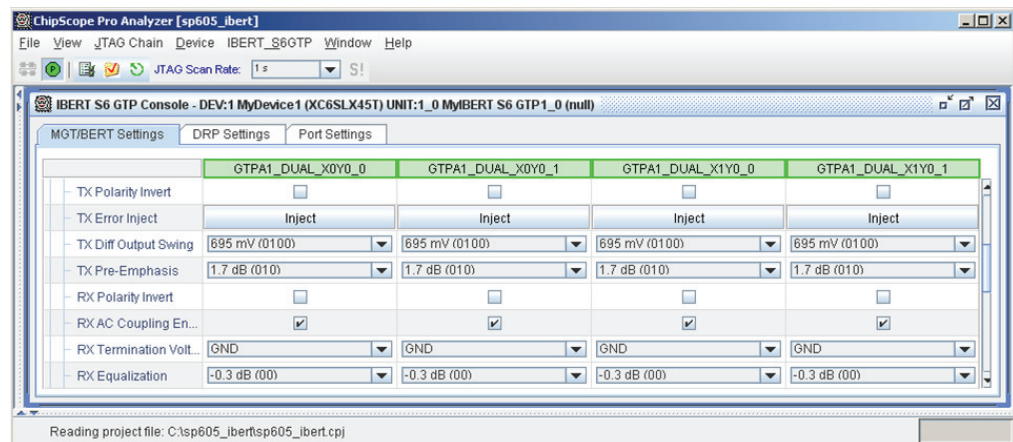
13. Verify the line rates for the GTP transceivers (see Figure 69):
  - a. The line rate is set to 2.5 Gb/s for all four GTP transceiver channels instantiated in the design.
  - b. Select **Near-End PCS** for these GTP transceiver channels: PCIe (GTPA1\_DUAL\_X0Y0\_0), FMC (GTPA1\_DUAL\_X1Y0\_0), and SFP (GTPA1\_DUAL\_X1Y0\_1).
  - c. The SMA transceiver channel (GTPA1\_DUAL\_X0Y0\_1) has been looped on external loopback. Select the loopback mode for the SMA transceiver channel as **None** (no internal loopback).



UG665\_38\_112909

Figure 69: Verify the GTP Transceiver Loopback Configuration and Link Status

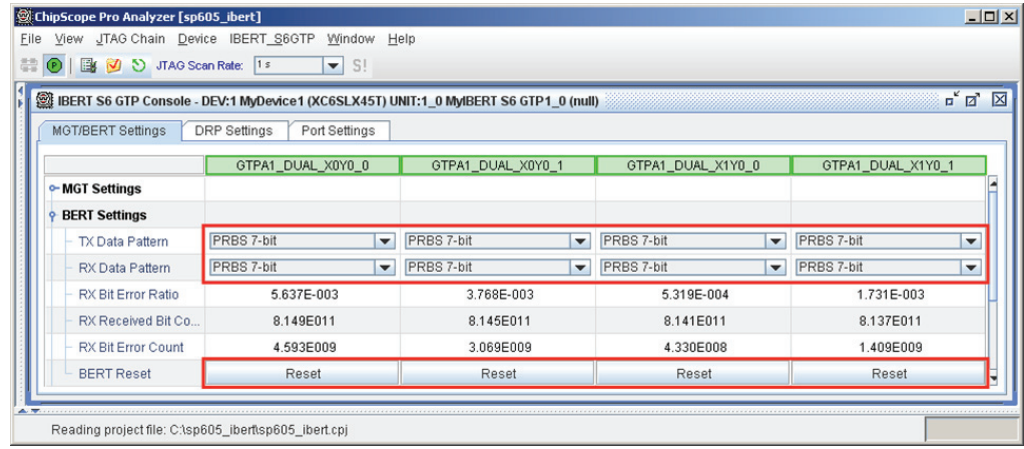
14. Configure the GTP transmit parameter settings (see Figure 70):
  - a. Set the *TX Diff Output Swing* parameter to 695 mV (0100).
  - b. Set the *TX Pre-Emphasis* parameter to 1.7 dB (010).



UG665\_39\_112909

Figure 70: Modifying the Transmitter Settings of the GTP Transceiver Channels

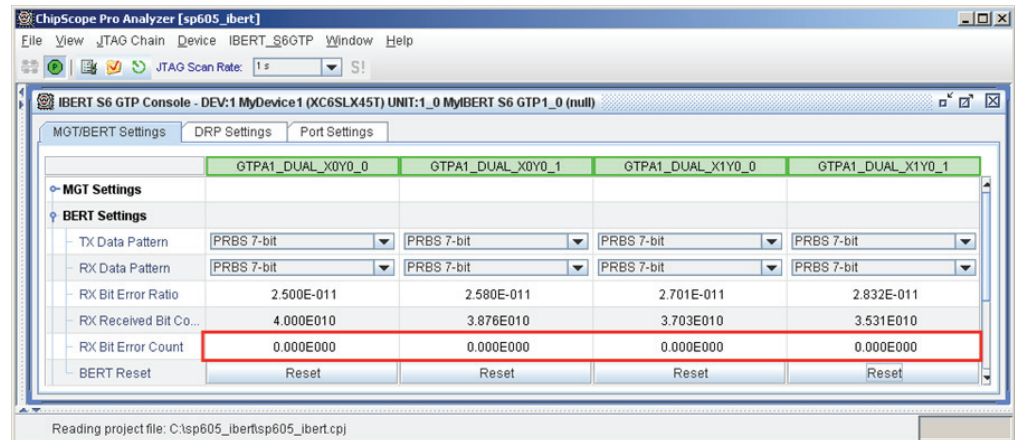
15. Configure the bit error ratio test (BERT) parameter settings (see Figure 71):
  - a. Set the TX/RX data patterns to PRBS 7-bit.
  - b. Click the BERT **Reset** buttons for each channel.



UG665\_40\_112909

Figure 71: Configuring the BERT Settings for the GTP Transceiver Channels

16. View the reported BERT (see Figure 72). The RX bit error count should be 0.



UG665\_41\_112909

Figure 72: Verify the Bit Error Ratio on All Four Transceiver Channels

Congratulations! The IBERT reference design for the Spartan-6 FPGA Connectivity Kit has been set up and the pre-built demo that uses the GTP transceivers running at 2.5 Gb/s has been tested.

For further details on other example reference designs available for the SP605 board, refer to <http://www.xilinx.com/sp605> and click on **SP605 Documentation**.

## Reference Design Files

The design checklist in [Table 2](#) includes simulation, implementation, and hardware details for the reference designs. After registration, reference design files are available for download at [ug665.zip](#).

Table 2: Design Checklist

Parameter	Description
<b>General</b>	
Developer Name	Xilinx
Target devices (stepping level, ES, production, speed grades)	XC6SLX45T-3-FGG484
Source code provided	Y (for custom logic only)
Source code format	Verilog
Design uses code or IP from an existing reference design or application note, third party, CORE Generator software	Uses code from a third party and LogiCORE IP from the CORE Generator software
<b>Simulation</b>	
Functional simulation performed	Y
Timing simulation performed	N
Testbench used for functional and timing simulations	Y (for functional simulations)
Testbench format	System Verilog (inhouse verification), Verilog (customer deliverable)
Simulator software/version used	ModelSim 6.4b
SPICE/IBIS simulations	N
<b>Implementation</b>	
Synthesis software tools/version used	XST
Implementation software tools/versions used	ISE 12.1 tool
Static timing analysis performed	Y
<b>Hardware Verification</b>	
Hardware verified	Y
Hardware platform used for verification	SP605 board

## Installation is Complete

The Xilinx design tools have been successfully installed, the CORE Generator tool flow for IP delivery is better understood, and the FPGA application is ready to be designed and implemented targeting the Spartan-6 LXT architecture.

For updated information on this Spartan-6 FPGA Connectivity Kit, go to <http://www.xilinx.com/s6connkit>. Check this page regularly for the latest in documentation, FAQs, reference design examples, product updates, and known issues.

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