ACPL-4800

High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

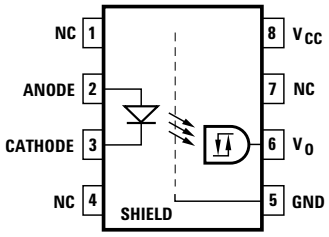
AVAGO TECHNOLOGIES

Datasheet

Description

The ACPL-4800 fast speed optocoupler contains a GaAsP LED and photo detector with built-in Schmitt trigger to provide logic-compatible waveforms, eliminating the need for additional wave shaping. The totem pole output eliminates the need for a pull up resistor and allows for direct drive Intelligent Power Module or gate drive.

Functional Diagram



TRUTH TABLE
(POSITIVE LOGIC)

LED	V_O
ON	HIGH
OFF	LOW

Note: The connection of a 0.1 μF bypass capacitor between pins 5 & 8 is recommended.

Features

- **Performance Specified for Fast IPM Applications over Industrial Temperature Range: -40°C to 100°C**
- **Wide Operating V_{CC} Range: 4.5 to 20 Volts**
- **Typical Propagation Delays 150 ns**
- **Minimized Pulse Width Distortion**
  PWD = 250 ns
- **Propagation Delay Difference**
  Min. –100 ns, Max. 250 ns
- **30 kV/μs Minimum Common Mode Transient Immunity at V_{CM} = 1000 V**
- **Hysteresis**
- **Totem Pole Output (No Pull-up Resistor Required)**
- **Safety Approval:**
  Pending for UL 1577, 3750 Vrms / 1 minute
  Pending for CSA File CA88324, Notice #5
  Pending for IEC/EN/DIN EN 60747-5-2, V_{IORM} = 630 Vpeak

Applications

- **IPM Interface Isolation**
- **Isolated IGBT/MOSFET Gate Drive**
- **AC and Brushless DC Servo Motor Drives**
- **Low Power Inverters**
- **General Digital Isolation**

Ordering Information

Specify Part Number followed by Option Number (if desired).

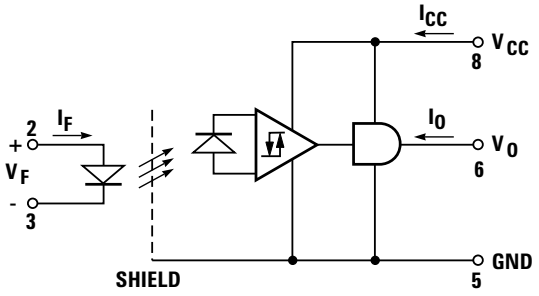
Example:

ACPL-4800-XXX

- 060 = IEC/EN/DIN EN 60747-5-2 Option
- 300 = Gull Wing Lead Option
- 500 = Tape and Reel Packaging Option
- XXXE = Lead-Free Option

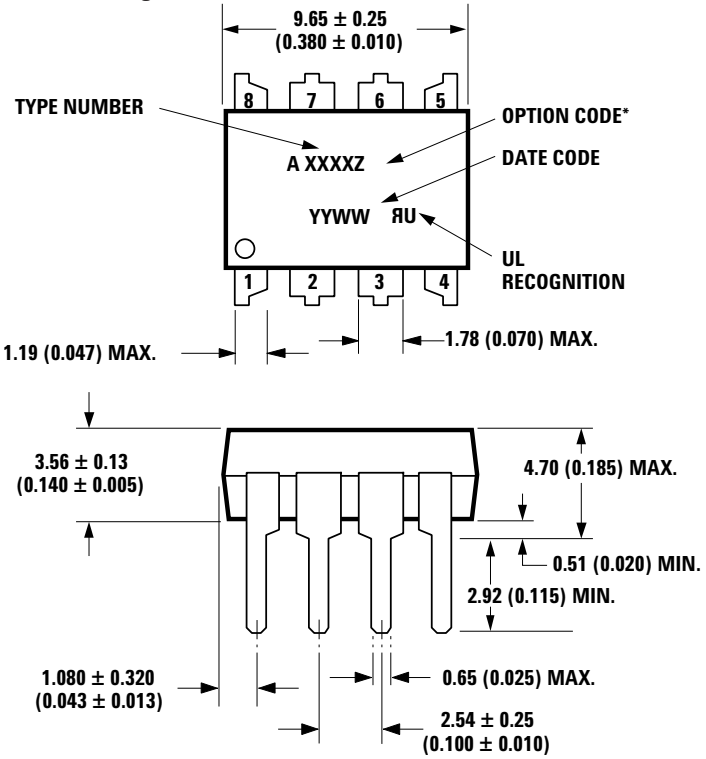
Option data sheets are available. Contact Avago sales representative or authorized distributor for information.

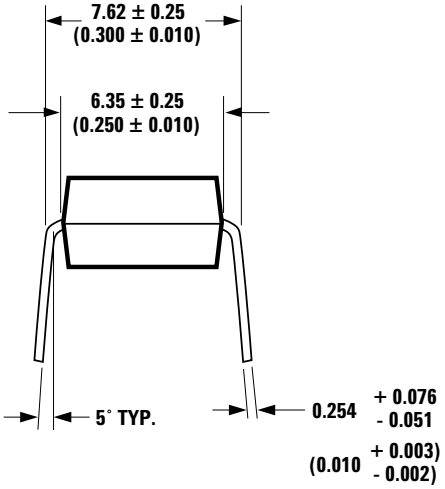
Schematic



Package Outline Drawings

DIP-8 Package

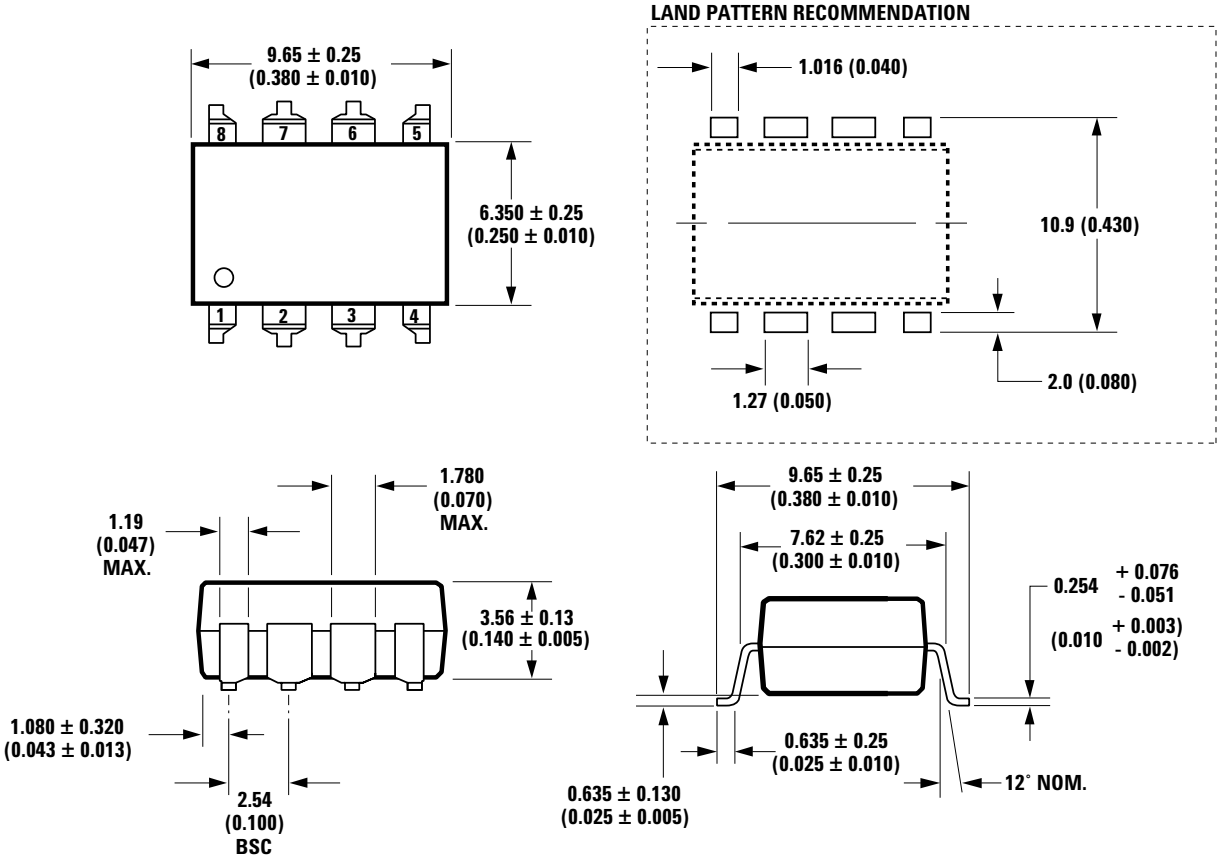




DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

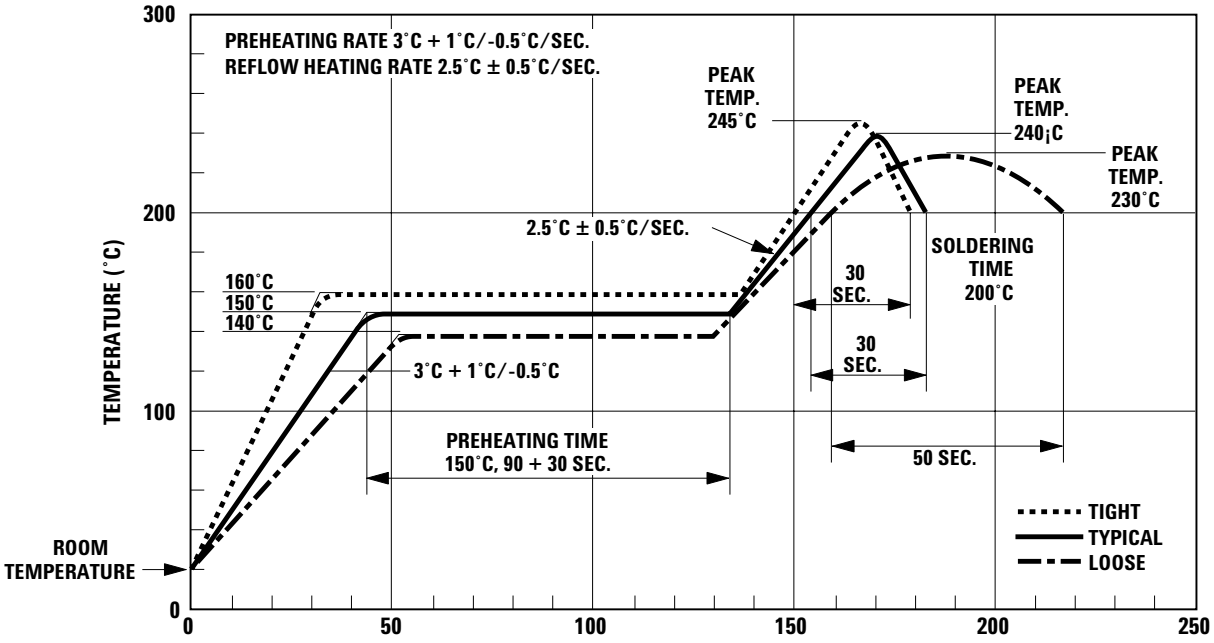
DIP-8 Package with Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

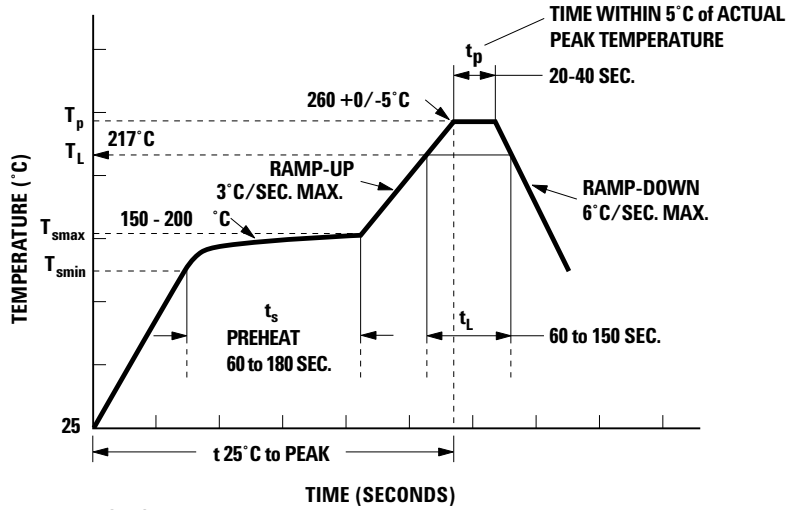
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile (Gull Wing Surface Mount Option 300 Parts)



Note: Use of non-chlorine-activated fluxes is highly recommended

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200˚C, T_{smin} = 150˚C

Table 2. Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08		Through insulation distance, conductor to conductor, usually the direct distance between the photo emitter and photo detector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	mm	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Table 3. IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (Option 060)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1			
for rated mains voltage ≤ 300 V_{rms}		I-IV	
for rated mains voltage ≤ 450 V_{rms}		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR},100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5=V_{PR}, Type and Sample Test, t_m=60 sec, Partial discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Over-voltage (Transient Over-voltage tini = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values - maximum values allowed in the event of a failure.			
Case Temperature	T_S	175	°C
Input Current	$I_{S, INPUT}$	230	mA
Output Power (refer to Thermal Derating Curve)	$P_{S, OUTPUT}$	600	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

Note:
Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.

Thermal Derating Curve

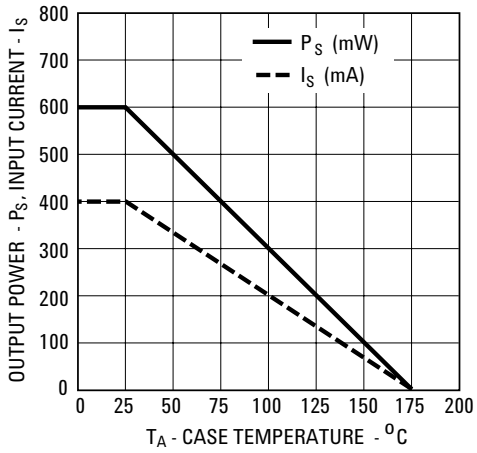


Table 4. Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Operating Temperature	T_A	-40	100	°C	
Average Forward Input Current	$I_{F(AVG)}$		10	mA	
Peak Transient Input Current	$I_{F(TRAN)}$				
(≤1 μs Pulse Width, 300 pps)			1.0	A	
(≤200 μs Pulse Width, < 1% Duty Cycle)			40	mA	
Reverse Input Voltage	V_R		5	V	
Average Output Current	I_O		25	mA	
Supply Voltage	V_{CC}	0	25	V	
Output Voltage	V_O	-0.5	25	V	
Total Package Power Dissipation	P_T		210	mW	1
Lead Solder Temperature (Through Hole Parts Only)	260 °C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile (Surface Mount Parts Only)	See Package Outline Drawings section				

Table 5. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	V
Forward Input Current (ON)	IF(ON)	6	10	mA
Forward Input Voltage (OFF)	VF(OFF)	-	0.8	V
Operating Temperature	T_A	-40	100	C

Table 6. Electrical Specification

$-40°C \le T_A \le 100°C$, $4.5V \le V_{CC} \le 20V$, $6mA \le I_{F(ON)} \le 10$ mA, $0V \le V_{F(OFF)} \le 0.8$ V, unless otherwise specified.
All Typicals at $T_A = 25°C$. See Note 7.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	I_{OL} = 6.4 mA		1,3	
Logic High Output Voltage	V_{OH}	2.4	V_{CC} - 1.1V		V	I_{OH} = -2.6 mA		2,3,7	
		2.7				I_{OH} = -0.4 mA			
Output Leakage Current (VOUT = VCC+0.5V)	I_{OHH}			100	μA	Vcc = 5 V	I_F = 10mA		
				500		Vcc = 20 V			
Logic Low Supply Current	I_{CCL}		1.9	3.0	mA	Vcc = 5.5 V	V_F = 0 V I_O = Open		
			2.0	3.0		Vcc = 20 V			
Logic High Supply Current	I_{CCH}		1.5	2.5	mA	Vcc = 5.5 V	I_F = 10 mA I_O = Open		
			1.6	2.5		Vcc = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	V_O = Vcc = 5.5 V	V_F=0V		2
		50				V_O = Vcc = 20 V			
Logic High Short Circuit Output Current	I_{OSH}			-25	mA	V_{CC} = 5.5 V	I_F=6mA V_O=GND		2
				-50		V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7	V	T_A = 25 C	I_F=6mA	4	
				1.85					
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 μA			
Input Diode Temperature Coefficient	DV_F DT_A		-1.7		mV/°C	I_F = 6 mA			
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, VF = 0 V			3

Table 7. Switching Specifications (AC)
$-40°C \le T_A \le 100°C$, $4.5V \le V_{CC} \le 20V$, $6mA \le I_{F(ON)} \le 10$ mA, $0V \le V_{F(OFF)} \le 0.8V$.
All Typicals at $T_A = 25°C$, $I_{F(ON)} = 6$ mA unless otherwise specified.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Leve	t_{PHL}		150	350	ns	With Peaking Capacitor	5,6	5
Propagation Delay Time to Logic High Output Level	t_{PLH}		110	350	ns	With Peaking Capacitor	5,6	5
Pulse Width Distortion	PWD			250	ns	$\lvert t_{PHL} - t_{PLH} \rvert$		8
Propagation Delay Difference Between Any 2 Parts	PDD	-100		250	ns			10
Output Rise Time (10-90%)	t_r		16		ns		5,8	
Output Fall Time (90-10%)	t_f		20		ns		5,8	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	-30000			V/µs	$\lvert V_{CM} \rvert$ = 1000 V, I_F = 6.0 mA, V_{CC} = 5 V, T_A = 25 C	9	6
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	30000			V/µs	$\lvert V_{CM} \rvert$ = 1000 V, V_F = 0 V, V_{CC} = 5 V, T_A = 25 C	9	6

Table 8.Package Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			Vrms	RH < 50%, t = 1 min. T_A = 25°C		4,7
Input-Output Resistance	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 Vdc		4
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 Vdc		4

Notes:
1. Derate total package power dissipation, P_T, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.
2. Duration of output short circuit time should not exceed 10 ms.
3. Input capacitance is measured between pin 2 and pin 3.
4. Device considered a two-terminal device: pins 1, 2, 3, and 4 shorted together and pins 5, 6, 7, and 8 shorted together.
5. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
6. CMH is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, $V_O > 2.0$ V. CML is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, $V_O < 0.8$ V.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ³ 4200 V rms for one second (leakage detection current limit, $I_{I-O} \le 5$ mA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
8. Pulse Width Distortion (PWD) is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
9. Use of a 0.1 µF bypass capacitor connected between pins 5 and 8 is recommended.
10. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition.

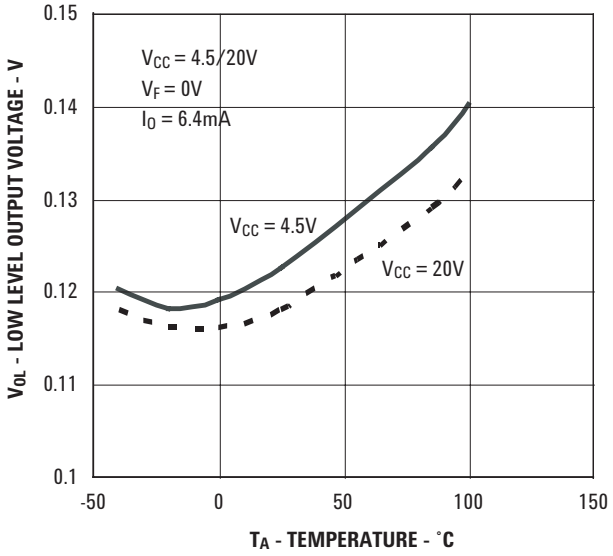


Figure 1. Typical Logic Low Output Voltage vs. Temputer

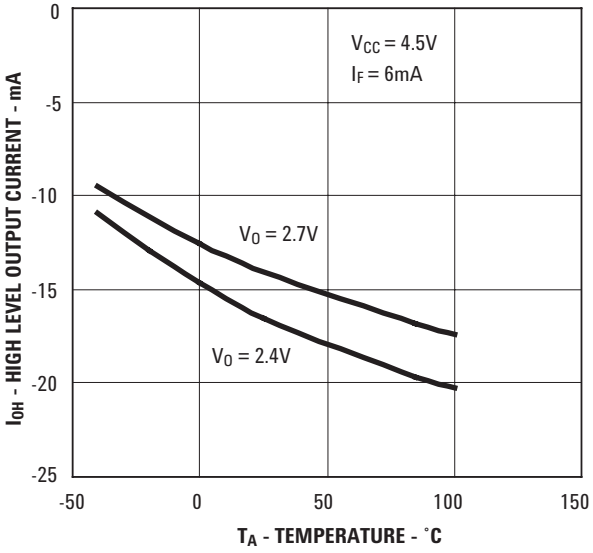


Figure 2. Typical Logic High Output Current vs. Temputer

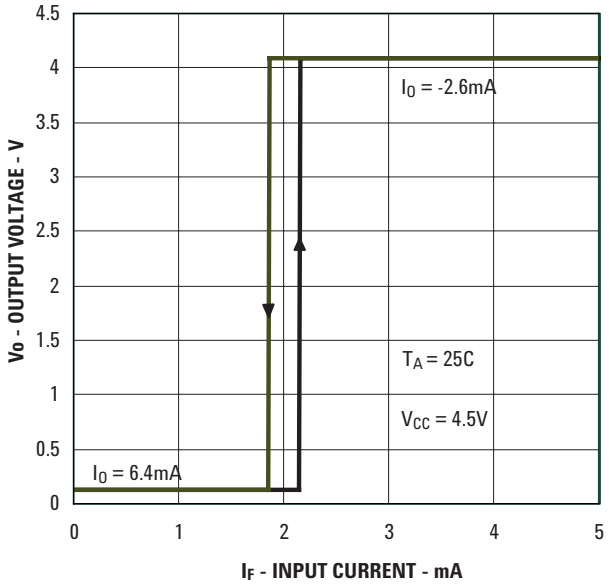


Figure 3. Typical Output Voltage vs. Forward Input Current

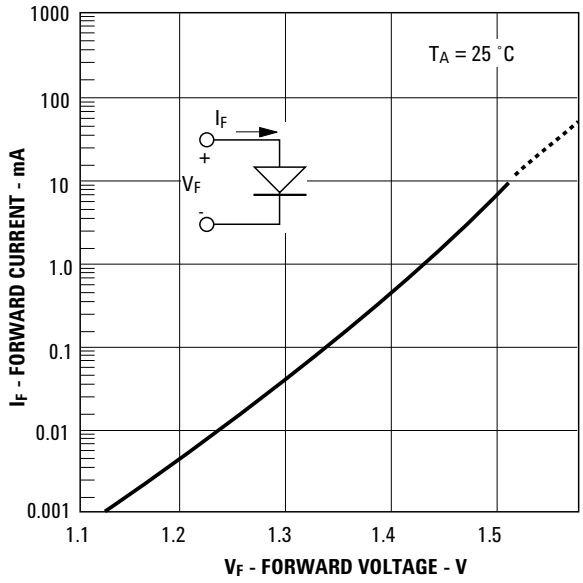
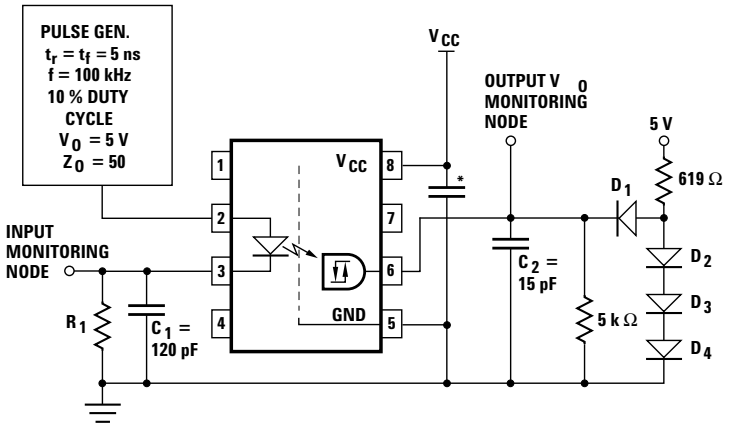


Figure 4. Typical Input Diode Forward Characteristic



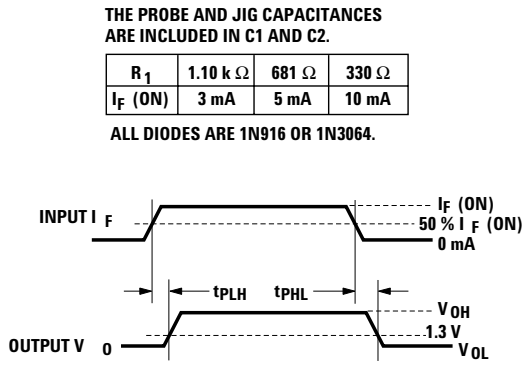


Figure 5. Circuit for t_{PLH},t_{PHL},t_r,t_f

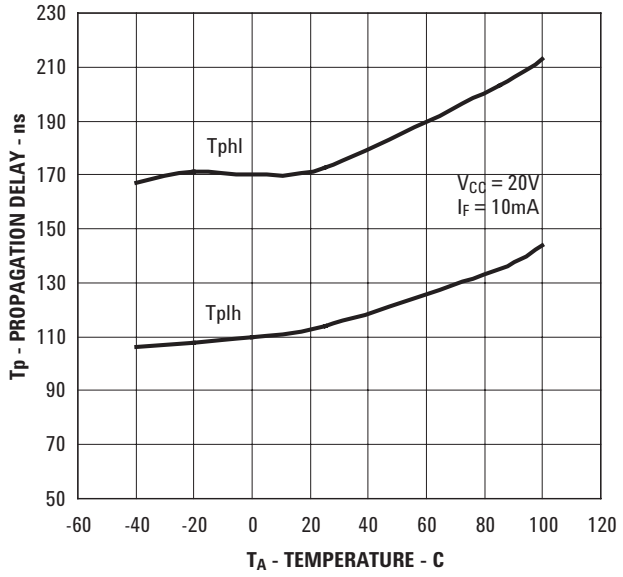


Figure 6. Typical Propagation Delays vs.Temperature.

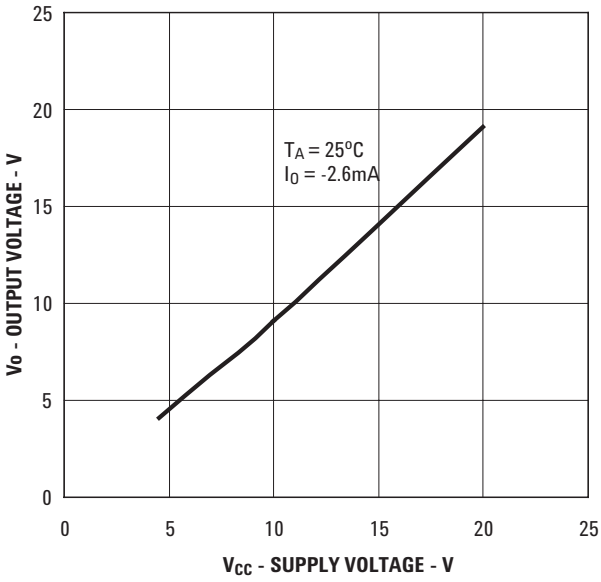


Figure 7. Typical Logic High Output Voltage vs. Supply Voltage

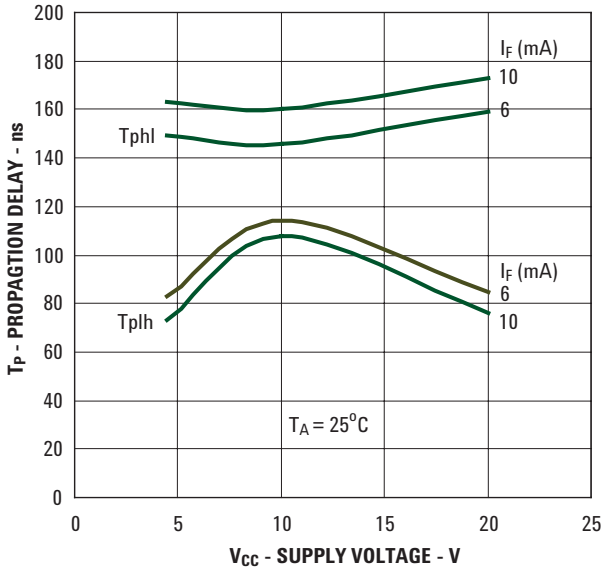
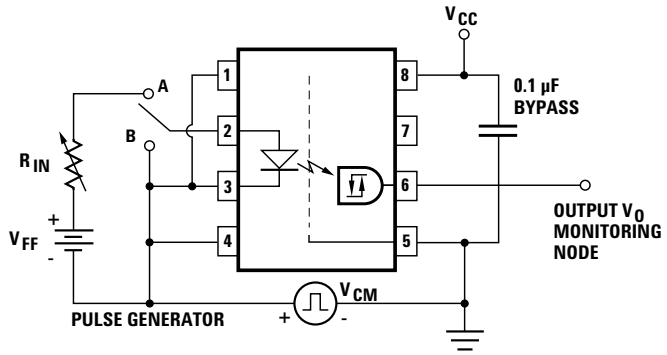


Figure 8. Typical Propogation Delats vs. Supply Voltage



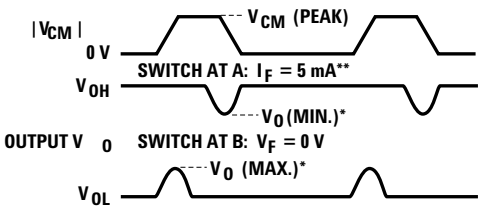


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

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