MCOT21605A1V-EGM	2 x 16	Euro/Jap/Cyrillic	OLED Module

Specification	
Version: 1	Date: 18/10/2017

Revision		
1	12/10/2017	First Issue.

Display Features	
Character Count	2 x 16
Appearance	Green on Black
Logic Voltage	5V
Interface	Parallel / SPI / I2C
Font Set	English / Japanese / Cyrillic
Character Height	5.57
Module Size	68.50 x 17.50 x 2.17 mm
Operating Temperature	-40°C ~ +70°C
Construction	TAB

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the SSD1311 specification.(Provided Separately)
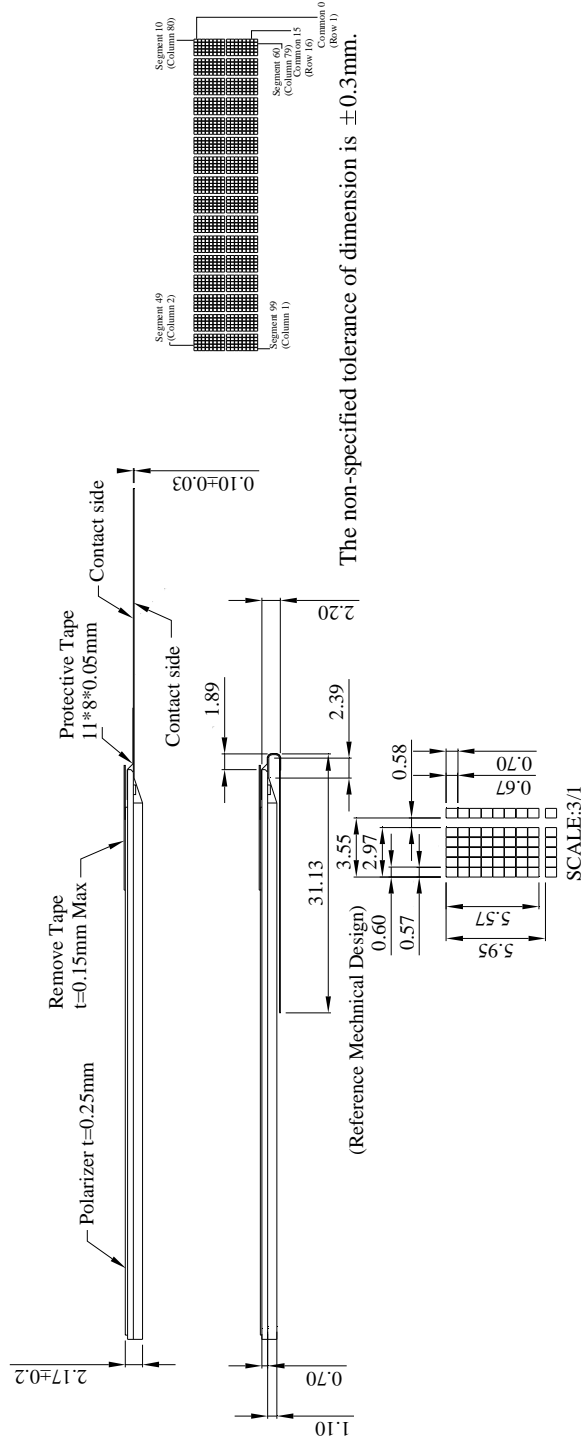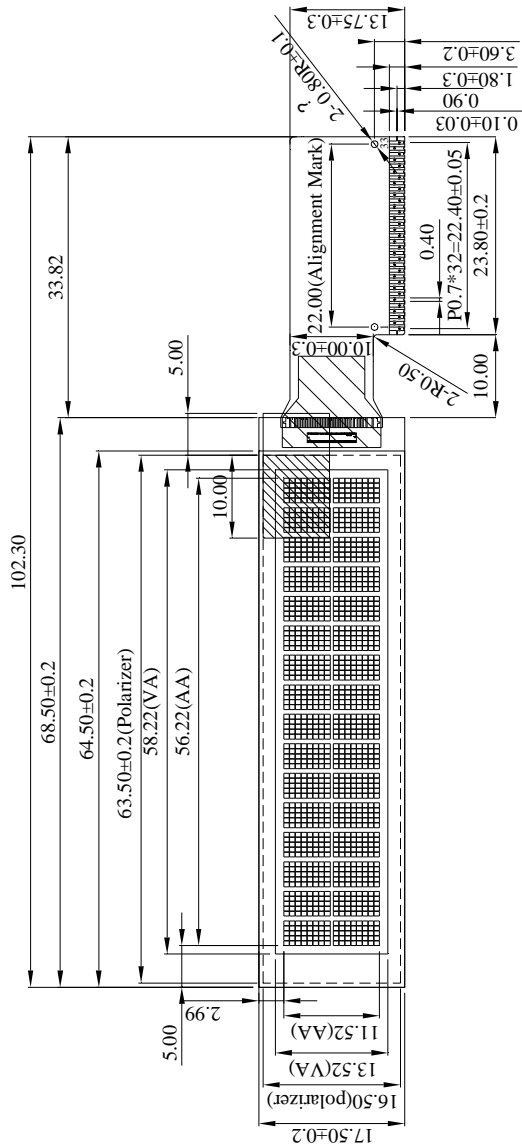
Display Accessories	
Part Number	Description
MPBV4-Iss2	Direct solder-to-2mm pitch DIL pinout interface board. Compatible with: 0.7, 0.8, 0.845 and 1mm pitch pads.
MCIB-13 V2	Direct solder OLED character interface board. Used in conjunction with MCIB-12 and UC32.

Optional Variants	
Appearance	Voltage
Blue on Black White on Black Red on Black Yellow on Black	
Interface	

Mechanical Specifications

Module Size	68.50 x 17.50 x 2.17 (Without Backlight)				W x H x D mm
Active Area	56.22 x 11.52	W x H mm	Hole-to-Hole	---	W x H mm
Character Size	2.96 x 5.57	W x H mm	Character Pitch	3.55 x 5.95	W x H mm
Dot Size	0.57 x 0.67	W x H mm	Dot Pitch	0.60 x 0.70	W x H mm

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	NC	18	D0
2	VSL	19	D1
3	VSS	20	D2
4	REGVDD	21	D3
5	SHLC	22	D4
	SHLS	23	D5
7	VDD	24	D6
8	VDDIO	25	D7
9	BS0	26	IREF
10	BS1	27	ROM0
11	BS2	28	ROM1
12	GPIO	29	OPR0
13	CS#	30	OPR1
14	RES#	31	VCOMH
15	D/C#	32	VCC
16	R/W#(WR#)	33	NC
17	E(RD#)		

The non-specified tolerance of dimension is ±0.3mm.

Segment 10 (Column 80)
Segment 60 (Column 79)
Common 15 (Row 16)
Common 0 (Row 1)
Segment 49 (Column 2)
Segment 99 (Column 1)

13.75±0.3
3.60±0.2
1.80±0.3
0.90
0.10±0.03
2-0.80R±0.1
33.82
5.00
22.00(Alignment Mark)
0.40
P0.7*32=22.40±0.05
23.80±0.2
10.00±0.3
2-R0.50
10.00
102.30
68.50±0.2
64.50±0.2
63.50±0.2(Polarizer)
58.22(VA)
56.22(AA)
10.00
2.99
5.00
11.52(AA)
13.52(VA)
16.50(polarizer)
17.50±0.2

Protective Tape 11*8*0.05mm
Contact side
Contact side
0.10±0.03
Remove Tape t=0.15mm Max
Polarizer t=0.25mm
2.17±0.2
0.70
1.10

1.89
2.39
2.20
31.13
3.55
2.97
0.60
0.57
(Reference Mechnical Design)
0.58
0.67
0.70
5.57
5.95
SCALE:3/1

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Block Diagram
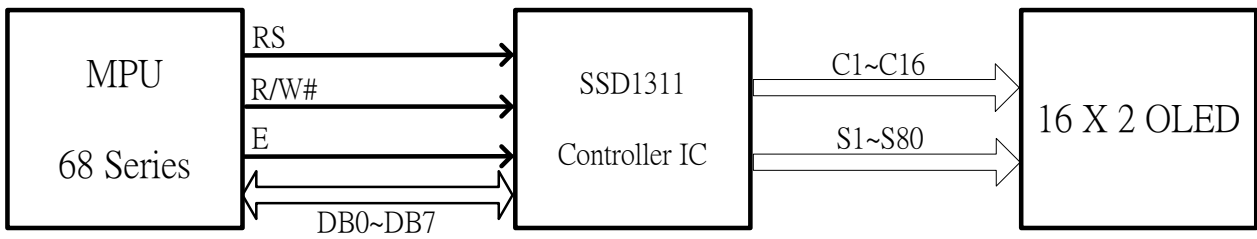
Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F

Pin Layout

Pin	Symbol	Description
1	NC	No connection
2	VSL	This is segment voltage (output low level) reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, connect with resistor and diode to ground (details depend on application).
3	VSS	Ground pin. It must be connected to external ground.
4	REGVDD	Internal VDD regulator selection pin in 5V I/O application mode. When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application). When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/O application).
5	SHLC	This pin is used to determine the Common output scanning direction. COM scan direction <table><tr><td>SHLC</td><td>COM scan direction</td></tr><tr><td>1</td><td>COM0 to COM31 (Normal)</td></tr><tr><td>0</td><td>COM31 to COM0 (Reverse)</td></tr></table>(1) 0 s connected to VSS (2) 1 s connected to VDDIO
6	SHLS	This pin is used to change the mapping between the display data column address and the Segment driver. SEG scan direction <table><tr><td>SHLS</td><td>SEG direction</td></tr><tr><td>1</td><td>SEG0 to SEG99 (Normal)</td></tr><tr><td>0</td><td>SEG99 to SEG0 (Reverse)</td></tr></table>(1) 0 s connected to VSS (2) 1 s connected to VDDIO
7	VDD	Power Supply For Core Logic Operation. VDD can be supplied externally or regulated internally. In LV IO application (internal VDD is disabled), this is a power input pin. In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO. A capacitor should be connected between VDD and VSS under all circumstances.
8	VDDIO	Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.
9	BS0	MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS2, BS1 and BS0 are pin select.
10	BS1	Bus Interface selection
11	BS2	<table><tr><td>BS[2:0]</td><td>Interface</td></tr><tr><td>000</td><td>Serial Interface</td></tr><tr><td>001</td><td>Invalid</td></tr><tr><td>010</td><td>I²C</td></tr><tr><td>011</td><td>Invalid</td></tr><tr><td>100</td><td>8-bit 6800 parallel</td></tr><tr><td>101</td><td>4-bit 6800 parallel</td></tr><tr><td>110</td><td>8-bit 8080 parallel</td></tr><tr><td>111</td><td>4-bit 8080 parallel</td></tr></table>(1) 0 s connected to VSS (2) 1 s connected to VDDIO
12	GPIO	GPIO pin. Details refer to OLED command DCh.
13	CS#	Chip Select Input Connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW). In I2C mode, this pin must be connected to VSS.
14	RES#	Reset Signal Input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation.

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15	D/C#	Data/Command Control Pin Connecting to the MCU. When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data. When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register. In I2C mode, this pin acts as SA0 for slave address selection. When serial interface is selected, this pin must be connected to VSS.
16	R/W#(WR#)	Read / Write Control Input Pin Connecting to the MCU interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
17	E(RD#)	MCU Interface Input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
18-25	D0~D7	Bi-directional Data Bus Connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
26	IREF	Segment Output Current Reference pin. IREF is supplied externally. A resistor should be connected between this pin and VSS to maintain current of around 15uA.
27	ROM0	These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table: Character ROM selection 	ROM1	ROM0	ROM
0	0	A
0	1	B
1	0	C
1	1	S/W selectable [3]	
28	ROM1	Note (1) 0 is connected to VSS (2) 1 is connected to VDDIO
29	OPR0	This pin is used to select the character number of character generator. Character RAM selection | OPR1	OPR0	CGROM	CGRAM
---	---	---	---
1	1	256	0
0	1	248	8
1	0	250	6
0	0	240	8	
30	OPR1	Note (1) 0 is connected to VSS (2) 1 is connected to VDDIO
31	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS. No external power supply can connect to this pin.
32	VCC	Power Supply for Panel Driving Voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
33	NC	No connection.

Font Map

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

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Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

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Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

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Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDDIO	---	-0.3	---	6.00	V
Operating Temperature	TOP	---	-40	---	70	°C
Storage Temperature	TST	---	-40	---	85	°C

Electronic Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Input High Voltage	VIH	---	0.80xVDD	---	---	V
Input Low Voltage	VIL	---	---	---	0.20xVDD	V
Output High Voltage	VOH	IOH=0.5mA	0.90xVDD	---	---	V
Output Low Voltage	VOL	IOL=0.5mA	---	---	0.10xVDD	V
Supply Voltage for Logic	VDDIO	---	4.80	5.00	5.30	V
Supply Voltage for Display	VCC	---	11.50	12.00	12.50	V
50% Checkboard Operating Current.	IDD	VCC=12V	14	16	18	mA
CIEx(Green)	---	(CIE1931)	0.24	0.28	0.32	---
CIEy(Green)	---	(CIE1931)	0.59	0.63	0.67	---

OLED Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Viewing Angle	(V)θ	---	160	---	---	Deg
	(H)φ	---	160	---	---	Deg
Contrast Ratio	CR	Dark	2000:1	---	---	---
Response Time	T Rise	---	---	10	---	µs
	T Fall	---	---	10	---	µs
Display with 50% Checkboard Brightness			90	110	---	cd/m^2

OLED Life Time

Item	Conditions	Typical	Remark
Operating Life Time	Ta=25°C. Initial checkboard brightness. 50%. 100cd/m2	50,000 Hours	---

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