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MCOT42005A1V-EWM	4 x 20	Euro/Jap/Cyrillic	OLED Module

Specification

Version: 3	Date: 10/10/2017

Revision

1	21/03/2016	First Issue.
2	01/06/2016	Modify Static Electricity Test.
3	21/09/2017	Modify Reliablity Test Condition.

Display Features	
Character Count	4 x 20
Appearance	White on Black
Logic Voltage	5V
Interface	Parallel / SPI / I2C
Font Set	English / Japanese / Cyrillic
Character Height	4.77
Module Size	84.50 x 27.50 x 2.05 mm
Operating Temperature	-40°C ~ +70°C
Construction	TAB

RoHS compliant

Box Quantity	Weight / Display
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* - For full design functionality, please use this specification in conjunction with the SSD1311 specification.(Provided Separately)

Display Accessories

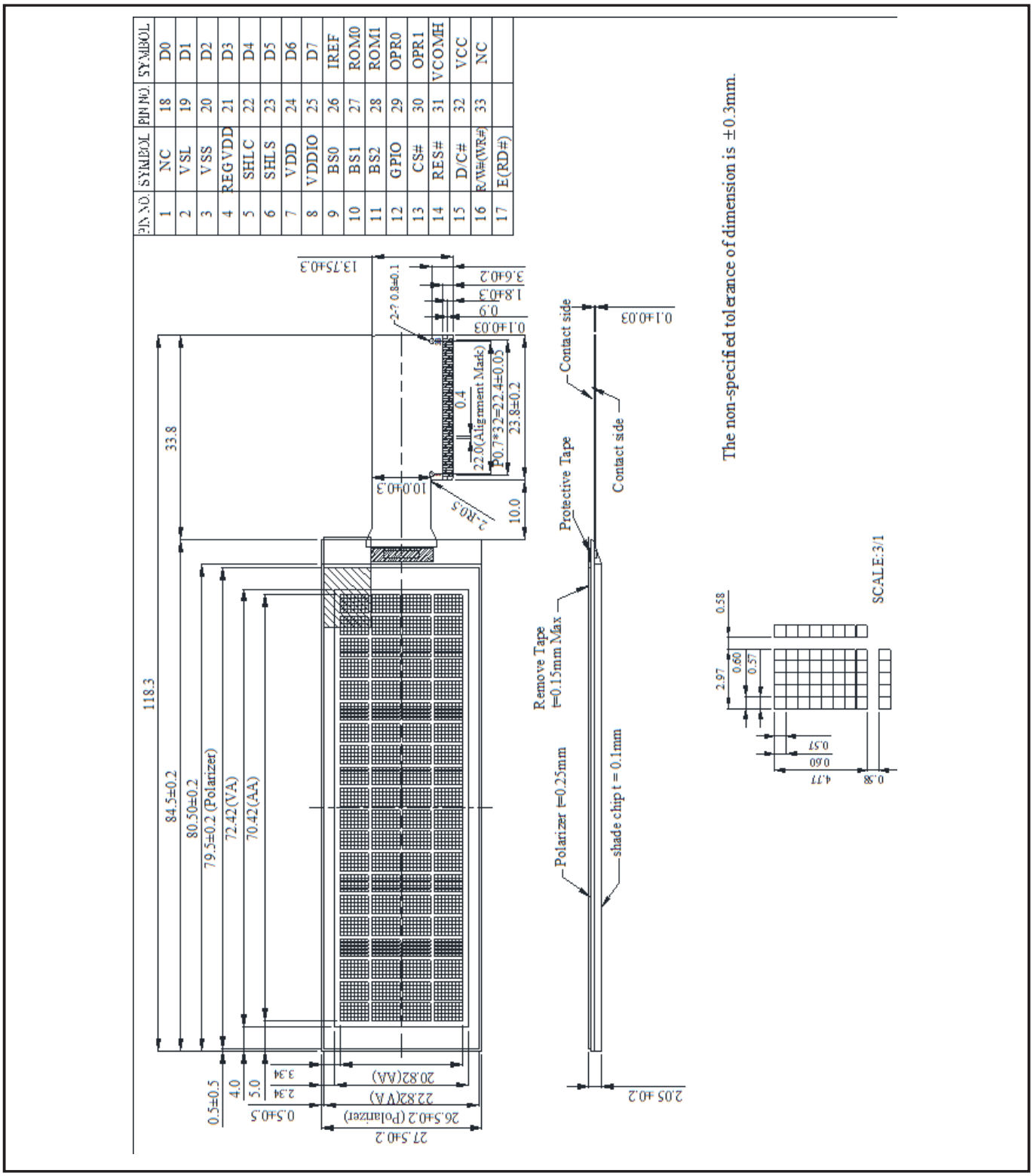
Part Number	Description
MPBV4-Iss2	Direct solder-to-2mm pitch DIL pinout interface board. Compatible with: 0.7, 0.8, 0.845 and 1mm pitch pads.
MCIB-13 V2	Direct solder OLED character interface board. Used in conjunction with MCIB-12 and UC32.

Optional Variants

Appearance	Voltage
Green on Black Yellow on Black	

Interface

Mechanical Specifications					
Module Size	84.50 x 27.50 x 2.05 (Without Backlight)				W x H x D mm
Active Area	70.42 x 20.82	W x H mm	Hole-to-Hole	---	W x H mm
Character Size	2.97 x 4.77	W x H mm	Character Pitch	3.55 x 5.35	W x H mm
Dot Size	0.57 x 0.57	W x H mm	Dot Pitch	0.60 x 0.60	W x H mm



MCOT42005A1V-EWM	4 x 20	Euro/Jap/Cyrillic	OLED Module
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Version: 3		Date: 10/10/2017	
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Block Diagram

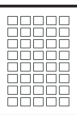
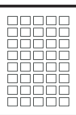
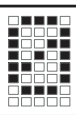
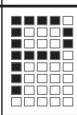
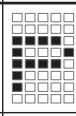
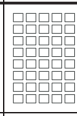
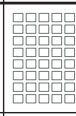
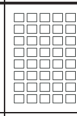
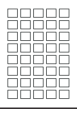
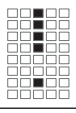
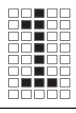
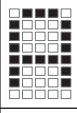
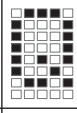
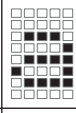
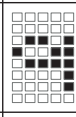
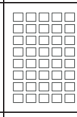
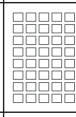
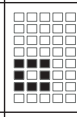
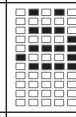
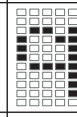
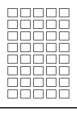
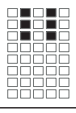
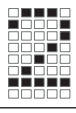
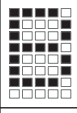
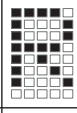
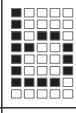
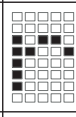
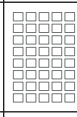
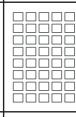
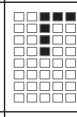
Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
DD RAM Address	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33
DD RAM Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
DD RAM Address	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73

Pin Layout

<table>
<tr><th>Pin</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>NC</td><td>No connection</td></tr>
<tr><td>2</td><td>VSL</td><td>This is segment voltage (output low level) reference pin.
When external VSL is not used, this pin should be left open.
When external VSL is used, connect with resistor and diode to ground (details depend on application).</td></tr>
<tr><td>3</td><td>VSS</td><td>Ground pin. It must be connected to external ground.</td></tr>
<tr><td>4</td><td>REGVDD</td><td>Internal VDD regulator selection pin in 5V I/O application mode.
When this pin is pulled HIGH, internal VDD regulator is enabled (5V I/O application).
When this pin is pulled LOW, internal VDD regulator is disabled (Low voltage I/O application).</td></tr>
<tr><td>5</td><td>SHLC</td><td>This pin is used to determine the Common output scanning direction.
COM scan direction
<table>
<tr><td>SHLC</td><td>COM scan direction</td></tr>
<tr><td>1</td><td>COM0 to COM31 (Normal)</td></tr>
<tr><td>0</td><td>COM31 to COM0 (Reverse)</td></tr>
</table>
(1) 0 s connected to VSS
(2) 1 s connected to VDDIO</td></tr>
<tr><td>6</td><td>SHLS</td><td>This pin is used to change the mapping between the display data column address and the Segment driver.
SEG scan direction
<table>
<tr><td>SHLS</td><td>SEG direction</td></tr>
<tr><td>1</td><td>SEG0 to SEG99 (Normal)</td></tr>
<tr><td>0</td><td>SEG99 to SEG0 (Reverse)</td></tr>
</table>
(1) 0 s connected to VSS
(2) 1 s connected to VDDIO</td></tr>
<tr><td>7</td><td>VDD</td><td>Power Supply For Core Logic Operation.
VDD can be supplied externally or regulated internally.
In LV IO application (internal VDD is disabled), this is a power input pin.
In 5V IO application (internal VDD is enabled), VDD is regulated internally from VDDIO.
A capacitor should be connected between VDD and VSS under all circumstances.</td></tr>
<tr><td>8</td><td>VDDIO</td><td>Low voltage power supply and power supply for interface logic level in both Low Voltage I/O and 5V I/O application. It should match with the MCU interface voltage level and must be connected to external source.</td></tr>
<tr><td>9</td><td>BS0</td><td rowspan="3">MCU bus interface selection pins. Select appropriate logic setting as described in the following table.
BS2, BS1 and BS0 are pin select.
Bus Interface selection
<table>
<tr><td>BS[2:0]</td><td>Interface</td></tr>
<tr><td>000</td><td>Serial Interface</td></tr>
<tr><td>001</td><td>Invalid</td></tr>
<tr><td>010</td><td>I²C</td></tr>
<tr><td>011</td><td>Invalid</td></tr>
<tr><td>100</td><td>8-bit 6800 parallel</td></tr>
<tr><td>101</td><td>4-bit 6800 parallel</td></tr>
<tr><td>110</td><td>8-bit 8080 parallel</td></tr>
<tr><td>111</td><td>4-bit 8080 parallel</td></tr>
</table>
(1) 0 s connected to VSS
(2) 1 s connected to VDDIO</td></tr>
<tr><td>10</td><td>BS1</td></tr>
<tr><td>11</td><td>BS2</td></tr>
<tr><td>12</td><td>GPIO</td><td>GPIO pin. Details refer to OLED command DCh.</td></tr>
<tr><td>13</td><td>CS#</td><td>Chip Select Input Connecting to the MCU.
The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
In I2C mode, this pin must be connected to VSS.</td></tr>
<tr><td>14</td><td>RES#</td><td>Reset Signal Input.
When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
</table>

<table>
<tr><td>15</td><td>D/C#</td><td>Data/Command Control Pin Connecting to the MCU.
When the pin is pulled HIGH, the data at D[7:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[7:0] will be transferred to a command register.
In I2C mode, this pin acts as SA0 for slave address selection.
When serial interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>16</td><td>R/W#(WR#)</td><td>Read / Write Control Input Pin Connecting to the MCU interface.
When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input.
Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.
When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>17</td><td>E(RD#)</td><td>MCU Interface Input.
When 6800 interface mode is selected, this pin will be used as the Enable (E) signal.
Read/write operation is initiated when this pin is pulled HIGH and the chip is selected.
When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected.
When serial or I2C interface is selected, this pin must be connected to VSS.</td></tr>
<tr><td>18-25</td><td>D0~D7</td><td>Bi-directional Data Bus Connecting to the MCU data bus.
Unused pins are recommended to tie LOW.
When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SID and D2 will be the serial data output: SOD.
When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.</td></tr>
<tr><td>26</td><td>IREF</td><td>Segment Output Current Reference pin.
IREF is supplied externally.
A resistor should be connected between this pin and VSS to maintain current of around 15uA.</td></tr>
<tr><td>27</td><td>ROM0</td><td rowspan="2">These pins are used to select Character ROM; select appropriate logic setting as described in the following table. ROM1 and ROM0 are pin select as shown in below table:
Character ROM selection
<table>
<tr><th>ROM1</th><th>ROM0</th><th>ROM</th></tr>
<tr><td>0</td><td>0</td><td>A</td></tr>
<tr><td>0</td><td>1</td><td>B</td></tr>
<tr><td>1</td><td>0</td><td>C</td></tr>
<tr><td>1</td><td>1</td><td>S/W selectable (3)</td></tr>
</table>
Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>28</td><td>ROM1</td></tr>
<tr><td>29</td><td>OPR0</td><td rowspan="2">This pin is used to select the character number of character generator.
Character RAM selection
<table>
<tr><th>OPR1</th><th>OPR0</th><th>CGROM</th><th>CGRAM</th></tr>
<tr><td>1</td><td>1</td><td>256</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>248</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>250</td><td>6</td></tr>
<tr><td>0</td><td>0</td><td>240</td><td>8</td></tr>
</table>
Note
(1) 0 is connected to VSS
(2) 1 is connected to VDDIO</td></tr>
<tr><td>30</td><td>OPR1</td></tr>
<tr><td>31</td><td>VCOMH</td><td>COM signal deselected voltage level.
A capacitor should be connected between this pin and VSS.
No external power supply can connect to this pin.</td></tr>
<tr><td>32</td><td>VCC</td><td>Power Supply for Panel Driving Voltage.
This is also the most positive power voltage supply pin. It is supplied by external high voltage source.</td></tr>
<tr><td>33</td><td>NC</td><td>No connection.</td></tr>
</table>

Font Map

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

MCOT42005A1V-EWM	4 x 20	Euro/Jap/Cyrillic	OLED Module
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Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

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Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

MCOT42005A1V-EWM	4 x 20	Euro/Jap/Cyrillic	OLED Module
Specification			
Version: 3	Date: 10/10/2017		
Revision			

Absolute Maximum Ratings

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage for Logic	VDDIO	---	-0.3	---	6.00	V
Input Voltage	VI	---	-0.3	---	VDD	°C
Operating Temperature	TOP	---	-40	---	70	°C
Storage Temperature	TST	---	-40	---	85	°C

Electronic Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Input High Voltage	VIH	---	0.80xVDD	---	---	V
Input Low Voltage	VIL	---	---	---	0.20xVDD	V
Output High Voltage	VOH	IOH=0.5mA	0.90xVDD	---	---	V
Output Low Voltage	VOL	IOL=0.5mA	---	---	0.10xVDD	V
Supply Voltage for Logic	VDD/VSS	---	4.80	5.00	5.30	V
Supply Voltage for Display	VCC	---	11.00	12.00	13.00	V
50% Checkboard Operating Current.	ICC	VCC=12V	22	23	25	mA
CIEx(White)	---	(CIE1931)	0.26	0.28	0.30	---
CIEy(White)	---	(CIE1931)	0.30	0.32	0.34	---

OLED Characteristics

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit
Viewing Angle	(V)θ	---	160	---	---	Deg
	(H)φ	---	160	---	---	Deg
Contrast Ratio	CR	Dark	2000:1	---	---	---
Response Time	T Rise	---	---	10	---	μs
	T Fall	---	---	10	---	μs
Display with 50% Checkboard Brightness			100	120	---	cd/m^2

OLED Life Time

Item	Conditions	Typical	Remark
Operating Life Time	Ta=25°C. Initial checkboard brightness. 50%.	50,000 Hours	---