General Description
The MAX77816 is a high-current, high-efficiency buck-boost regulator targeting single-cell Li-ion battery-powered applications. It supports a wide output voltage range from 2.60V to 5.14V. The IC allows 5A (TYP) maximum switch current. In buck mode, the output current can go as high as 4A, and in boost mode, the maximum output current can be 3A. A unique control algorithm allows high efficiency, outstanding line/load transient response, and seamless transition between buck and boost modes.

The IC features I²C-compatible serial interface. The I²C interface allows the output voltage to be dynamically adjusted thus enabling finer control of system power consumption. The I²C interface also provides features such as enable control and device status monitoring.

The multifunction GPIO pin is register settable to 5 different options such as FPWM mode enable and inductor peak current level selection. These options provide design flexibility that allows the IC to cover a wide range of applications and use cases.

Applications
● Smartphones and Tablets
● Wearable Devices
● Wireless Communication Devices
● RF Power Amplifiers
● Battery-Powered Applications

Benefits and Features
● Buck and Boost Operation Including Seamless Transition between Buck and Boost Modes
  • 2.3V to 5.5V VIN Range
  • 2.60V to 5.14V VOUT with 20mV Step
  • 3A Minimum Continuous Output Current (VINBB ≥ 3.0V, VOUTBB = 3.3V)
  • Burst Current: 3.6A Minimum Output Current for 800µs (VINBB ≥ 3.0V, VOUTBB = 3.3V)
● I²C Serial Interface Allows Dynamic VOUT Adjustment and Provides Design Flexibility
● 97.5% Peak Efficiency
● 40µA Quiescent Current
● Safety Features Enhance Device and System Reliability
  • Soft-Start
  • True Shutdown™
  • Thermal Shutdown and Short-Circuit Protection
● Multifunction GPIO Pin
  • MAX77816A: FPWM Mode Enable
  • MAX77816B: Inductor Peak Current-Limit selection
  • MAX77816C: Output Voltage Selection
  • MAX77816D: Power-OK indicator
  • MAX77816E: Interrupt Indicator
● Small Size: 1.827mm x 2.127mm, 20-Bump WLP, 0.4mm Pitch

Typical Application Circuit

Ordering Information appears at end of data sheet.

True Shutdown is a trademark of Maxim Integrated Products, Inc.
MAX77816

High-Efficiency Buck-Boost Regulator
with 5A Switches

Absolute Maximum Ratings

SYS to GND .......................................................... -0.3V to +6.0V
INBB, OUTBB to PGNDBB ............................................. -0.3V to +6.0V
PGNDBB to GND .................................................. -0.3V to +0.3V
SCL, SDA to GND .................................................. -0.3V to (V_SYS + 0.3V)
EN, GPIO to GND .................................................. -0.3V to (V_SYS + 0.3V)
FB_BB to GND .................................................. -0.3V to (V_OUTBB + 0.3V)
LXBB1 to PGNDBB .............................................. -0.3V to (V_INBB + 0.3V)
LXBB2 to PGNDBB .............................................. -0.3V to (V_OUTBB + 0.3V)

LXBB1/LXBB2 Continuous RMS Current (Note 1) .............. 4.8A
Operating Temperature Range ............................. -40°C to +85°C
Junction Temperature ........................................ -150°C
Storage Temperature Range ................................. -65°C to +150°C
Soldering Temperature (reflow) ............................. +260°C
Continuous Power Dissipation at T_A = +70°C
(Derate 23.8mW/°C above +70°C) ......................... 1905mW

Note 1: LXBB1/LXBB2 node has internal clamp diodes to PGNDBB and INBB. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed the power dissipation limit of IC package.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

Junction-to-Ambient Thermal Resistance (θ_JA)........... 55.49°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_SYS = V_INBB = +3.8V, V_FB_BB = V_OUTBB = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.)

(Note 3)

<table>
<thead>
<tr>
<th>PARAMETER</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td><strong>GENERAL</strong></td>
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<tr>
<td>Input Voltage Range</td>
<td>V_INBB</td>
<td></td>
<td>2.3</td>
<td>5.5</td>
<td>V</td>
<td></td>
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<tr>
<td>Shutdown Supply Current</td>
<td>I_SHDN_25C</td>
<td>EN = low, T_A = +25°C</td>
<td>0.1</td>
<td></td>
<td>µA</td>
<td></td>
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<tr>
<td></td>
<td>I_SHDN_85C</td>
<td>EN = low, T_A = +85°C (Note 5)</td>
<td>1</td>
<td></td>
<td></td>
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<tr>
<td>Input Supply Current</td>
<td>I_Q_SKIP</td>
<td>SKIP mode, no switching</td>
<td>40</td>
<td>60</td>
<td>µA</td>
<td></td>
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<tr>
<td></td>
<td>I_Q_PWM</td>
<td>FPWM mode, no load</td>
<td>6</td>
<td></td>
<td>mA</td>
<td></td>
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<tr>
<td>Active Discharge Resistance</td>
<td>R_DISCHG</td>
<td></td>
<td>100</td>
<td></td>
<td>Ω</td>
<td></td>
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<tr>
<td>Thermal Shutdown</td>
<td>T_SHDN</td>
<td>Rising, 20°C hysteresis</td>
<td>+165</td>
<td></td>
<td>°C</td>
<td></td>
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<tr>
<td><strong>H-BRIDGE</strong></td>
<td></td>
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<tr>
<td>Output Voltage Range</td>
<td>V_OUT</td>
<td></td>
<td>2.60</td>
<td>5.14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Default Output Voltage</td>
<td>VOUT[6:0] = 0x28</td>
<td></td>
<td>3.4</td>
<td></td>
<td>V</td>
<td></td>
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<tr>
<td>Output Voltage Accuracy</td>
<td>V_OUT_ACC1</td>
<td>PWM mode, VOUT[6:0] = 0x28, no load</td>
<td>-1.0</td>
<td>+1.0</td>
<td>%</td>
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<tr>
<td></td>
<td>V_OUT_ACC2</td>
<td>SKIP mode, VOUT[6:0] = 0x28, no load, T_A = +25°C</td>
<td>-1.0</td>
<td>+4.5</td>
<td>%</td>
<td></td>
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<tr>
<td>Line Regulation</td>
<td>V_INBB = 2.3V to 5.5V</td>
<td></td>
<td>0.200</td>
<td></td>
<td>%/V</td>
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<tr>
<td>Load Regulation</td>
<td>(Note 4)</td>
<td></td>
<td>0.125</td>
<td></td>
<td>%/A</td>
<td></td>
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<tr>
<td>Line Transient Response</td>
<td>V_OS1</td>
<td>I_OUT = 1.5A, V_INB changes from 3.4V to 2.9V in 25µs (20mV/µs), L = 1µH, C_OUT_NOM = 47µF (Note 4)</td>
<td>50</td>
<td></td>
<td>mV</td>
<td></td>
</tr>
</tbody>
</table>

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Maxim Integrated │ 2
## Electrical Characteristics (continued)

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BB} = V_{OUTBB} = +3.3V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.)

(Note 3)

<table>
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<tr>
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<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Load Transient Response</td>
<td>V_{OS2} V_{US2}</td>
<td>I_{OUT} changes from 10mA to 1.5A in 15µs, L = 1µH, C_{OUT_NOM} = 47µF (Note 4)</td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
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<tr>
<td>Output Voltage Ramp-Up Slew Rate</td>
<td></td>
<td>BB_RU_SR = 0 (Note 6)</td>
<td>20</td>
<td></td>
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<td>mV/µs</td>
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<tr>
<td></td>
<td></td>
<td>BB_RU_SR = 1 (Note 6)</td>
<td>40</td>
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<td>mV/µs</td>
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<tr>
<td>Output Voltage Ramp-down Slew Rate</td>
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<td>BB_RD_SR = 0 (Note 6)</td>
<td>5</td>
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<td>mV/µs</td>
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<tr>
<td></td>
<td></td>
<td>BB_RD_SR = 1 (Note 6)</td>
<td>10</td>
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<td>mV/µs</td>
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<tr>
<td>Typical Load Efficiency</td>
<td>η_{OUT_TYP}</td>
<td>I_{OUT} = 100mA (Note 4)</td>
<td>95</td>
<td></td>
<td></td>
<td>%</td>
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<tr>
<td>Peak Efficiency</td>
<td>η_{PK}</td>
<td></td>
<td>97.5</td>
<td></td>
<td></td>
<td>%</td>
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<tr>
<td>LXBB1/2 Current Limit</td>
<td>I_{LIM,LXBB}</td>
<td>ILIM[1:0] = 11b or GPIO_CFG[2:0] = 010b, GPIO = high</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ILIM[1:0] = 10b</td>
<td>3.1</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>ILIM[1:0] = 01b or GPIO_CFG[2:0] = 010b, GPIO = low</td>
<td>1.80</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>ILIM[1:0] = 00b</td>
<td>1.15</td>
<td></td>
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<td></td>
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<tr>
<td>High-Side PMOS ON Resistance</td>
<td>R_{DSON(PMOS)}</td>
<td>I_{LXBB} = 100mA per switch</td>
<td>34</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>Low-Side NMOS ON Resistance</td>
<td>R_{DSON(NMOS)}</td>
<td>I_{LXBB} = 100mA per switch</td>
<td>45</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>f_{SW}</td>
<td>PWM mode, T_A = +25°C</td>
<td>2.25</td>
<td>2.50</td>
<td>2.75</td>
<td>MHz</td>
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<tr>
<td>Turn-On Delay Time</td>
<td>t_{ON_DLY}</td>
<td>From EN asserting to LXBB switching (Note 6)</td>
<td>100</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Soft-Start Time</td>
<td>t_{SS}</td>
<td>I_{OUT} = 10mA, ILIM[1:0] = 11b or 10, or GPIO_CFG[2:0] = 010b, GPIO = high (Note 4)</td>
<td>120</td>
<td></td>
<td></td>
<td>µs</td>
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<tr>
<td></td>
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<td>I_{OUT} = 10mA, ILIM[1:0] = 01b or 00, or GPIO_CFG[2:0] = 010b, GPIO = low (Note 4)</td>
<td>800</td>
<td></td>
<td></td>
<td>µs</td>
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<tr>
<td>Minimum Effective Output Capacitance</td>
<td>C_{EFF(MIN)}</td>
<td>0A &lt; I_{OUT} &lt; 3000mA</td>
<td>16</td>
<td></td>
<td></td>
<td>µF</td>
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<tr>
<td>LXBB1, LXBB2 Leakage Current</td>
<td>I_{LK_25}</td>
<td>VLXBB1/2 = 0V or 5.5V, VOUTBB = 5.5V, V_SYS = VINBB = 5.5V, T_A = +25°C</td>
<td>0.1</td>
<td>1</td>
<td></td>
<td>µA</td>
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<tr>
<td></td>
<td>I_{LK_85}</td>
<td>VLXBB1/2 = 0V or 5.5V, VOUTBB = 5.5V, V_SYS = VINBB = 5.5V, T_A = +25°C (Note 5)</td>
<td>0.2</td>
<td></td>
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<tr>
<td>SYS Undervoltage Lockout Threshold</td>
<td>V_{UVLO_R}</td>
<td>V_SYS rising</td>
<td>2.375</td>
<td>2.50</td>
<td>2.625</td>
<td>V</td>
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<tr>
<td></td>
<td>V_{UVLO_F}</td>
<td>V_SYS falling</td>
<td>2.05</td>
<td></td>
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</tbody>
</table>
## Electrical Characteristics (continued)

$(V_{SYS} = V_{INBB} = +3.8V, V_{FB_{BB}} = V_{OUTBB} = +3.3V, T_A = -40^\circ C$ to $+85^\circ C$, typical values are at $T_A = +25^\circ C$, unless otherwise noted.)

(Note 3)

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>ENABLE INPUT (EN)</td>
<td></td>
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<tr>
<td>EN Logic-Low Threshold</td>
<td>$V_{EN_L}$</td>
<td>$V_{SYS} \leq 5.5V, T_A = +25^\circ C$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>EN Logic-High Threshold</td>
<td>$V_{EN_H}$</td>
<td>$V_{SYS} \leq 5.5V, T_A = +25^\circ C$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>EN Internal Pulldown Resistance</td>
<td>$R_{EN}$</td>
<td>Pulldown resistor to GND</td>
<td>400 800 1600 kΩ</td>
</tr>
<tr>
<td>GENERAL PURPOSE INPUT/OUTPUT (GPIO)</td>
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<tr>
<td>Input Logic-Low Threshold</td>
<td>$V_{GPI_L}$</td>
<td>GPIO[2:0] = 001b or 010b or 011b, $V_{SYS} \leq 4.5V, T_A = +25^\circ C$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Input Logic-High Threshold</td>
<td>$V_{GPI_H}$</td>
<td>GPIO[2:0] = 001b or 010b or 011b, $V_{SYS} \leq 4.5V, T_A = +25^\circ C$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Input Internal Pulldown Resistance</td>
<td>$R_{EN}$</td>
<td>GPIO[2:0] = 001b or 010b or 011b, Pulldown resistor to GND</td>
<td>400 800 1600 V</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>$V_{GPO_L}$</td>
<td>GPIO[2:0] = 100b or 101b, $I_{SINK} = 1mA$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>$I_{GPO_25C}$</td>
<td>GPIO[2:0] = 100b or 101b, $T_A = +25^\circ C$</td>
<td>-1 +1 µA</td>
</tr>
<tr>
<td></td>
<td>$I_{GPO_85C}$</td>
<td>GPIO[2:0] = 100b or 101b, $T_A = +85^\circ C$ (Note 5)</td>
<td>0.1 µA</td>
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<tr>
<td>POK Threshold</td>
<td>$V_{POK_R}$</td>
<td>GPIO[2:0] = 100b, $V_{OUTBB}$ rising, expressed as a percentage of $V_{OUTBB}$</td>
<td>92.5 %</td>
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<td></td>
<td>$V_{POK_F}$</td>
<td>GPIO[2:0] = 100b, $V_{OUTBB}$ falling, expressed as a percentage of $V_{OUTBB}$</td>
<td>90 %</td>
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<tr>
<td>I2C-COMPATIBLE INTERFACE—I/O STAGE</td>
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<tr>
<td>SCL, SDA Input High Voltage</td>
<td>$V_{IH}$</td>
<td></td>
<td>1.4 V</td>
</tr>
<tr>
<td>SCL, SDA Input Low Voltage</td>
<td>$V_{IL}$</td>
<td></td>
<td>0.4 V</td>
</tr>
<tr>
<td>SCL, SDA Input Hysteresis</td>
<td>$V_{HYS}$</td>
<td>(Note 5)</td>
<td>0.1 V</td>
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<tr>
<td>SCL, SDA Input Current</td>
<td>$I_I$</td>
<td></td>
<td>-10 10 µA</td>
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<tr>
<td>SDA Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$I_{SINK} = 3mA$</td>
<td>0.4 V</td>
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<tr>
<td>SCL, SDA Input Capacitance</td>
<td>$C_I$</td>
<td></td>
<td>10 pF</td>
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<tr>
<td>Maximum Pulse Width of Spikes that must be suppressed by the input filter</td>
<td>$I_{SP}$</td>
<td>(Note 5)</td>
<td>50 ns</td>
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</tbody>
</table>
MAX77816  
High-Efficiency Buck-Boost Regulator  
with 5A Switches

Electrical Characteristics (continued)

\( V_{SYS} = V_{INBB} = +3.8\, \text{V}, \; V_{FB\_BB} = V_{OUTBB} = +3.3\, \text{V}, \; T_A = -40^\circ C \text{ to } +85^\circ C, \) typical values are at \( T_A = +25^\circ C, \) unless otherwise noted.)

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<tr>
<td>I2C-COMPATIBLE INTERFACE–TIMING (Note 5)</td>
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<tr>
<td>Clock Frequency</td>
<td>( f_{SCL} )</td>
<td></td>
<td>1</td>
<td>MHz</td>
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<tr>
<td>Hold Time (REPEATED) START Condition</td>
<td>( t_{HD_STA} )</td>
<td></td>
<td>0.26</td>
<td>µs</td>
<td></td>
<td></td>
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<tr>
<td>SCL Low Period</td>
<td>( t_{LOW} )</td>
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<td>0.5</td>
<td>µs</td>
<td></td>
<td></td>
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<tr>
<td>SCL High Period</td>
<td>( t_{HIGH} )</td>
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<td>0.26</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Setup Time REPEATED START Condition</td>
<td>( t_{SU_STA} )</td>
<td></td>
<td>0.26</td>
<td>µs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DATA Hold Time</td>
<td>( t_{HD_DAT} )</td>
<td></td>
<td>0</td>
<td>µs</td>
<td></td>
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<tr>
<td>DATA Setup Time</td>
<td>( t_{SU_DAT} )</td>
<td></td>
<td>50</td>
<td>ns</td>
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<td></td>
</tr>
<tr>
<td>Setup Time for STOP Condition</td>
<td>( t_{SU_STO} )</td>
<td></td>
<td>0.26</td>
<td>µs</td>
<td></td>
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<tr>
<td>Bus-Free Time Between STOP and START</td>
<td>( t_{BUF} )</td>
<td></td>
<td>0.5</td>
<td>µs</td>
<td></td>
<td></td>
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<tr>
<td>Capacitive Load for Each Bus Line</td>
<td>( C_B )</td>
<td></td>
<td>550</td>
<td>pF</td>
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</tr>
</tbody>
</table>

**Note 3:** Limits are 100% production tested at \( T_A = +25^\circ C. \) Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

**Note 4:** Guaranteed by design. Not production tested.

**Note 5:** Guaranteed by ATE characterization. Not directly tested in production.

**Note 6:** Guaranteed by design. Production tested through scan.
Typical Operating Characteristics

(V_{SYS} = V_{INBB} = +3.8V, V_{FB_BK} = V_{OUTBB} = +3.3V, T_A = +25°C.)
### Bump Configuration

#### TOP VIEW
(BUMP SIDE DOWN)

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
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<tbody>
<tr>
<td>+</td>
<td>SYS</td>
<td>EN</td>
<td>GND</td>
<td>SDA</td>
</tr>
<tr>
<td>B</td>
<td>FB_BB</td>
<td>LXBB2</td>
<td>GPIO</td>
<td>LXBB1</td>
</tr>
<tr>
<td>C</td>
<td>OUTBB</td>
<td>LXBB2</td>
<td>PGNDBB</td>
<td>LXBB1</td>
</tr>
<tr>
<td>D</td>
<td>OUTBB</td>
<td>LXBB2</td>
<td>PGNDBB</td>
<td>LXBB1</td>
</tr>
</tbody>
</table>

**20-BUMP WLP**
(5mm x 4mm, 0.4mm PITCH)

### Bump Description

<table>
<thead>
<tr>
<th>BUMPM</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>SYS</td>
<td>System (Battery) Voltage Input. Bypass to GND with a 1µF capacitor.</td>
</tr>
<tr>
<td>A2</td>
<td>EN</td>
<td>Active-High, Buck-Boost External Enable Input. An 800kΩ internal pulldown resistance to the GND.</td>
</tr>
<tr>
<td>A3</td>
<td>GND</td>
<td>Quite Ground. Star-ground connection to system GND.</td>
</tr>
<tr>
<td>A4</td>
<td>SDA</td>
<td>I²C Data I/O (Hi-Z in OFF State). This pin requires a pullup resistor to I²C power supply. Connect to GND if not used.</td>
</tr>
<tr>
<td>A5</td>
<td>SCL</td>
<td>I²C Clock Input (Hi-Z in OFF State). This pin requires a pullup resistor to I²C power supply. Connect to GND if not used.</td>
</tr>
<tr>
<td>B1</td>
<td>FB_BB</td>
<td>Buck-Boost Output Voltage Feedback</td>
</tr>
<tr>
<td>B2, C2, D2</td>
<td>LXBB2</td>
<td>Buck-Boost Switching Node 2</td>
</tr>
</tbody>
</table>
| B3    | GPIO | Multifunction GPIO:
MAX77816A/B/C: General Purpose Input. An 800kΩ internal pulldown resistance to the GND.
MAX77816D/E: Open-Drain Output. An external pullup resistor is required. |
| B4, C4, D4 | LXBB1 | Buck-Boost Switching Node 1 |
| B5, C5, D5 | INBB | Buck-Boost Input. Bypass to PGNDBB with a 10µF capacitor. |
| C1, D1 | OUTBB | Buck-Boost Output |
| C3, D3 | PGNDBB | Buck-Boost Power Ground. Star-ground connection to system GND. |
Detailed Description

Enable Control
When EN pin is set to high, the IC turns on the internal bias circuitry which takes typically 100µs (\(t_{ON\_DLY}\)) to be settled. As soon as the bias is ready, all user registers are accessible through I\(^2\)C. Write BB_EN bit to 1 to enable (register default) buck-boost output voltage regulation. The V\(_{OUT\_BB}\) takes 800µs (\(t_{SS}\)) to the nominal regulated voltage after BB_EN’s setting.

When EN pin is pulled low, the IC goes into shutdown mode. This event also resets all type-O registers to their POR default values.

Immediate Turn-Off Events
The following events initiate immediate turn-off.
- Thermal protection (\(T_J > +165°C\))
- \(V_{SYS} < SYS\_UVLO\) falling threshold (\(V_{UVLO\_F}\))
- Overcurrent protection (ILIM is consistently hit for 3ms)

The events in this category disable buck-boost until the hazardous condition come back to normal conditions.

Inductor Peak Current Limit (ILIM)
The buck-boost regulator’s high-side MOSFETs peak current limit (\(I_{LIM\_LXB}\)) is register programmable. Applications can use \(I_{LIM\_LXB}\) programmability to ensure that the regulator never exceeds the saturation current rating of the inductor on the PCB. In MAX77816B, \(I_{LIM\_LXB}\) is GPIO pin programmable. Refer to the Multifunction GPIO Pin section.

Multifunction GPIO Pin
The IC has a general-purpose input and output (GPIO) pin which can be configured as 5 different functions through GPIO_CFG[2:0]. The default function of the GPIO pin is listed below:
- MAX77816A: FPWM Mode Enable
  When the GPIO pin is connected to GND, the buck-boost regulator automatically transitions from SKI P mode to fixed frequency operation (PWM) as load current increases. SKI P mode helps maximize the buck-boost regulator’s efficiency at light load. When the GPIO is connected to a voltage above \(V_{GPI\_H}\), forced PWM (FPWM) switching behavior is enabled. The FPWM mode benefits applications where lowest output ripple is required. The BB_FPWM bitfield is ignored when GPIO_CFG[2:0] = 001b.
- MAX77816B: Inductor Peak Current-Limit (ILIM) Selection
  The buck-boost regulator’s high-side MOSFETs peak current limit (\(I_{LIM\_LXB}\)) is GPIO pin programmable. The ILIM[1:0] bitfield is ignored when GPIO_CFG[2:0] = 010b. Connect GPIO to GND to set ILIM to 1.8A (typ). Connect GPIO to a voltage above \(V_{GPI\_H}\) to program ILIM to 5A (typ).
- MAX77816C: Output Voltage Selection
  The GPIO pin sets the output voltage dynamically between VOUT[6:0] (GPIO = LOW) and VOUT_H[6:0] (GPIO = HIGH). When EN pin is asserted, the status of the GPIO pin is latched until completing soft-start so that changes on the GPIO pin are ignored. After soft-start is done, internal logic sets V\(_{OUT\_BB}\) based on the GPIO input.
- MAX77816D: Power-OK (POK) Indicator
  The device features an open-drain GPIO output to monitor the output voltage. The GPIO pin requires an external pullup resistor. GPIO goes high (high-impedance) after the output increases above 92.5% (\(V_{POK\_R}\)) of the nominal regulated voltage (V\(_{OUT\_REG}\)). GPIO goes low when the regulator output drops below 90% (\(V_{POK\_F}\)) of V\(_{OUT\_REG}\).
- MAX77816E: Interrupts Indicator
  The GPIO indicates the application processor that the status of the device has changed.
  INT[3:0], INT_MASK[3:0], and the GPIO pin work together to present the buck-boost regulator’s abnormal status, including overvoltage, overcurrent, power OK, and thermal shutdown. GPIO goes low when one or more bits of INT[3:0] becomes 1, and the related interrupts are not masked in INT_MASK[3:0]. GPIO becomes high (cleared) as soon as the read action of INT[3:0] starts.

Table 1. Enable Control Logic Truth Table

<table>
<thead>
<tr>
<th>EN PIN</th>
<th>BB_EN BIT</th>
<th>OPERATING MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>low</td>
<td>x</td>
<td>Device off</td>
</tr>
<tr>
<td>high</td>
<td>0</td>
<td>Disable output</td>
</tr>
<tr>
<td>high</td>
<td>1 (default)</td>
<td>Enable output</td>
</tr>
</tbody>
</table>
Buck-Boost Regulator

The MAX77816 buck-boost regulator utilizes a four-switch H-bridge configuration to realize buck, buck-boost, and boost operating modes. In this way, this topology maintains output voltage regulation when the input voltage is greater than, equal to, or less than the output voltage. The MAX77816 buck-boost is ideal in Li-ion battery-powered applications providing 2.60V to 5.14V of output voltage range and up to 3A of output current. High switching frequency and a unique control algorithm allow the smallest solution size, low output noise, and highest efficiency across a wide input voltage and output current range.

Figure 1. Interrupt Network

Figure 2. Buck-Boost Block Diagram
H-Bridge Controller

H-Bridge architecture operates at 2.5MHz fixed frequency with a pulse width modulated (PWM), current-mode control scheme. This topology is in a cascade of a boost regulator and a buck regulator using a single inductor and output capacitor. Buck, buck-boost, and boost stages are 100% synchronous for highest efficiency in portable applications.

There are three phases implemented with the H-bridge switch topology, as shown in Figure 3:

- **Φ1** Switch period (Phase-1: HS1 = ON, LS2 = ON) stores energy in the inductor, ramping up the inductor current at a rate proportional to the input voltage divided by inductance; $\frac{V_{INBB}}{L}$.
- **Φ2** Switch period (Phase-2: HS1 = ON, HS2 = ON) ramps the inductor current up or down, depending on the differential voltage across the inductor, divided by inductance; $\pm(\frac{V_{INBB} - V_{OUTBB}}{L})$.
- **Φ3** Switch period (Phase-3: LS1 = ON, HS2 = ON) ramps down the inductor current at a rate proportional to the output voltage divided by inductance; $-\frac{V_{OUTBB}}{L}$.

2-Phase buck topology is utilized when $V_{INBB} > V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ2 is followed by switch period Φ3, resulting in an inductor current waveform similar to Figure 4.

2-Phase boost topology is utilized when $V_{INBB} < V_{OUTBB}$. A switching cycle is completed in one clock period. Switch period Φ1 is followed by switch period Φ2, resulting in an inductor current waveform similar to Figure 5.

![Figure 3. Buck-Boost Switching Intervals](image)

![Figure 4. 2-Phase Buck Mode Switching Current Waveforms](image)

![Figure 5. 2-Phase Boost Mode Switching Current Waveforms](image)
Output Voltage Slew-Rate Control
Buck-Boost regulator supports programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew-rate can be set to 20mV/µs or 40mV/µs through BB_RU_SR bit, while the ramp-down slew-rate is programmable to 5mV/µs or 10mV/µs through BB_RD_SR bit.

Output Active Discharge
Buck-boost provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (BB_AD = 1), the internal resistor discharges the energy stored in the output capacitor to PGND_BB whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (BB_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

Inductor Selection
Buck-boost is optimized for a 1µH inductor. The lower the inductor DCR, the higher buck-boost efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for buck-boost.

Input Capacitor Selection
The input capacitor, C_IN, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of C_IN at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output Capacitor Selection
The output capacitor, C_OUT, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_OUT must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 16µF of minimum effective output capacitance. Considering DC bias characteristic of ceramic capacitors, a 47µF 6.3V capacitor is recommended for most of applications.

Table 2. Suggested Inductors for Buck-Boost

<table>
<thead>
<tr>
<th>MANUFACTURER</th>
<th>SERIES</th>
<th>NOMINAL INDUCTANCE (µH)</th>
<th>DC RESISTANCE (typ) (mΩ)</th>
<th>CURRENT RATING (A) -30% (%∆L/L)</th>
<th>CURRENT RATING (A) ∆T = -40°C RISE</th>
<th>DIMENSIONS (L x W x H (mm))</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDK</td>
<td>TFM201610GHM-1R0MTAA</td>
<td>1.0</td>
<td>50</td>
<td>3.8</td>
<td>3.0</td>
<td>2.0 x 1.6 x 1.0</td>
</tr>
<tr>
<td>TOKO</td>
<td>DFE322512C</td>
<td>1.0</td>
<td>34</td>
<td>4.6</td>
<td>3.7</td>
<td>3.2 x 2.5 x 1.2</td>
</tr>
<tr>
<td>Coilcraft</td>
<td>XAL4020-102MEB</td>
<td>1.0</td>
<td>13</td>
<td>8.7</td>
<td>9.6</td>
<td>4.0 x 4.0 x 2.1</td>
</tr>
</tbody>
</table>

Serial Interface
\textsuperscript{I}²C-compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. Refer to the Register Map section for details.

\textsuperscript{I}²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). \textsuperscript{I}²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration
\textsuperscript{I}²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 6 shows an example of a typical \textsuperscript{I}²C system. A device on \textsuperscript{I}²C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When MAX77816 \textsuperscript{I}²C compatible interface is operating, it is a slave on \textsuperscript{I}²C bus and it can be both a transmitter and a receiver.

Bit Transfer
One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).
START and STOP Conditions

When \$I^2C\$ serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to MAX77816. The master terminates transmission by issuing a NOT-ACKNOWLEDGE followed by a STOP condition.

STOP condition frees the bus. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from \$I^2C\$ serial interface until the next START condition, minimizing digital noise and feedthrough.

Acknowledged

Both \$I^2C\$ bus master and MAX77816 (Slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.
Slave Address

I²C slave address of the IC is shown in Table 3.

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The IC does not implement I²C specification called general call address. If the IC sees general call address (00000000b), it will not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides I²C 3.0-compatible (3.4MHz) serial interface.

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast mode plus)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the Pullup Resistor Sizing section of I²C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V²/R).

At power-up and after each STOP condition, the IC inputs filters are set for standard mode, fast mode, or fast mode plus (i.e. 0Hz to 1MHz).

Communication Protocols

The IC supports both writing and reading from its registers. The following sections show the I²C communication protocols for each functional block. The power block uses the same communications protocols.

Writing to a Single Register

Figure 10 shows the protocol for I²C master device to write one byte of data to the IC. This protocol is the same as SMBus specification’s write byte protocol. The write byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Table 3. I²C Slave Address

<table>
<thead>
<tr>
<th>SLAVE ADDRESS (7 bit)</th>
<th>SLAVE ADDRESS (Write)</th>
<th>SLAVE ADDRESS (Read)</th>
</tr>
</thead>
<tbody>
<tr>
<td>001 1000 (7’h18)</td>
<td>0x30 (0011 0000)</td>
<td>0x31 (0011 0001)</td>
</tr>
</tbody>
</table>

Figure 9. Slave Address Byte Example
Writing to a Sequential Register

Figure 11 shows the protocol for writing to a sequential register. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a STOP or REPEATED START.

The writing to sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Writing Multiple Bytes using Register-Data Pairs

Figure 12 shows the protocol for I^2C master device to write multiple bytes to the IC using register-data pairs. This protocol allows I^2C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP condition.

The multiple byte register-data pair protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte will be loaded into its target register and the data will become active.
8) Steps 4 to 7 are repeated as many times as the master requires.
9) The master sends a STOP condition.
Figure 11. Writing to Sequential Registers X to N
Figure 12. Writing to Multiple Registers with Multiple Byte Register-Data Pairs Protocol
Reading from a Single Register

I²C master device reads one byte of data to the IC. This protocol is the same as SMBus specification’s “Read Byte” protocol.

The “Read Byte” protocol is as follows:
1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a NOT-ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Reading from a Sequential Register

Figure 13 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data. When the master has all the data it requires, it issues a not-acknowledge (nA) and a STOP (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:
1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Figure 13. Reading Continuously from Sequential Registers X to N
MAX77816

High-Efficiency Buck-Boost Regulator
with 5A Switches

Registers

Register Map

I²C Slave Address (W/R): 0x30 / 0x31

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>REGISTER NAME</th>
<th>BIT 7</th>
<th>BIT 6</th>
<th>BIT 5</th>
<th>BIT 4</th>
<th>BIT 3</th>
<th>BIT 2</th>
<th>BIT 1</th>
<th>BIT 0</th>
<th>RESET VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>DEVICE_ID</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>TSHDN</td>
<td>BB_POKn</td>
<td>BB_OVP</td>
<td>BB_OCP</td>
</tr>
<tr>
<td>0x01</td>
<td>STATUS</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>TSHDN</td>
<td>BB_POKn</td>
<td>BB_OVP</td>
<td>BB_OCP</td>
</tr>
<tr>
<td>0x02</td>
<td>CONFIG1</td>
<td>ILIM[1:0]</td>
<td>BB_RU _SR</td>
<td>BB_RD _SR</td>
<td>BB_OVP_TH[1:0]</td>
<td>BB_AD</td>
<td>BB _FPWM</td>
<td>0xCE</td>
<td>0xCE</td>
<td>0xCE</td>
</tr>
<tr>
<td>0x03</td>
<td>CONFIG2</td>
<td>RSVD</td>
<td>BB_EN</td>
<td>EN_PD</td>
<td>POK_POL</td>
<td>RSVD</td>
<td>GPIO_CFG[2:0]</td>
<td>0x71</td>
<td>0x71</td>
<td>0x71</td>
</tr>
<tr>
<td>0x04</td>
<td>VOUT</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
</tr>
<tr>
<td>0x05</td>
<td>VOUT_H</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
</tr>
<tr>
<td>0x06</td>
<td>INT_MASK</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>THM_INT _MASK</td>
<td>POK_INT _MASK</td>
<td>OVP_INT _MASK</td>
</tr>
<tr>
<td>0x07</td>
<td>INT</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>RSVD</td>
<td>THM_INT</td>
<td>POK_INT</td>
<td>OVP_INT</td>
<td>OCP_INT</td>
</tr>
</tbody>
</table>

Register Reset Conditions

Type-O: Registers are reset when VSYS < VUVLO_F OR EN = LOW

DEVICE_ID

Device ID Register

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>ACCESS TYPE</th>
<th>TYPE: O</th>
<th>RESET VALUE: N/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Read Only</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

BIT | NAME      | POR | DESCRIPTION     |
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<td>—</td>
<td>Version</td>
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<tr>
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<td></td>
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<tr>
<td>6:3</td>
<td>VERSION[3:0]</td>
<td>—</td>
<td>Chip Revision History</td>
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<tr>
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<td></td>
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<td>001b: PASS1</td>
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</table>

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### STATUS

Status Register

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<th>TYPE: O</th>
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<tr>
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<th>POR</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:4</td>
<td>RESERVED</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>
| 3  | TSHDN      | —   | Thermal Shutdown Status
   |
|    |            |     | 0: Junction temperature ($T_{JCT}$) ≤ 165°C
   |    |            |     | 1: Junction temperature ($T_{JCT}$) > 165°C
| 2  | BB_POKn    | —   | Power-OK Status
   |
|    |            |     | 0: $V_{OUTBB}$ is below the POK threshold
   |    |            |     | 1: $V_{OUTBB}$ is above the POK threshold
| 1  | BB_OVP     | —   | Overvoltage Status
   |
|    |            |     | 0: $V_{OUTBB}$ is below the OVP threshold
   |    |            |     | 1: $V_{OUTBB}$ is above the OVP threshold
   |    |            |     | The OVP threshold is set by BB_OVP_TH[1:0]
| 0  | BB_OCP     | —   | Overcurrent Status
   |
|    |            |     | 0: Inductor peak current is below the ILIM threshold
   |    |            |     | 1: Inductor peak current is above the ILIM threshold
   |    |            |     | The ILIM threshold is set by ILIM[1:0]

---

MAX77816 High-Efficiency Buck-Boost Regulator with 5A Switches

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## CONFIG1
Configuration Register 1

<table>
<thead>
<tr>
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<tbody>
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<thead>
<tr>
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<th>NAME</th>
<th>POR</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 7:6     | ILIM[1:0]          | 11  | Inductor Peak Current Limit  
00b: 1.15A  
01b: 1.80A  
10b: 3.1A  
11b: 5A  
When GPIO_CFG[2:0] = 010b, ILIM[1:0] does not set inductor peak current level. Inductor peak current level is set by GPIO |
| 5       | BB_RU_SR           | 0   | Rising Ramp-Rate Control  
0: 20mV/µs  
1: 40mV/µs |
| 4       | BB_RD_SR           | 0   | Ramp-Down Slew Rate Control  
0: 5mV/µs  
1: 10mV/µs |
| 3:2     | BB_OVP_TH[1:0]     | 11  | Output OVP Threshold  
00b: No OVP  
01b: 110% of VOUT  
10b: 115% of VOUT  
11b: 120% of VOUT |
| 1       | BB_AD              | 1   | Output Active Discharge  
0: Disable active discharge  
1: Enable active discharge |
| 0       | BB_FPWM            | 0   | Forced PWM Enable  
0: SKIP mode  
1: Forced PWM  
When GPIO_CFG[2:0] = 001b, BB_FPWM does not set inductor peak current level. Inductor peak current level is set by GPIO |
### CONFIG2
Configuration Register2

<table>
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<th>POR</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>RESERVED</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>
| 6   | BB_EN      | 1   | 0: Disable buck-boost output  
1: Enable buck-boost output |
| 5   | EN_PD      | 1   | EN Input Pulldown Resistor Enable Setting  
0: Disable  
1: Enable |
| 4   | POK_POL    | 1   | 0: Active low  
1: Active high |
| 3   | RESERVED   | 0   |             |
| 2:0 | GPIO_CFG[2:0] | 001 | GPIO Pin Function Configuration  
001b: FPWM mode enable, MAX77816A default  
010b: Inductor peak current-limit selection,  
MAX77816B default  
011b: Output voltage selection, MAX77816C default  
100b: Power-OK status indication, MAX77816D default  
101b: Interrupt indication, MAX77816E default |
### VOUT

**Output Voltage Setting Register**

<table>
<thead>
<tr>
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<table>
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<th>BIT</th>
<th>NAME</th>
<th>POR</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
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<td>RESERVED</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

#### 6:0  VOUT[6:0]  011 1000

**Buck-Boost Output Voltage**

GPIO_CFG[2:0] = 011b: \( V_{OUT} \) sets the output voltage when GPIO = low

- 0x00 = 2.60V
- 0x01 = 2.62V
- 0x02 = 2.64V
- 0x03 = 2.66V
- 0x04 = 2.68V
- 0x05 = 2.70V
- 0x06 = 2.72V
- 0x07 = 2.74V
- 0x08 = 2.76V
- 0x09 = 2.78V
- 0x0A = 2.80V
- 0x0B = 2.82V
- 0x0C = 2.84V
- 0x0D = 2.86V
- 0x0E = 2.88V
- 0x0F = 2.90V
- 0x10 = 2.92V
- 0x11 = 2.94V
- 0x12 = 2.96V
- 0x13 = 2.98V
- 0x14 = 3.00V
- 0x15 = 3.02V
- 0x16 = 3.04V
- 0x17 = 3.06V
- 0x18 = 3.08V
- 0x19 = 3.10V
- 0x1A = 3.12V
- 0x1B = 3.14V
- 0x1C = 3.16V
- 0x1D = 3.18V
- 0x1E = 3.20V
- 0x1F = 3.22V

- 0x20 = 3.24V
- 0x21 = 3.26V
- 0x22 = 3.28V
- 0x23 = 3.30V
- 0x24 = 3.32V
- 0x25 = 3.34V
- 0x26 = 3.36V
- 0x27 = 3.38V
- 0x28 = 3.40V
- 0x29 = 3.42V
- 0x2A = 3.44V
- 0x2B = 3.46V
- 0x2C = 3.48V
- 0x2D = 3.50V
- 0x2E = 3.52V
- 0x2F = 3.54V
- 0x30 = 3.56V
- 0x31 = 3.58V
- 0x32 = 3.60V
- 0x33 = 3.62V
- 0x34 = 3.64V
- 0x35 = 3.66V
- 0x36 = 3.68V
- 0x37 = 3.70V
- 0x38 = 3.72V
- 0x39 = 3.74V
- 0x3A = 3.76V
- 0x3B = 3.78V
- 0x3C = 3.80V
- 0x3D = 3.82V
- 0x3E = 3.84V
- 0x3F = 3.86V

- 0x40 = 3.88V
- 0x41 = 3.90V
- 0x42 = 3.92V
- 0x43 = 3.94V
- 0x44 = 3.96V
- 0x45 = 3.98V
- 0x46 = 4.00V
- 0x47 = 4.02V
- 0x48 = 4.04V
- 0x49 = 4.06V
- 0x4A = 4.08V
- 0x4B = 4.10V
- 0x4C = 4.12V
- 0x4D = 4.14V
- 0x4E = 4.16V
- 0x4F = 4.18V
- 0x50 = 4.20V
- 0x51 = 4.22V
- 0x52 = 4.24V
- 0x53 = 4.26V
- 0x54 = 4.28V
- 0x55 = 4.30V
- 0x56 = 4.32V
- 0x57 = 4.34V
- 0x58 = 4.36V
- 0x59 = 4.38V
- 0x5A = 4.40V
- 0x5B = 4.42V
- 0x5C = 4.44V
- 0x5D = 4.46V
- 0x5E = 4.48V
- 0x5F = 4.50V

- 0x60 = 4.52V
- 0x61 = 4.54V
- 0x62 = 4.56V
- 0x63 = 4.58V
- 0x64 = 4.60V
- 0x65 = 4.62V
- 0x66 = 4.64V
- 0x67 = 4.66V
- 0x68 = 4.68V
- 0x69 = 4.70V
- 0x6A = 4.72V
- 0x6B = 4.74V
- 0x6C = 4.76V
- 0x6D = 4.78V
- 0x6E = 4.80V
- 0x6F = 4.82V
- 0x70 = 4.84V
- 0x71 = 4.86V
- 0x72 = 4.88V
- 0x73 = 4.90V
- 0x74 = 4.92V
- 0x75 = 4.94V
- 0x76 = 4.96V
- 0x77 = 4.98V
- 0x78 = 5.00V
- 0x79 = 5.02V
- 0x7A = 5.04V
- 0x7B = 5.06V
- 0x7C = 5.08V
- 0x7D = 5.10V
- 0x7E = 5.12V
- 0x7F = 5.14V
VOUT_H
Output Voltage Setting Register for MAX77816C, GPIO = HIGH

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>ACCESS TYPE</th>
<th>TYPE: O</th>
<th>RESET VALUE: 0x78</th>
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<tbody>
<tr>
<td>0x05</td>
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<thead>
<tr>
<th>BIT</th>
<th>NAME</th>
<th>POR</th>
<th>DESCRIPTION</th>
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</thead>
<tbody>
<tr>
<td>7</td>
<td>RESERVED</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

6:0 VOUT_H[6:0] 011 1000

Buck-Boost Output Voltage
GPIO_CFG[2:0]=011b: VOUT_H sets the output voltage when GPIO = high
GPIO_CFG[2:0]≠011b: VOUT_H does not control the output voltage

0x00 = 2.60V
0x01 = 2.62V
0x02 = 2.64V
0x03 = 2.66V
0x04 = 2.68V
0x05 = 2.70V
0x06 = 2.72V
0x07 = 2.74V
0x08 = 2.76V
0x09 = 2.78V
0x0A = 2.80V
0x0B = 2.82V
0x0C = 2.84V
0x0D = 2.86V
0x0E = 2.88V
0x0F = 2.90V
0x10 = 2.92V
0x11 = 2.94V
0x12 = 2.96V
0x13 = 2.98V
0x14 = 3.00V
0x15 = 3.02V
0x16 = 3.04V
0x17 = 3.06V
0x18 = 3.08V
0x19 = 3.10V
0x1A = 3.12V
0x1B = 3.14V
0x1C = 3.16V
0x1D = 3.18V
0x1E = 3.20V
0x1F = 3.22V

0x20 = 3.24V
0x21 = 3.26V
0x22 = 3.28V
0x23 = 3.30V
0x24 = 3.32V
0x25 = 3.34V
0x26 = 3.36V
0x27 = 3.38V
0x28 = 3.40V
0x29 = 3.42V
0x2A = 3.44V
0x2B = 3.46V
0x2C = 3.48V
0x2D = 3.50V
0x2E = 3.52V
0x2F = 3.54V
0x30 = 3.56V
0x31 = 3.58V
0x32 = 3.60V
0x33 = 3.62V
0x34 = 3.64V
0x35 = 3.66V
0x36 = 3.68V
0x37 = 3.70V
0x38 = 3.72V
0x39 = 3.74V
0x3A = 3.76V
0x3B = 3.78V
0x3C = 3.80V
0x3D = 3.82V
0x3E = 3.84V
0x3F = 3.86V

0x40 = 3.88V
0x41 = 3.90V
0x42 = 3.92V
0x43 = 3.94V
0x44 = 3.96V
0x45 = 3.98V
0x46 = 4.00V
0x47 = 4.02V
0x48 = 4.04V
0x49 = 4.06V
0x4A = 4.08V
0x4B = 4.10V
0x4C = 4.12V
0x4D = 4.14V
0x4E = 4.16V
0x4F = 4.18V
0x50 = 4.20V
0x51 = 4.22V
0x52 = 4.24V
0x53 = 4.26V
0x54 = 4.28V
0x55 = 4.30V
0x56 = 4.32V
0x57 = 4.34V
0x58 = 4.36V
0x59 = 4.38V
0x5A = 4.40V
0x5B = 4.42V
0x5C = 4.44V
0x5D = 4.46V
0x5E = 4.48V
0x5F = 4.50V

0x60 = 4.52V
0x61 = 4.54V
0x62 = 4.56V
0x63 = 4.58V
0x64 = 4.60V
0x65 = 4.62V
0x66 = 4.64V
0x67 = 4.66V
0x68 = 4.68V
0x69 = 4.70V
0x6A = 4.72V
0x6B = 4.74V
0x6C = 4.76V
0x6D = 4.78V
0x6E = 4.80V
0x6F = 4.82V
0x70 = 4.84V
0x71 = 4.86V
0x72 = 4.88V
0x73 = 4.90V
0x74 = 4.92V
0x75 = 4.94V
0x76 = 4.96V
0x77 = 4.98V
0x78 = 5.00V
0x79 = 5.02V
0x7A = 5.04V
0x7B = 5.06V
0x7C = 5.08V
0x7D = 5.10V
0x7E = 5.12V
0x7F = 5.14V
## INT_MASK
Interrupt Mask Register

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<td>RESERVED</td>
<td>0000</td>
<td>Thermal Shutdown Interrupt Mask Bit</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0: Unmask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask</td>
</tr>
<tr>
<td>3</td>
<td>THM_INT_MASK</td>
<td>0</td>
<td>Power-OK Interrupt Mask Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Unmask</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>1: Mask</td>
</tr>
<tr>
<td>2</td>
<td>POK_INT_MASK</td>
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<td>OVP Interrupt Mask Bit</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>0: Unmask</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Mask</td>
</tr>
<tr>
<td>1</td>
<td>OVP_INT_MASK</td>
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<td>OCP interrupt mask bit</td>
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<td>0: Unmask</td>
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<td>1: Mask</td>
</tr>
<tr>
<td>0</td>
<td>OCP_INT_MASK</td>
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## INT
Interrupt Status Register

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<th>DESCRIPTION</th>
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<tbody>
<tr>
<td>7:4</td>
<td>RESERVED</td>
<td>0000</td>
<td>Thermal Shutdown Interrupt Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No status change or status change from 1 to 0 for TSHDN</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Status change from 0 to 1 happened for TSHDN</td>
</tr>
<tr>
<td>3</td>
<td>THM_INT</td>
<td>0</td>
<td>Power-OK Interrupt Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No status change or status change from 1 to 0 for BB_POKn</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Status change from 1 to 0 happened for BB_POKn</td>
</tr>
<tr>
<td>2</td>
<td>POK_INT</td>
<td>0</td>
<td>OVP Interrupt Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No status change or status change from 1 to 0 for BB_OVP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Status change from 0 to 1 happened for BB_OVP</td>
</tr>
<tr>
<td>1</td>
<td>OVP_INT</td>
<td>0</td>
<td>OCP Interrupt Bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: No status change or status change from 1 to 0 for BB_OCP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Status change from 0 to 1 happened for BB_OCP</td>
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### Ordering Information

<table>
<thead>
<tr>
<th>PART</th>
<th>GPIO DEFAULT TYPE</th>
<th>GPIO DEFAULT FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAX77816AEWP+T</td>
<td>Input</td>
<td>FPWM Mode Enable</td>
</tr>
<tr>
<td>MAX77816BEWP+T*</td>
<td>Input</td>
<td>Inductor Peak Current-Limit Selection</td>
</tr>
<tr>
<td>MAX77816CEWP+T*</td>
<td>Input</td>
<td>Output Voltage Selection</td>
</tr>
<tr>
<td>MAX77816DEWP+T*</td>
<td>Output</td>
<td>Power-OK Status Indication</td>
</tr>
<tr>
<td>MAX77816EEWP+T*</td>
<td>Output</td>
<td>Interrupt Indication</td>
</tr>
</tbody>
</table>

*Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

*Future product—Contact Maxim for availability.

### Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

<table>
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<th>PACKAGE CODE</th>
<th>OUTLINE NO.</th>
<th>LAND PATTERN NO.</th>
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<tbody>
<tr>
<td>20 WLP</td>
<td>W201F2+1</td>
<td>21-0771</td>
<td>Refer to Application Note 1891</td>
</tr>
</tbody>
</table>

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Revision History

<table>
<thead>
<tr>
<th>REVISION NUMBER</th>
<th>REVISION DATE</th>
<th>DESCRIPTION</th>
<th>PAGES CHANGED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>6/17</td>
<td>Initial release</td>
<td></td>
</tr>
</tbody>
</table>

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