Hitachi Global Storage Technologies

HITACHI
Inspire the Next

Hard Disk Drive Specification
Hitachi Travelstar 5K100

2.5 inch ATA/IDE hard disk drive

Models: HTS541010G9AT00
HTS541080G9AT00
HTS541060G9AT00
HTS541040G9AT00
HTS541020G9AT00

Revision 1.4

11 July 2006

Hitachi Global Storage Technologies

HITACHI
Inspire the Next

Hard Disk Drive Specification
Hitachi Travelstar 5K100

2.5 inch ATA/IDE hard disk drive

Models: HTS541010G9AT00
HTS541080G9AT00
HTS541060G9AT00
HTS541040G9AT00
HTS541030G9AT00
HTS541020G9AT00

Revision 1.4 11 July 2006

1st Edition (Revision 1.0) (30 June 2004) Revised
2nd Edition (Revision 1.1) (23 December 2004) Revised
3rd Edition (Revision 1.2)(25 August 2005) Revised
4th Edition (Revision 1.3)(1 December 2005) Revised
5th Edition (Revision 1.4)(11 July 2006) Final

Table of contents

List of Tables

1.0 General

1.1 Introduction

This document describes the specifications of the following Travelstar 5K100, a 2.5-inch hard disk drive, ATA/IDE interface with a rotational speed of 5400 RPM and a height of 9.5 mm:

Drive name	Model number	Capacity	Height (mm)	Rotation Speed (rpm)
Travelstar 5K100-100	HTS541010G9AT00	100 GB	9.5	5,400
Travelstar 5K100-80	HTS541080G9AT00	80 GB	9.5	5,400
Travelstar 5K100-60	HTS541060G9AT00	60 GB	9.5	5,400
Travelstar 5K100-40	HTS541040G9AT00	40 GB	9.5	5,400
Travelstar 5K100-30	HTS541030G9AT00	30 GB	9.5	5,400
Travelstar 5K100-20	HTS541020G9AT00	20 GB	9.5	5,400

Part 1 of this document beginning on page 7 defines the hardware functional specification. Part 2 of this document beginning on page 57 defines the interface specification

These specifications are subject to change without notice.

1.2 References

ATA/ATAPI-6 (T13/1410D Revision 3b)

1.3 Abbreviations

Abbreviation	Meaning
32 KB	32 x 1024 bytes
64 KB	64 x 1024 bytes
A	Ampere
AC	alternating current
AT	Advanced Technology
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
C	Celsius
CSA	Canadian Standards Association
C-UL	Canadian-Underwriters Laboratory
Cyl	cylinder
DC	Direct Current
DFT	Drive Fitness Test
DMA	Direct Memory Access
ECC	error correction code

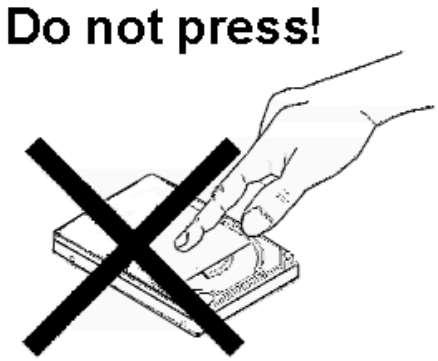
EEC	European Economic Community
EMC	electromagnetic compatibility
ERP	Error Recovery Procedure
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
FRU	field replacement unit
G	gravity (a unit of force)
G^2/Hz	$(32\ ft/sec)^2$ per Hertz
Gb	1,000,000,000 bits
GB	1,000,000,000 bytes
GND	ground
h	hexadecimal
HDD	hard disk drive
Hz	Hertz
I	Input
ILS	integrated lead suspension
I/O	Input/Output
ISO	International Standards Organization
KB	1,000 bytes
Kbpi	1000 bits per inch
kgf-cm	kilogram (force)-centimeter
KHz	kilohertz
LBA	logical block addressing
Lw	unit of A-weighted sound power
m	meter
max	maximum
MB	1,000,000 bytes
Mbps	1,000,000 bits per second
MHz	megahertz
MLC	Machine Level Control
mm	millimeter
ms	millisecond
us, ms	microsecond
No	number
O	Output
OD	Open Drain Programmed Input/Output
PIO	Programmed Input/Output
POH	power on hours
Pop	population
P/N	part number
p-p	peak-to-peak
PSD	power spectral density
RES	radiated electromagnetic susceptibility

RFI	radio frequency interference
RH	relative humidity
% RH	per cent relative humidity
RMS	root mean square
RPM	revolutions per minute
RST	reset
R/W	read/write
sec	second
SELV	secondary low voltage
S.M.A.R.T	Self-Monitoring, Analysis, and Reporting Technology
TPI	tracks per inch
Trk	track
TTL	transistor-transistor logic
UL	Underwriters Laboratory
V	volt
VDE	Verband Deutscher Electrotechniker
W	watt
3-state	transistor-transistor tristate logic

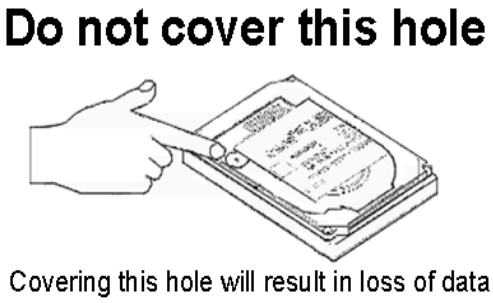
1.4 Caution

- Do not apply force to the top cover (See figure below).
- Do not cover the breathing hole on the top cover (See figure below).
- Do not touch the interface connector pins or the surface of the printed circuit board
- This drive can be damaged by electrostatic discharge (ESD). Any damages incurred to the drive after its removal from the shipping package and the ESD protective bag are the responsibility of the user.

1.5 Drive handling precautions



Do not press on the drive cover during handling.



2.0 Outline of the drive

- 2.5 inch, 9.5-mm height
- Formatted capacities of 100 GB, 80 GB, 60 GB, 40 GB, 30GB, 20 GB
- 512 bytes/sector
- AT Interface (Enhanced IDE) conforming to ATA/ATAPI-6
- Integrated controller
- No-ID recording format
- Coding : 100/106
- Multi zone recording
- Enhanced ECC On-The-Fly
    - 10 bit 40 symbol non Interleaved Read Solomon code
    - Non interleave On-The-Fly correction
    - Included 2 symbol system ECC
- Segmented Buffer with write cache –8192 KB (Upper 417 KB is used for firmware)
- Fast data transfer rate – up to 100 MB/s
- Media data transfer rate (max): 493 Mb/s
- Average seek time: 12 ms for read
- Closed-loop actuator servo (Embedded Sector Servo)
- Rotary voice coil motor actuator
- Load/Unload mechanism
- Mechanical latch
    - 0.65 Watts at idle state
- Adaptive power save control - 0.65 Watts at idle state
- Power on to ready - 3.5 sec
- Operating shock:
    - 2940 m/sec^2 (300 G)/2ms
    - 1568 m/sec^2 (160G)/1ms
- Non-operating shock: 9810 m/sec^2 (1000 G) 1ms

Part 1. Functional specification

3.0 Fixed-disk subsystem description

3.1 Control electronics

The control electronics works with the following functions:

- AT Interface Protocol
- Embedded Sector Servo
- No-ID (TM) formatting
- Multizone recording
- Code: 100/106
- System ECC
- Enhanced Adaptive Battery Life Extender

3.2 Head disk assembly data

The following technologies are used in the drive:

- Pico Slider
- Textured laminated AFC glass disk
- GMR head
- Integrated lead suspension (ILS)
- Load/unload mechanism
- Mechanical latch

4.0 Drive characteristics

4.1 Formatted capacity

Table 1: Formatted capacities

	100GB	**80GB**	**60GB**	**40GB**	**30GB**	**20GB**
Physical Layout						
Bytes per sector	512	512	512	512	512	512
Sectors per track	440-891	429-880	429-880	429-880	400-880	429-880
Number of heads	4	4	3	2	1	1
Number of disks	2	2	2	1	1	1
Logical layout						
Number of heads	16	16	16	16	16	16
Number of Sectors/track	63	63	63	63	63	63
Number of Cylinders	16,383	16,383	16,383	16,383	16,383	16,383
Number of sectors	195,371,568	156,301,488	117,210,240	78,140,160	58,605,120	39,070,080
Total logical data bytes	100,030,242,816	80,026,361,856	60,011,642,880	40,007,761,920	30,005,821,440	20,003,880,960

4.2 Data sheet

Table 2: Data sheet

Rotational Speed [RPM]	5400	5400
Data transfer rates (buffer to/from media) (Mbps)	493	493
Data transfer rates ULTRA DMA 100 (Mbyte/sec)	100	
Recording density (Kbit/mm) (Max Typ)	30.1	28.2
(KBPI) (Max Typ)	764	717
Track density (track/mm) (Typ)	4457	3803
(KTPI) (Typ)	113.2	96.6
Areal density (Mbit/sq-mm - Max)	134	107
(Gbit/sq-inch - Max)	86	70
Number of zones	24	24

4.3 Cylinder allocation

Data format is allocated by each characteristics in 3 different Adaptive formats described below.

Table 3: Cylinder allocation (40 Bp/ format)

40 B/p format		
Zone	**Cylinders**	**Sectors/Track**
Data Zone 0	0 - 4,211	880
Data Zone 1	4,212 - 8,423	858
Data Zone 2	8,424 - 10,607	858
Data Zone 3	10,608 - 13,727	825
Data Zone 4	13,728 - 17,159	814
Data Zone 5	17,160 - 19,031	814
Data Zone 6	19,032 - 22,151	792
Data Zone 7	22,152 - 24,335	770
Data Zone 8	24,336 - 26,675	759
Data Zone 9	26,676 - 29,015	748
Data Zone 10	29,016 - 32,759	726
Data Zone 11	32,760 - 34,319	726
Data Zone 12	34,320 - 38,219	693
Data Zone 13	38,220 - 40,559	682
Data Zone 14	40,560 - 44,615	660
Data Zone 15	44,616 - 47,579	638
Data Zone 16	47,580 - 50,699	616
Data Zone 17	50,700 - 54,719	594
Data Zone 18	54,288 - 57,719	572
Data Zone 19	57,720 - 61,151	550
Data Zone 20	61,152 - 65,207	528
Data Zone 21	65,208 - 66,923	495
Data Zone 22	66,924 - 68,483	484
Data Zone 23	68,484 - 71,759	462

Table 4: Cylinder allocation (50 B/p format)

Data Zone 0	0 - 3,839	858
Data Zone 1	3,840 - 6,527	836
Data Zone 2	6,528 - 9,727	825
Data Zone 3	9,728 - 12,159	814
Data Zone 4	12,160 - 15,359	792
Data Zone 5	15,360 - 17,663	792
Data Zone 6	17,664 - 19,327	759
Data Zone 7	19,328 - 21,503	748
Data Zone 8	21,504 - 23,295	748
Data Zone 9	23,296 - 25,471	726
Data Zone 10	25,472 - 26,879	726
Data Zone 11	26,880 - 28,159	704
Data Zone 12	28,160 - 30,207	693
Data Zone 13	30,208 - 31,487	682
Data Zone 14	31,488 - 34,943	660
Data Zone 15	34,944 - 37,119	638
Data Zone 16	37,120 - 39,935	616
Data Zone 17	39,936 - 43,135	594
Data Zone 18	43,136 - 45,951	572
Data Zone 19	45,952 - 47,231	561
Data Zone 20	47,232 - 51,071	528
Data Zone 21	51,072 - 53,887	495
Data Zone 22	53,888 - 56,831	462
Data Zone 23	56,832 - 58,879	440

4.4 Performance characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical head positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (read ahead/write cache)

Note: All the above parameters contribute to drive performance. There are other parameters that contribute to the performance of the actual system. This specification defines the essential characteristics of the drive. It does not include system throughput which is dependent on the system and the application.

The following table gives a typical value for each parameter. The detailed descriptions are found in Section 5.0, “Data integrity” beginning on page 19.

Table 5: Performance characteristics

Function	
Average random seek time - read (ms)	12
Average random seek time - write (ms)	14
Rotational speed (RPM)	5400
Power-on-to-ready (sec)	3.5
Command overhead (ms)	1.0
Disk-buffer data transfer (Mb/s)	493 max
Buffer-host data transfer (Mb/s)	100

4.4.1 Command overhead

Command overhead time is defined as the interval from the time that a drive receives a command to the time that the actuator starts its motion

4.4.2 Mechanical positioning

4.4.2.1 Average seek time (including settling)

Table 6: Mechanical positioning performance

Command type	Typical (ms)	Max (ms)
Read	12	14
Write	13	15

“Typical” and “Max” are used throughout this document and are defined as follows:

Typical Average of the drive population tested at nominal environmental and voltage conditions.

Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See Section 6.1, “Environment” on page 23 and Section 6.2, “DC power requirements” on page 25 for ranges.)

The seek time is measured from the start of the actuator’s motion to the start of a reliable read or write operation. A reliable read or write implies that error correction or recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max} (Max+1-n)(Tn_{in} + Tn_{out})}{(max + 1)(max)}$$

where

max = maximum seek length
n = seek length (1 to max)
Tnin = inward measured seek time for an n track seek
Tnout = outward measured seek time for an n track seek

4.4.2.2 Full stroke seek time

Table 7: Full stroke seek time

Command type	Typical (ms)	Max (ms)
Read	23.0	30.0
Write	24.0	31.0

Full stroke seek is measured as the average of 1,000 full stroke seeks.

4.4.2.3 Single track seek time (without command overhead, including settling)

Table 8: Single track seek time

Command type	Typical (ms)	Max (ms)
Read	2.5	4.0
Write	3.0	4.5

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

4.4.2.4 Average latency

Table 9: Average latency

Rotational speed (RPM)	Time for one revolution (ms)	Average latency (ms)
5400	11.1	5.5

4.4.2.5 Drive ready time

Table 10: Drive ready time

Condition	Drive ready time (sec)	
	Typical	Max
Power on to Ready	3.5	9.5

Ready	The condition in which the drive is able to perform a media access command (for example – read, write) immediately.
Power on to Ready	This includes the time required for the internal self diagnostics.

4.4.3 Operating modes

4.4.3.1 Description of operating modes

Table 11: Description of operating modes

Operating mode	Description
Spin-up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Performance Idle	The device is capable of responding immediately to idle media access requests. All electronic components remain powered and the full frequency servo remains operational.
Active idle	The device is capable of responding immediately to media access requests. Some circuitry—including servo system and R/W electronics—is in power saving mode. The head is parked near the mid-diameter the disk without servoing. A device in Active idle mode may take longer to complete the execution of a command because it must activate that circuitry.
Low power idle	The head is unloaded onto the ramp position. The spindle motor is rotating at full speed.

Table 11: Description of operating modes

Operating mode	Description
Standby	The device interface is capable of accepting commands. The spindle motor is stopped. All circuitry except the host interface is in power saving mode. The execution of commands is delayed until the spindle becomes ready.
Sleep	The device requires a soft reset or a hard reset to be activated. All electronics, including spindle motor and host interface, are shut off.

4.4.3.2 Mode transition time - from Standby to Idle

Table 12: Drive ready time

From	To	Transition Time (typ)	Transition Time (max.)
Standby	Idle	2.5	9.5

4.4.3.3 Operating mode at power on

The device goes into Idle mode after power on or hard reset as an initial state. Initial state may be changed to Standby mode using pin C on the interface connector. Refer to section 7.10, “Drive address setting” on page 55 for details.

4.4.3.4 Adaptive power save control

The transient timing from Performance Idle mode to Active Idle mode and Active Idle mode to Low Power Idle mode is controlled adaptively according to the access pattern of the host system. The transient timing from Low Power Idle mode to Standby mode is also controlled adaptively, if it is allowed by Set Features Enable Advanced Power Management subcommand.

5.0 Data integrity

5.1 Data loss at power off

- Data loss will not be caused by a power off during any operation except the write operation.
- A power off during a write operation causes the loss of any received or resident data that has not been written onto the disk media.
- A power off during a write operation might make a maximum of one sector of data unreadable. This state can be recovered by a rewrite operation.

5.2 Write Cache

When the write cache is enabled, the write command may complete before the actual disk write operation finishes. This means that a power off, even after the write command completion, could cause the loss of data that the drive has received but not yet written onto the disk.

In order to prevent this data loss, confirm the completion of the actual write operation prior to the power off by issuing a

- Soft reset
- Hard reset
- Flush Cache command
- Standby command
- Standby Immediate command
- Sleep command

Confirm the command's completion.

5.3 Equipment status

The equipment status is available to the host system whenever the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- the access recalibration/tuning is complete
- the spindle speed meets requirements for reliable operations
- the self-check of drive is complete

The appropriate error status is made available to the host system if any of the following conditions occur after the drive has become ready:

- The spindle speed lies outside the requirements for reliable operation
- The occurrence of a Write Fault condition

5.4 WRITE safety

The drive ensures that the data is written into the disk media properly. The conditions listed below are monitored during a write operation. When one of these conditions exceeds the criteria, the write operation is terminated and the automatic retry sequence is invoked.

- Head off track
- External shock
- Low supply voltage
- Spindle speed out of tolerance
- Head open/short

5.5 Data buffer test

The data buffer is tested at power on reset and when a drive self-test is requested by the host. The test consists of a write/read '00'x and 'ff'x pattern on all buffers.

5.6 Error recovery

Errors occurring on the drive are handled by the error recovery procedure.

Errors that are uncorrectable after application of the error recovery procedures are reported to the host system as non-recoverable errors.

5.7 Automatic reallocation

The sectors that show some errors may be reallocated automatically when specific conditions are met. The drive does not report any auto reallocation to the host system. The conditions for auto reallocation are described below.

5.7.1 Nonrecovered write errors

When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sectors are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

5.7.2 Nonrecoverable read error

When a read operation fails after ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the required criteria, this sector is reallocated.

5.7.3 Recovered read errors

When a read operation for a sector fails and is recovered at the specific ERP step, the sector is reallocated automatically. A media verification sequence may be run prior to the reallocation according to the predefined conditions.

5.8 ECC

The 10 bit 40 symbol non interleaved ECC processor provides user data verification and correction capability. The first 6 symbol of ECC are 4 check symbols for user data and the 2 symbol system ECC. The other 34 symbols are Read Solomon ECC. Hardware logic corrects up to 16 symbols (20 bytes) errors on-the-fly.

2 symbol System ECC is generated when HDC receives user data from HOST, and can correct up to 1 symbol (10 bit) error on-the-fly when one transfers to HOST.

6.0 Specification

6.1 Environment

6.1.1 Temperature and humidity

Table 13: Environmental condition

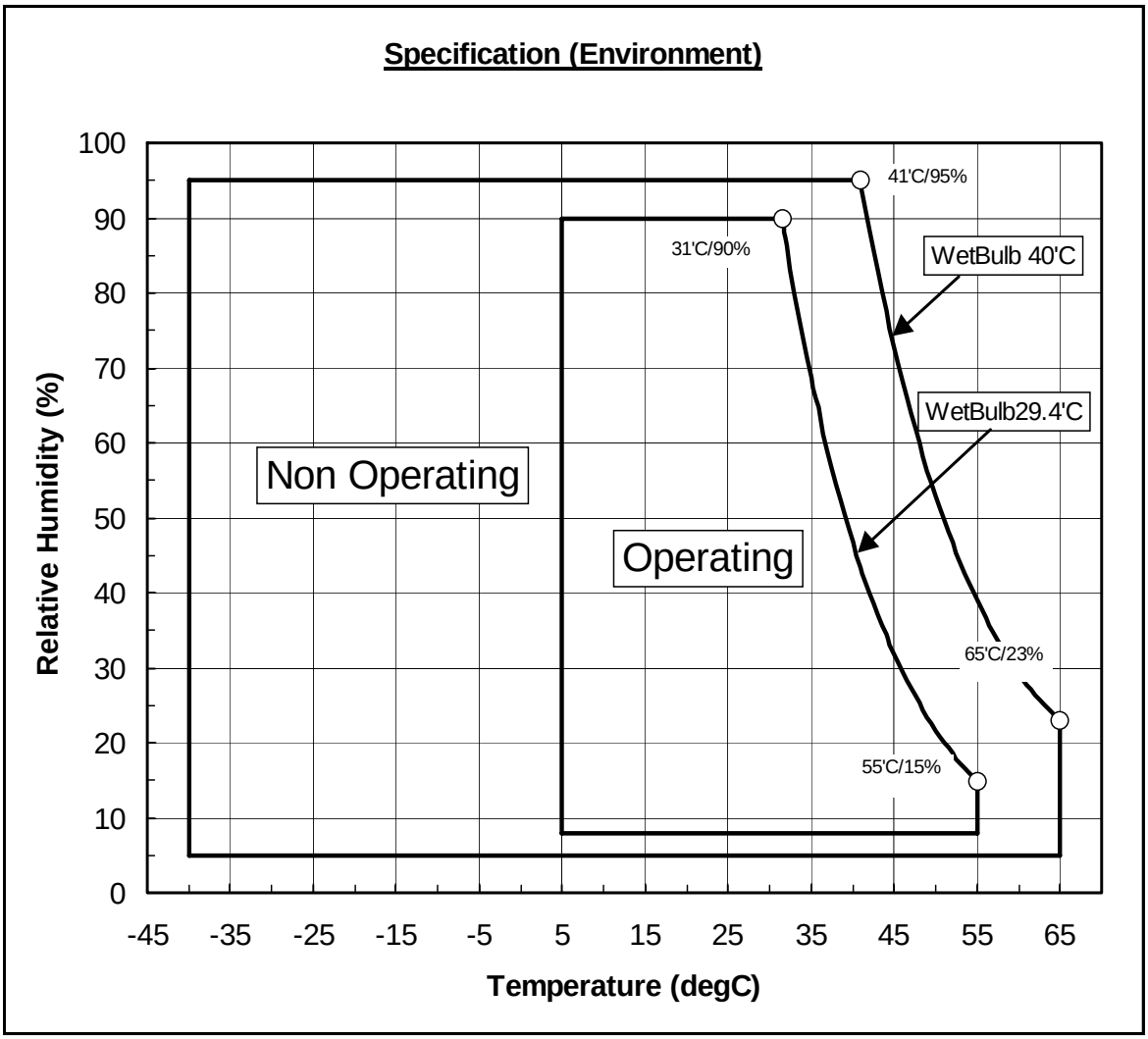
Operating conditions	
Temperature	5 to 55ºC (See note below)
Relative humidity	8 to 90%, non-condensing
Maximum wet bulb temperature	29.4ºC, non-condensing
Maximum temperature gradient	20ºC/hour
Altitude	–300 to 3,048 m (10,000 ft)
Non-operating conditions	
Temperature	–40 to 65ºC
Relative humidity	5 to 95%, non-condensing
Maximum wet bulb temperature	40ºC, non-condensing
Maximum temperature gradient	20ºC/hour
Altitude	–300 to 12,192 m (40,000 ft)

Notes:

The system is responsible for supplying sufficient ventilation to maintain a surface temperature below 60ºC at the center of the top cover of the drive and below 63°C at the center of the drive circuit board assembly.

The maximum storage period in the shipping package is one year.

Table 14: Limits of temperature and humidity



6.1.1.1 Corrosion test

The drive must be functional and show no signs of corrosion after being exposed to a temperature humidity stress of 50°C/90% RH (relative humidity) for one week followed by a temperature and humidity drop to 25°C/40%RH in 2 hours.

6.1.2 Radiation noise

The drive shall work without degradation of the soft error rate under the following magnetic flux density limits at the enclosure surface.

Table 15: Magnetic flux density limits

Frequency (KHz)	Limits (uT RMS)
0–60	500
61–100	250
101–200	100
201–400	50

6.1.3 Conductive noise

The disk drive shall work without soft error degradation in the frequency range from DC to 20 Mhz injected through any two of the mounting screw holes of the drive when an AC current of up to 45 mA (p-p) is applied through a 50-ohm resistor connected to any two mounting screw holes.

6.1.4 Magnetic fields

The disk drive will withstand radiation and conductive noise within the limits shown below. The test method is defined in the Noise Susceptibility Test Method specification, P/N 95F3944.

6.2 DC power requirements

Connection to the product should be made in a safety extra low voltage (SELV) circuits. The voltage specifications are applied at the power connector of the drive.

Table 16: DC power requirements

Item	Requirements
Nominal supply	+5Volt DC
Supply voltage	–0.3 Volt to 6.0 Volt
Power supply ripple (0–20 MHz) [1]	100mV p-p max.
Tolerance[2]	±5%
Supply rise time	1 - 100 ms

Watts (RMS typical)	All models
Performance Idle average[3]	2.0

Watts (RMS typical)	All models
Active Idle average	1.1
Low Power Idle average	0.65
Read average [4]	2.0
Write average	2.0
Seek average [5]	2.5
Standby	0.2
Sleep	0.1
Startup (max. peak) [6]	5.0
Average from power on to ready	3.8

Footnotes:

[1] The maximum fixed disk ripple is measured at the 5 volt input of the drive.

[2] The disk drive shall not incur damage for an over voltage condition of +25% (maximum duration of 20 ms) on the 5 volt nominal supply.

[3] The idle current is specified at an inner track.

[4] The read/write current is specified based on three operations of 63 sector read/write per 100 ms.

[5] The seek average current is specified based on three operations per 100 ms.

[6] The worst case operating current includes motor surge.

6.2.1 Power consumption efficiency

Table 17: Power consumption efficiency

Capacity	Power Consumption Efficiency (Watts/GB)
100GB	0.007
80GB	0008
60GB	0.011
40GB	0.016
30GB	0.022
20GB	0.033

Note: Power consumption efficiency is calculated as Power Consumption of Low Power Idle in Watts/Capacity (GB).

6.3 Reliability

6.3.1 Data Reliability

- Probability of not recovering data is 1 in 10^{13} bits read
- ECC implementation

On-the-fly correction performed as a part of read channel function recovers up to 16 symbols of error in one sector (1 symbol is 10 bits).

6.3.2 Failure prediction (S.M.A.R.T.)

The drive supports the Self-Monitoring, Analysis and Reporting Technology (S.M.A.R.T.) function. The details are described in Section 11.9, “S.M.A.R.T. Function” on page 77 and Section 13.39, “S.M.A.R.T. Function Set (B0h)” on page 168.

6.3.3 Cable noise interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.3.4 Service life and usage condition

The drive is designed to be used under the following conditions:

- The drive should be operated within specifications of shock, vibration, temperature, humidity, altitude, and magnetic field.
- The drive should be protected from ESD.
- The breathing hole in the top cover of the drive should not be covered.
- Force should not be applied to the cover of the drive.
- The specified power requirements of the drive should be satisfied.
- The drive frame should be grounded electrically to the system through four screws.
- The drive should be mounted with the recommended screw depth and torque.
- The interface physical and electrical requirements of the drive should satisfy ATA-6.
- The power-off sequence of the drive should comply with the required power off sequence described in Section 6.3.6.2, “Required Power-Off Sequence” on page 28.

Service life of the drive is approximately 5 years or 20,000 power on hours, which comes first, under the following assumptions:

- Less than 333 power on hours per month.
- Seeking/Writing/Reading operation is less than 20% of power on hours.

This does not represent any warranty or warranty period. Applicable warranty and warranty period are covered by the purchase agreement.

6.3.5 Preventive maintenance

None

6.3.6 Load/unload

The product supports a minimum of 600,000 normal load/unloads.

Load/unload is a functional mechanism of the hard disk drive. It is controlled by the drive micro code. Specifically, unloading of the heads is invoked by the following commands:

- Hard reset
- Standby

- Standby immediate
- Sleep

Load/unload is also invoked as one of the idle modes of the drive.

The specified start/stop life of the product assumes that load/unload is operated normally, not in emergency mode.

6.3.6.1 Emergency unload

When hard disk drive power is interrupted while the heads are still loaded, the micro code cannot operate and the normal 5-volt power is unavailable to unload the heads. In this case, normal unload is not possible. The heads are unloaded by routing the back EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

The drive supports a minimum of 20,000 emergency unloads.

6.3.6.2 Required Power-Off Sequence

The required BIOS sequence for removing power from the drive is as follows:

Step 1: Issue one of the following commands:

- Standby
- Standby immediate
- Sleep

Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload.

Step 2: Wait until the Command Complete status is returned
In a typical case 350 ms are required for the command to finish completion; however, the BIOS time out value needs to be 30 seconds considering error recovery time. Refer to Section 14.0, “Timings” on page 203.

Step 3: Terminate power to the drive
This power-down sequence should be followed for entry into any system power-down state, system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios, such as battery removal during operation.

6.3.6.3 Power Switch design considerations

In systems that use this drive consideration should be given to the design of the system power switch.

Hitachi recommends that the switch operate under control of the BIOS rather than be hardwired. The same recommendation is made for cover-close switches. When a hardwired switch is turned off, emergency unload occurs, as well as the problems cited in Section 5.1, “Data loss at power off” on page 19 and Section 5.2, “Write Cache” on page 19.

6.3.6.4 Test considerations

Start/stop testing is classically performed to verify head/disk durability. The heads do not land on the disk, therefore this type of test should be viewed as a test of the load/unload function.

Start/Stop testing should be done by commands through the interface, not by power cycling the drive. Simple power cycling of the drive invokes the emergency unload mechanism and subjects the HDD to nontypical mechanical stress.

Power cycling testing may be required to test the boot-up function of the system. In this case Hitachi recommends that the power-off portion of the cycle contain the sequence specified in Section 6.3.6.2, “Required Power-Off Sequence” on page 28. If this is not done, the emergency unload function is invoked and nontypical stress results.

6.4 Mechanical specifications

6.4.1 Physical dimensions and weight

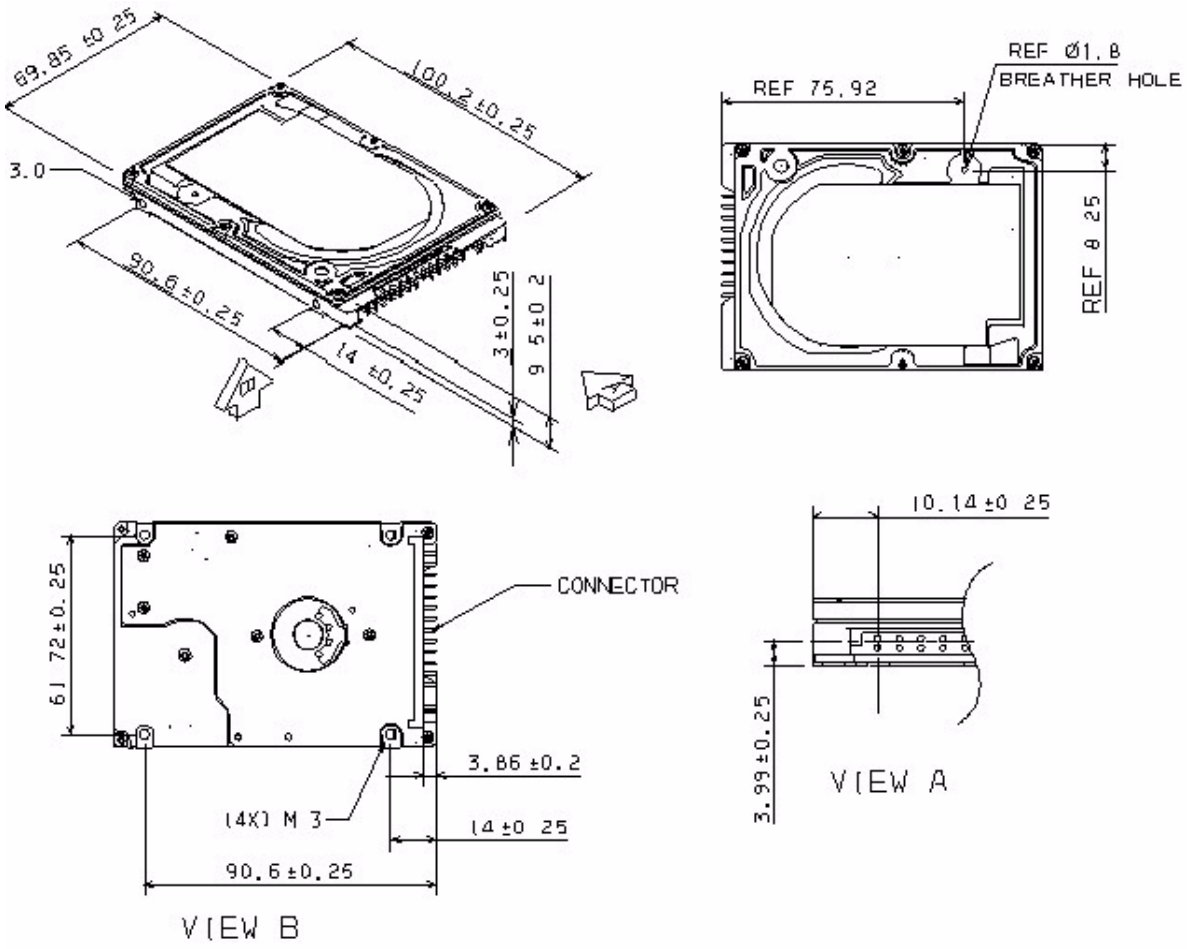
The following table lists the dimensions of the drive.

Table 18: Physical dimensions and weight

	100GB, 80GB, 60GB models	**40GB, 30GB, 20GB models**
Height [mm]	9.5±0.2	9.5±0.2
Width [mm]	69.85±0.25	69.85±0.25
Length [mm]	100.2±0.25	100.2±0.25
Weight [grams - maximum]	102	95

6.4.2 Mounting hole locations

The mounting hole locations and size of the drive are shown below.



6.4.3 Connector and jumper description

A jumper is used to designate the drive address as either master or slave. The jumper setting method is described in Section 7.10, “Drive address setting” on page 55.

Connector specifications are included in Section 7.2, “Interface connector” on page 39.

6.4.4 Mounting orientation

The drive will operate in all axes (six directions) and will stay within the specified error rates when tilted ±5degrees from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting screw torque is 3.0±0.5 kgf-cm.

The recommended mounting screw depth is 3.0±0.3 mm for bottom and 3.5±0.5 mm for horizontal mounting.

The user is responsible for using the appropriate screws or equivalent mounting hardware to mount the drive securely enough to prevent excessive motion or vibration of the drive at seek operation or spindle rotation.

6.4.5 Load/unload mechanism

The head load/unload mechanism is provided to protect the disk data during shipping, movement, or storage. Upon power down, a head unload mechanism secures the heads at the unload position. See Section 6.5.4, “Nonoperating shock” on page 34 for additional details.

6.5 Vibration and shock

All vibration and shock measurements in this section are for drives without mounting attachments for systems. The input level shall be applied to the normal drive mounting points.Vibration tests and shock tests are to be conducted by mounting the drive to a table using the bottom four mounting holes.

6.5.1 Operating vibration

The drive will operate without a hard error while being subjected to the following vibration levels.

6.5.1.1 Random vibration

The test consists of 30 minutes of random vibration using the power spectral density (PSD) levels below. The vibration test level is 6.57 m/sec^2 RMS (Root Mean Square) (0.67 G RMS).

Table 19: Random vibration PSD profile breakpoints (operating)

Random vibration PSD profile breakpoint	
Hz	**m x 10n (m^2/sec^4)/Hz**
5	1.9 x E–3
17	1.1 x E–1
45	1.1 x E–1
48	7.7 x E–1
62	7.7 x E–1
65	9.6 x E–2
150	9.6 x E–2
200	4.8x E–2
500	4.8 x E–2

6.5.1.2 Swept sine vibration

Table 20: Swept sine vibration

Swept sine vibration (zero to peak 5 to 500 to 5 Hz sine wave)	**Sweep rate (oct/min)**
9.8 m/sec^2 (1 G) (5-500 Hz)	1.0

6.5.2 Nonoperating vibration

The disk drive withstands the vibration levels described below without any loss or permanent damage.

6.5.2.1 Random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes for a duration of 15 minutes per axis. The PSD levels for the test simulating the shipping and relocation environment is shown below.

Table 21: Random Vibration PSD Profile Breakpoints (nonoperating)

Hz	(m2/sec4)/Hz
2.5	0.096
5	2.88
40	1.73
500	1.73

Note: Overall RMS (root mean square) level of vibration is 29.50 m/sec^2 (3.01 G).

6.5.2.2 Swept sine vibration

- 49 m/sec^2 (5 G) (zero-to-peak), 5 to 500 to 10 Hz sine wave
- 0.5 oct/min sweep rate
- 25.4 mm (peak-to-peak) displacement, 5 to 10 to 5 Hz

6.5.3 Operating shock

The hard disk drive meets the criteria in the table below while operating under these conditions:

- The shock test consists of 10 shock inputs in each axis and direction for a total of 60.
- There must be a minimum delay of 3 seconds between shock pulses.
- The disk drive will operate without a hard error while subjected to the following half-sine shock pulse

Table 22: Operating shock

Duration of 1 ms	Duration of 2 ms	Duration of 11 ms
1568 m/sec^2 (160 G)	2940 m/sec^2 (300 G)	147 m/sec^2 (15 G)

The input level shall be applied to the normal disk drive subsystem mounting points used to secure the drive in a normal system.

6.5.4 Nonoperating shock

The drive withstands the following half-sine shock pulse without any data loss or permanent damage.

Table 23: Nonoperating shock

Duration of 1 ms	Duration of 11 ms
9800 m/sec^2 (1000 G)	1470 m/sec^2 (150 G)

The shocks are applied for each direction of the drive for three mutually perpendicular axes, one axis at a time. Input levels are measured on a base plate where the drive is attached with four screws

6.6 Acoustics

6.6.1 Sound power levels

The criteria of A-weighted sound power level are described below.

Measurements are to be taken in accordance with ISO 7779. The mean of the sample of 40 drives is to be less than the typical value. Each drive is to be less than the maximum value. The drives are to meet this requirement in both board down orientations.

Table 24: Weighted sound power

		A-weighted sound power	
		Typical (Bels)	**Maximum (Bels)**
100GB, 80GB, 60GB models	Idle	2.5	2.7
	Operating	2.7	2.9
40GB, 30GB, 20GB models	Idle	2.2	2.4
	Operating	2.4	2.6

The background power levels of the acoustic test chamber for each octave band are to be recorded.

Sound power tests are to be conducted with the drive supported by spacers so that the lower surface of the drive be located 25±3 mm above from the chamber floor. No sound absorbing material shall be used.

The acoustical characteristics of the disk drive are measured under the following conditions:

Mode definitions

- **Idle mode:** Power on, disks spinning, track following, unit ready to receive and respond to control line commands.
- **Operating mode:** Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is calculated with the following formula:

$$Ns = 0.4/(Tt + T1)$$

where:

Ns = average seek rate in seeks/s
Tt = published seek time from one random track to another without including rotational latency
T1= equivalent time in seconds for the drive to rotate by half a revolution

6.6.2 Discrete tone penalty

Discrete tone penalties are added to the A-weighted sound power (Lw) with the following formula only when determining compliance.

$$Lwt(spec) = Lw = 0.1Pt + 0.3 < 4.0 \text{ (Bels)}$$

where

Lw = A-weighted sound power level
Pt = Value of desecrate tone penalty = dLt – 6.0(dBA)
dLt = Tone-to-noise ratio taken in accordance with ISO 7779 at each octave band

6.7 Identification labels

The following labels are affixed to every drive:

- A label which is placed on the top of the head disk assembly containing the statement "Made by Hitachi" or equivalent, part number, EC number, and FRU number.
- A bar code label which is placed on the disk drive based on user request. The location on the disk drive is to be designated in the drawing provided by the user.
- Labels containing the vendor's name, disk drive model number, serial number, place of manufacture, and UL/CSA logos.
- Labels containing jumper information if required by the customer.

6.8 Electromagnetic compatibility

When installed in a suitable enclosure and exercised with a random accessing routine at the maximum data rate, the drive meets the worldwide EMC requirements listed below:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15
- RFI Japan VCCI, Requirements of Hitachi products
- EU EMC Directive, Technical Requirements and Conformity Assessment Procedures

6.8.1 CE mark

The product is certified for compliance with EC directive 89/336/EEC. The EC marking for the certification appears on the drive.

6.8.2 C-TICK mark

The drive complies with the Australian EMC standard "Limits and methods of measurement of radio disturbance characteristics of information technology equipment, AS/NZS 3548:1995 Class B.

6.8.3 BSMI mark

The product complies with the Taiwan EMC standard "Limits and methods of measurement of radio disturbance characteristics of information technology equipment, CNS 13438 Class B."

6.8.4 MIC mark

The product complies with the Korea EMC standard. The regulation for certification of information and communication equipment is based on "Telecommunications Basic Act" and "Radio Waves Act". Korea EMC requirement are based technically on CISPR22:1993-12 measurement standards and limits. MIC standards are likewise based on IEC standards.

6.9 Safety

The drive complies with the safety standards of different countries as listed below.

6.9.1 UL and CSA approval

The drive is qualified per UL (Underwriters Laboratory) 60950 Third Edition (2000) and CAN/CSA C22.2 No.60950-1 Third Edition, for use in Information Technology Equipment, including Electric Business Equipment. The UL Recognition or the CSA certification is maintained for the product life. The UL and C-UL recognition mark or the CSA monogram for CSA certification appears on the drive.

6.9.2 IEC compliance

All models of the Travelstar 5K100 comply with IEC 60950-1999.

6.9.3 German safety mark

All models of the Travelstar 5K100 are approved by TUV on Test Requirement: EN60950:2000, but the GS mark has not been obtained.

6.9.4 Flammability

The printed circuit boards used in this drive are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. Except for small mechanical parts, all other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better.

6.9.5 Secondary circuit protection

This product utilizes printed circuit wiring that must be protected against the possibility of sustained combustion due to circuit or component failures as defined in C-B 2-4700-034 (Protection Against Combustion). Adequate secondary over current protection is the responsibility of the using system.

The user must protect the drive from its electrical short circuit problem. A 10 amp limit is required for safety purposes.

6.10 Packaging

Drives are packed in ESD protective bags and shipped in appropriate containers.

7.0 Electrical interface specification

7.1 Cabling

The maximum cable length from the host system to the hard disk drive plus circuit pattern length in the host system shall not exceed 18 inches.

7.2 Interface connector

The signal connector for AT attachment is designed to mate with Dupont part number 69764-044 or equivalent.

The figure below and “” on page 31 show the connector and pin location.

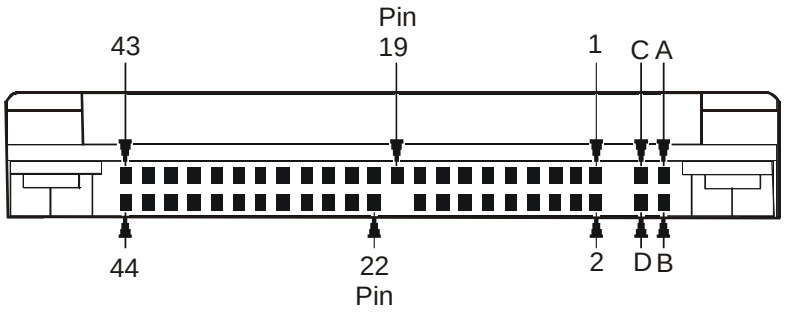


Figure 1 : Interface connector pin assignments

Figure 1: Interface connector pin assignments

Pin position 20 is left blank for correct connector insertion.

Pin positions A, B, C, and D are used for the drive address setting. (Refer to “” on page 55 for correct address setting.)

7.3 Signal definitions

The pin assignments of interface signals are listed as follows:Signal definitions

Table 25: Signal definitions

PIN	SIGNAL	I/O	Type		PIN	SIGNAL	I/O	Type
01	RESET-	I	TTL		02	GND		
03	DD07	I/O	3–state		04	DD08	I/O	3–state
05	DD06	I/O	3–state		06	DD09	I/O	3–state
07	DD05	I/O	3–state		08	DD10	I/O	3–state
09	DD04	I/O	3–state		10	DD11	I/O	3–state
11	DD03	I/O	3–state		12	DD12	I/O	3–state
13	DD02	I/O	3–state		14	DD13	I/O	3–state
15	DD01	I/O	3–state		16	DD14	I/O	3–state
17	DD00	I/O	3–state		18	DD15	I/O	3–state
19	GND				(20)	Key		
21	DMARQ	O	3–state		22	GND		
23	DIOW-(*)	I	TTL		24	GND		
25	DIOR-(*)	I	TTL		26	GND		
27	IORDY(*)	O	3–state		28	CSEL	I	TTL
29	DMACK-	I	TTL		30	GND		
31	INTRQ	O	3–state		32	reserved		
33	DA01	I	TTL		34	PDIAG-	I/O	OD
35	DA00	I	TTL		36	DA02	I	TTL
37	CS0-	I	TTL		38	CS1-	I	TTL
39	DASP-	I/O	OD		40	GND		
41	+ 5V logic	power			42	+ 5V motor	power	
43	GND				44	(reserved)		

O	designates an output from the drive
I	designates an input to the drive
I/O	designates an input/output common
OD	designates an Open-Drain output
power	designates a power supply to the drive
reserved	designates reserved pins which must be left unconnected

The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the host decides to allow a DMA burst, if the Ultra DMA transfer mode was previously chosen via SetFeatures. The drive becomes aware of this change upon assertion of the DMACK- line. These lines revert back to their original definitions upon the desertion of DMACK at the termination of the DMA burst.

Table 26: Special signal definitions for Ultra DMA

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	DDMARDY-	IORDY
	HSTROBE	DIOR-
	STOP	DIOW-
Read Operation	HDMARDY-	DIOR-
	DSTROBE	IORDY
	STOP	DIOW-

7.4 Signal descriptions

DD00–DD15

A 16-bit bi-directional data bus between the host and the drive. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00–15, are used for data transfer. These are 3-state lines with 16mA current sink capability.

DA00–DA02

These are addresses used to select the individual register in the drive.

CS0-

The chip select signal generated from the Host address bus. When active, one of the Command Block Registers [Data, Error (Features when written), Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status (Command when written) register] can be selected.

CS1-

The chip select signal generated from the Host address bus. When active, one of the Control Block Registers [Alternate Status (Device Control when written) and Drive Address register] can be selected.

RESET-

This line is used to reset the drive. It shall be kept at a Low logic state during power up and kept High thereafter.

DIOW-

The rising edge of this signal holds data from the data bus to a register or data register of the drive.

DIOR-

When this signal is low, it enables data from a register or data register of the drive onto the data bus. The data on the bus shall be latched on the rising edge of DIOR-

INTRQ

The interrupt is enabled only when the drive is selected and the host activates the IEN- bit in the Device Control Register. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. The IRQ is reset to zero by a host read of the status register or a write to the Command Register. This signal is a 3-state line with 16mA of sink capability.

DASP-

This is a time-multiplexed signal which indicates that a drive is active or that device 1 is present. This signal is driven by an Open-Drain driver and internally pulled up to 5.0 volts through a 10 k. resistor. During a Power-On initialization or after RESET- is negated, DASP- shall be asserted by device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450 ms for device 1 to assert DASP-. If device 1 is not present, device 0 may assert DASP- to drive an LED indicator on a host. The DASP- signal shall be negated following acceptance of the first valid command by device 1. Anytime after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

Caution

The host shall not drive DASP-. If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain VoH and VoL compatibility, given the IoH and IoL requirements of the DASP- device drivers.

Caution

When DASP- is negated, the line is in a high impedance state. The signal level may look less than 5.0V even though the line is pulled up to 5.0V through a resistor."

PDIAG-

This signal shall be asserted by device 1 to indicate to device 0 that it has completed the diagnostics. This line is pulled up to 3.3 volts in the drive through a 10 kΩ resistor.

Following a Power On Reset, software reset, or RESET-, drive 1 shall negate PDIAG- within 1 ms (to indicate to device 0 that it is busy). Drive 1 shall then assert PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status.

Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate PDIAG- within 1 ms to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert PDIAG-. Device 1 should clear BSY before asserting PDIAG-, as PDIAG- is used to indicate that device 1 has passed its diagnostics and is ready to post status. If DASP- was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics and clears the device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

CSEL (Cable Select)

This signal is monitored to determine the drive address (master or slave) when the jumper on the interface connector is at Position-3.

When CSEL is at ground or is at a low level, the drive works as a Master. If CSEL is open or is at a logical high level, the drive works as a Slave.

The signal level of CSEL to one drive should be different from the signal level to another drive on the same AT interface cable to avoid master-master or slave-slave configurations.

KEY

Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion.

IORDY

This signal is an indication to the host that the drive is ready to complete the current I/O cycle. This line is driven low at the falling edge of DIOR- or DIOW-when the drive needs some additional WAIT cycle(s) to

extend the PIO cycle. This line can be connected to the host IORDY signal in order to insert a WAIT state(s) into the host PIO cycle. This signal is an Open-Drain output with 16mA sink capability.

5V Power

There are two input pins for the +5 V power supply. One is the "+5 V Logic" input pin and the second is the "+5 V Motor" input pin. These two input pins are tied together within the drive.

DMACK-

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.
This signal is internally pulled up to 5 Volt through a 15kΩ resistor with a resistor tolerance value of –50% to +100%.

DMARQ

This signal is used for DMA data transfers between the host and drive. It shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by HIOR- and HIOW- signals. This signal is used in a handshake mode with DMACK-. This signal is a 3-state line with 24 mA sink capability and internally pulled down to GND through a 10 kΩ resistor.

HDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive. The signal HDMARDY- is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate HDMARDY- to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD (15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The STOP signal shall be asserted by the host prior to initiation of an Ultra DMA burst. A STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

DDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal DDMARDY- is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate DDMARDY- to pause an Ultra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

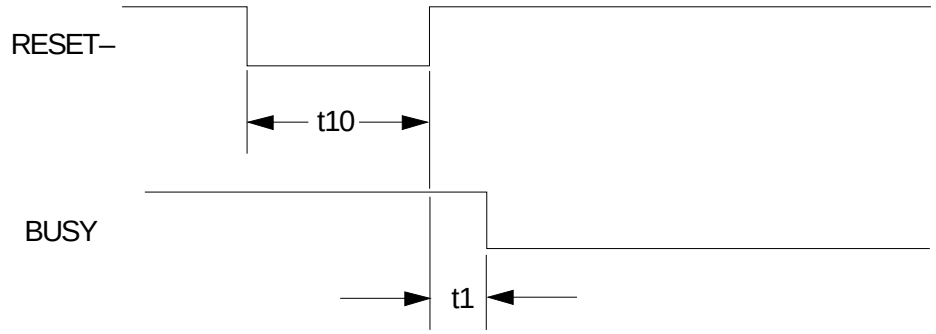
The signal DSTROBE is the data in strobe signal from the device for an Ultra DMA data in transfer. Both the rising and the falling edge of DSTROBE latch the data from DD (15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

7.5 Interface logic signal levels

The interface logic signals have the following electrical specifications:

Inputs	Voltage Input high (ViH)	2.0 V min./5.5 V max.
	Voltage input low (ViL)	–0.5 V min./0.8 V max.
Outputs	Voltage output high at IoH min (VoH)	2.4 V min.
	Voltage output low at IoL min (VoL)	0.5 V max.
Current	Driver Sink Current (IoL)	16mA min
	Driver Source Current (IoH)	400 µA min.

7.6 Reset timings



	PARAMETER DESCRIPTION	Min (µs)	Max (µs)
t1	RESET– high to Not BUSY	–	9.5
t10	RESET– low width	25	–

7.7 PIO timings

The PIO cycle timings meet Mode 4 of the ATA/ATAPI-6 description.

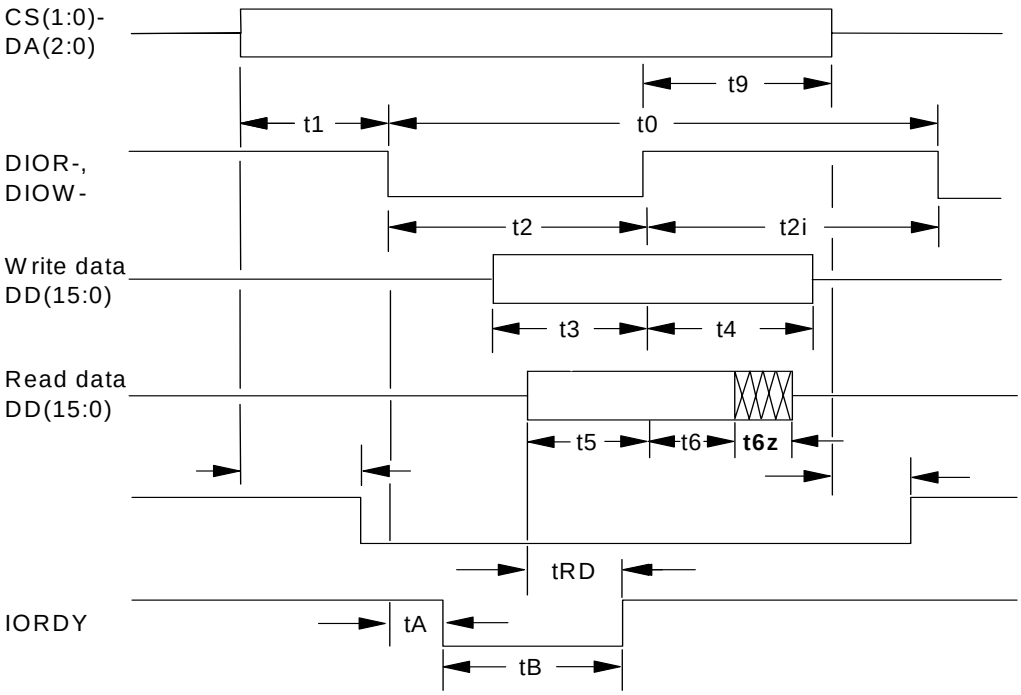


Table 27: PIO cycle timings

	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
t1	Address valid to DIOR-/DIOW- setup	25	–
t2	DIOR-/DIOW- pulse width	70	–
t2i	DIOR-/DIOW- recovery time	25	–
t3	DIOW- data setup	20	–
t4	DIOW- data hold	10	–
t5	DIOR- data setup	20	–
t6	DIOR- data hold	5	–
t6z	DIOR- data tristate	–	30
t9	DIOR-/DIOW- to address valid hold	10	–
tRD	Read data valid to IORDY active	0	–
tA	IORDY setup width	–	35
tB	IORDY pulse width	–	1,250

7.8 Multi word DMA timings

The Multi word DMA timings meet Mode 2 of the ATA/ATAPI-6 description.

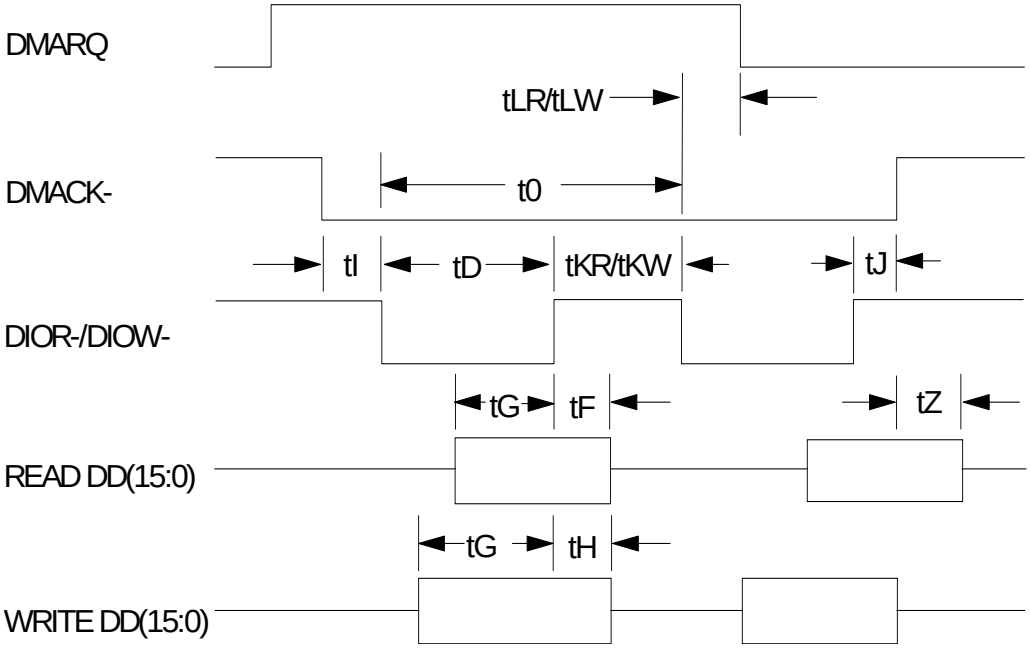


Table 28: Multiword DMA cycle timings

	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
tD	DIOR-/DIOW- asserted pulse width	70	–
tE	DIOR- data access	–	50
tF	DIOR- data hold	5	–
tG	DIOR-/DIOW- data setup	20	–
tH	DIOW- data hold	10	–
tI	DMACK- to DIOR-/DIOW- setup	0	–
tJ	DIOR-/DIOW- to DMACK- hold	5	–
tKR/tKW	DIOR- negated pulse width / DIOW- negated pulse width	25	–
tLR/tLW	DIOR- to DMARQ delay / DIOW- to DMARQ delay	–	35
tZ	DMACK- to read data released	–	25

7.9 Ultra DMA timings

The Ultra DMA timings meet Mode 0, 1, 2, 3, 4 and 5 of the Ultra DMA Protocol.

7.9.1 Initiating Read DMA

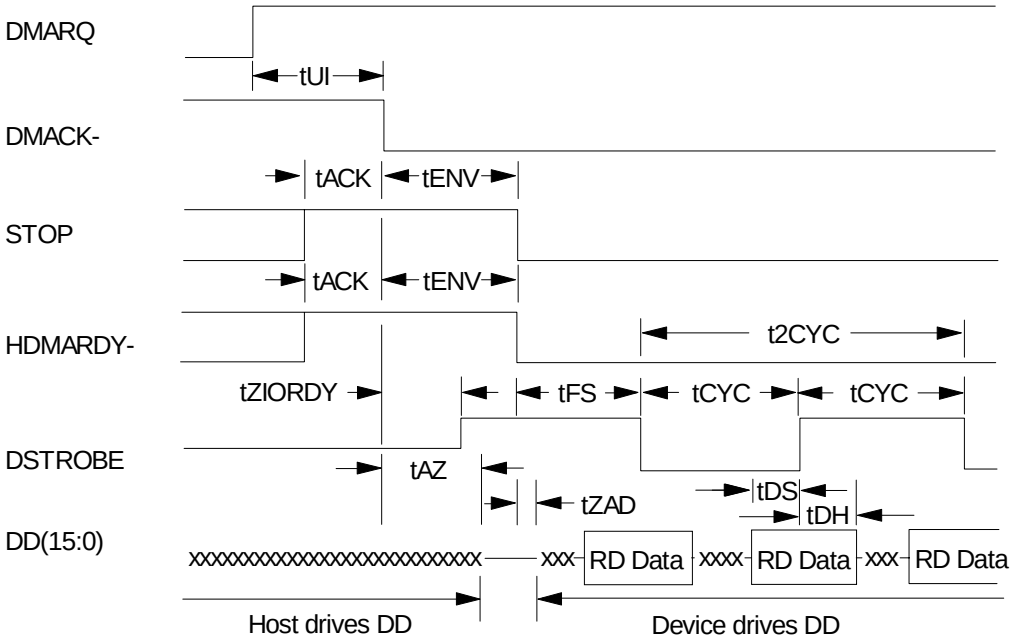


Table 29: Ultra DMA cycle timings (Initiating Read)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	50
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–
tFS	First DSTROBE time	0	230	0	200	0	170	0	130	0	120	0	90
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	16.8	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–	38	–
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10
tZAD	Drivers to assert	0	–	0	–	0	–	0	–	0	–	0	–
tDS	Data setup time at host	15	–	10	–	7	–	7	–	5	–	4	–
tDH	Data hold time at host	5	–	5	–	5	–	5	–	5	–	4.6	–

7.9.2 Host Pausing Read DMA

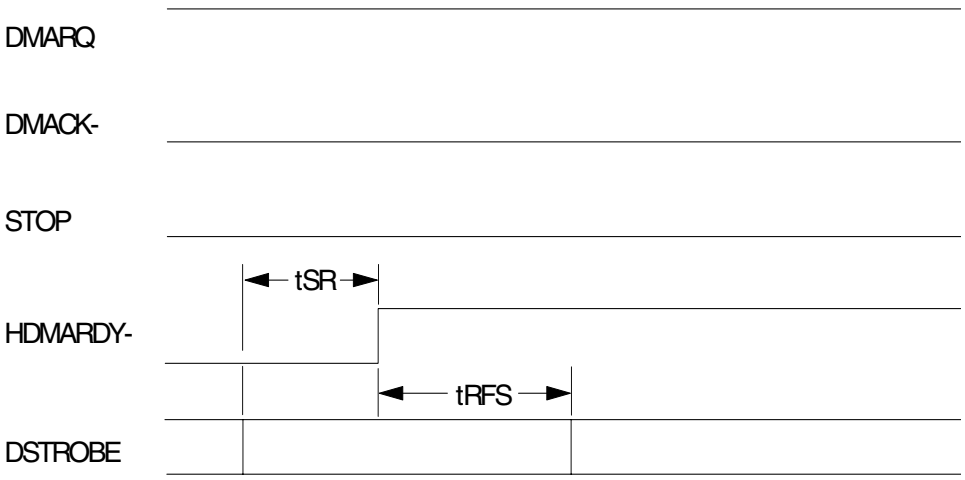


Table 30: Ultra DMA cycle timings (Host Pausing Read)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSR	DSTROBE to HDMARDY- time	–	50	–	30	–	20	–	–	–	–	–	–
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50

Note: When a host does not satisfy the tSR timing, the host should be ready to receive two more data words after HDMARDY - is negated.

7.9.3 Host Terminating Read DMA

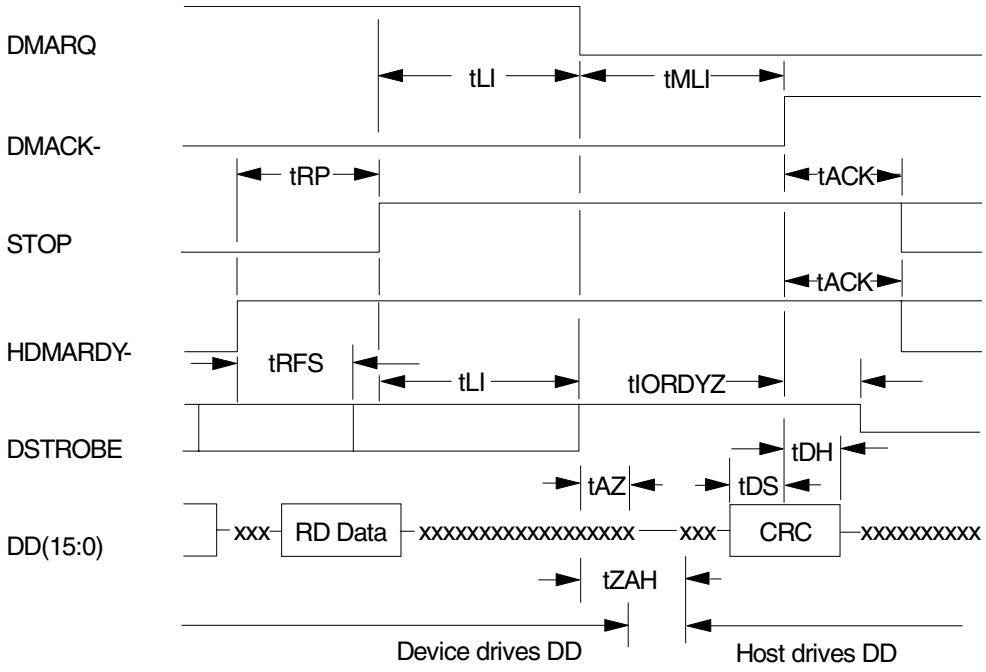


Table 31: Ultra DMA cycle timings (Host Terminating Read)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–
tACK	Hold time for DMACK- negation	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

7.9.4 Device Terminating Read DMA

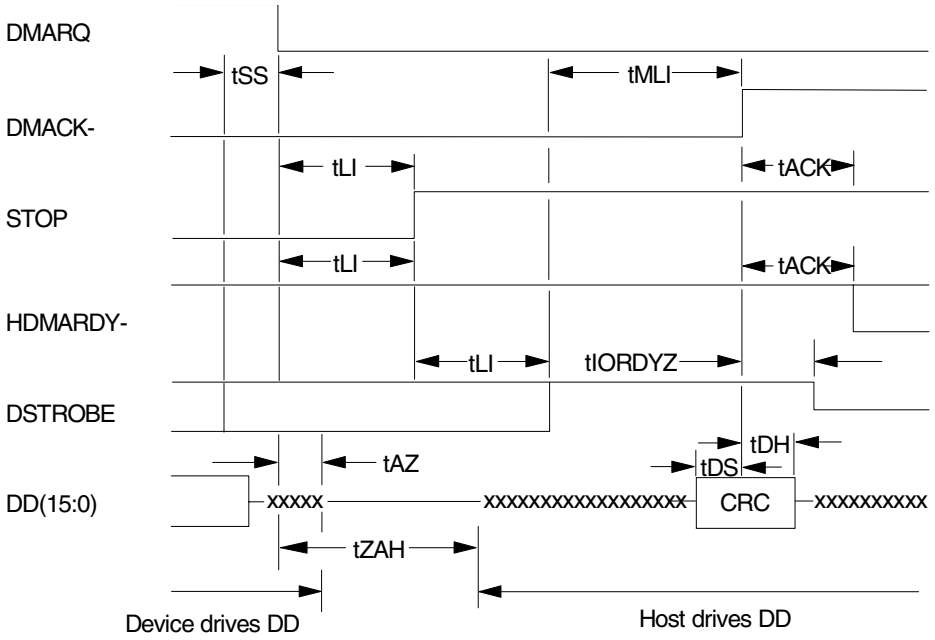


Table 32: Ultra DMA cycle timings (Device Terminating Read)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSS	Time from DSTROBE edge to negation of DMARQ	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Maximum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–
tACK	Hold time for DMACK- negation	20	–	20	–	20	–	20	–	20	–	–	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

7.9.5 Initiating Write DMA

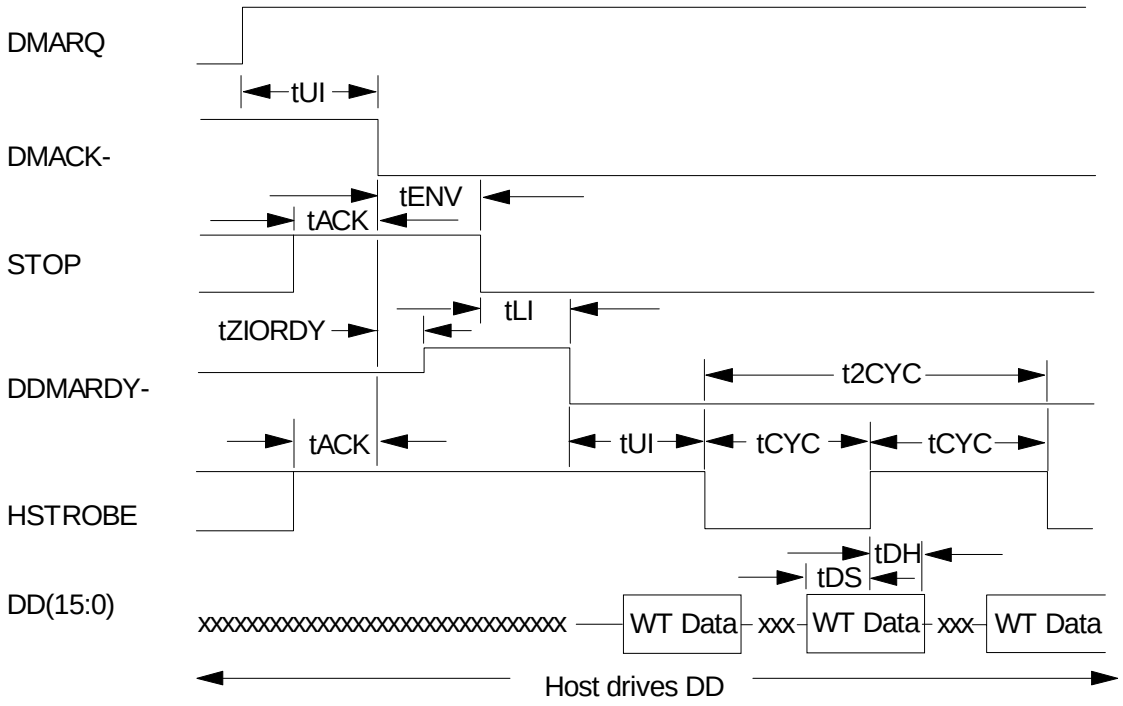


Table 33: Ultra DMA cycle timing (Initiating Write)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	55
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	16.8	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–	38	–
tDS	Data setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tDH	Data Hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–

7.9.6 Device Pausing Write DMA

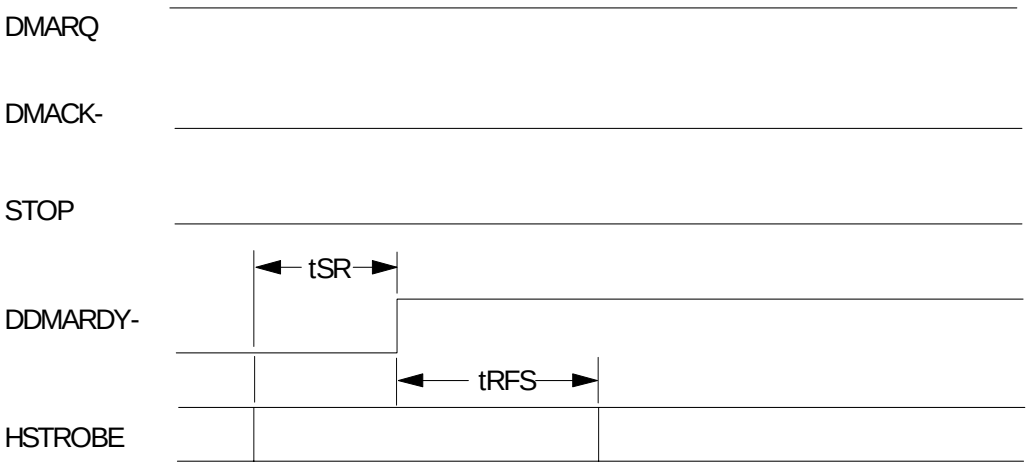


Table 34: Ultra DMA cycle timing (Device Pausing Write)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSR	HSTROBE to DDMARDY- time	–	50	–	30	–	20	–	–	–	–	–	–
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50

Note: When a device does not satisfy the tSR timing, the device is ready to receive two more data words after DDMARDY- is negated.

7.9.7 Device Terminating Write DMA

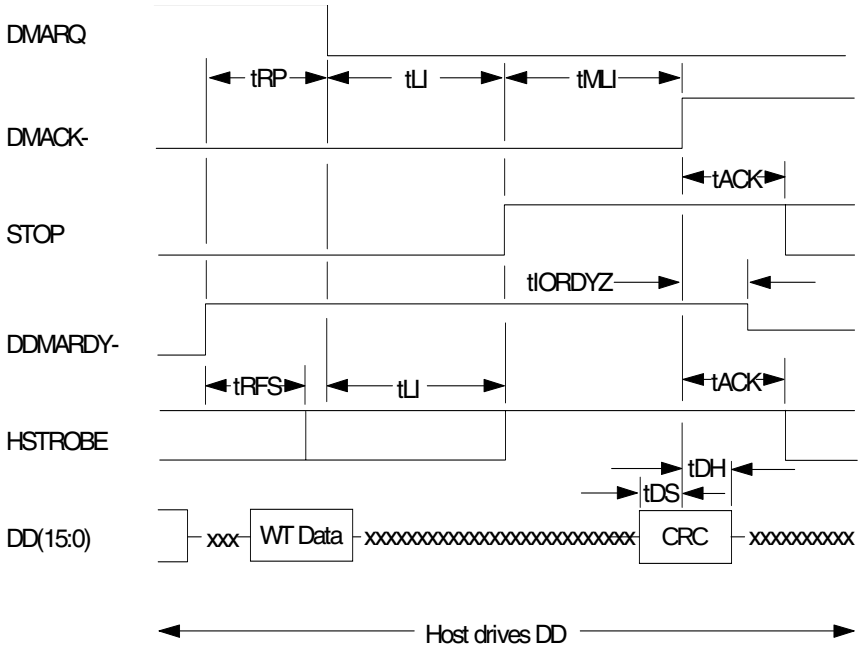


Table 35: Ultra DMA cycle timings (Device TerminatingWrite)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tMLI	Interlocking time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tDS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tDH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–
tACK	Hold time for DMACK- negation	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

7.9.8 Host Terminating Write DMA

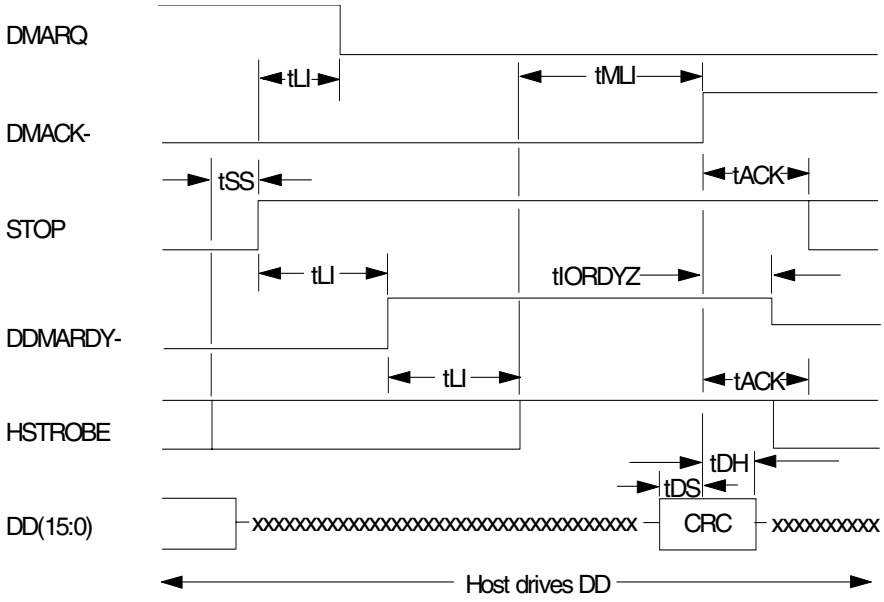
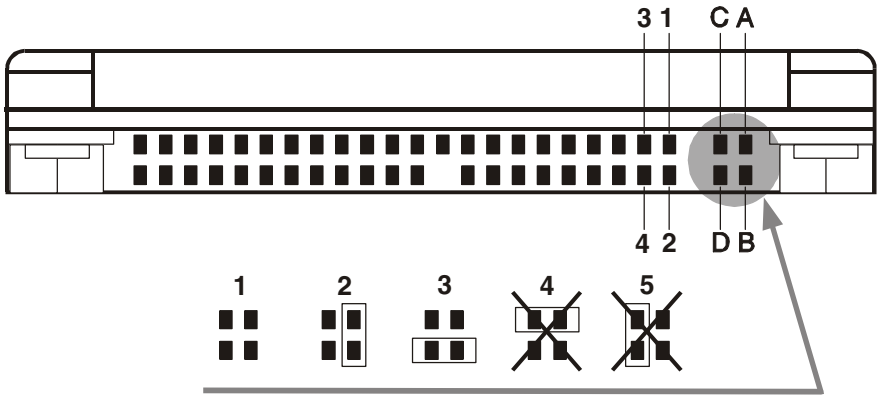


Table 36: Ultra DMA cycle timings (Host Terminating Write)

	PARAMETER DESCRIPTION	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
tSS	Time from HSTROBE edge to assertion of STOP	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tCH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

7.10 Drive address setting

A jumper placed on the interface connector determines the drive address. Three drive addresses are shown below. Two addresses require the setting of a jumper.



Setting 1—Device 0 (Master) (no jumper is used)
Setting 2—Device 1 (Slave)
Setting 3—Cable Select
Setting 4—Do not attach a jumper here
Setting 5—Do not attach a jumper here

The default setting at shipment is Setting 1 (no jumper).

When pin C is grounded, the drive does not spin up at POR.

When the drive address is Cable Select, the address depends on the condition of pin 28 of the AT interface cable. If pin 28 is ground (or low), the drive is a Master. If pin 28 is open (or logic high), the drive is a Slave.

7.11 Addressing of HDD registers

The host addresses the drive through a set of registers called a Task File. These registers are mapped into the host's I/O space. Two chip select lines (CS0- and CS1-) and three address lines (DA00–02) are used to select one of these registers, while a DIOR- or DIOW- is provided at the specified time.

The chip select line CS0- is used to address the Command Block registers while the CS1- is used to address Control Block registers.

The following table shows the I/ O address map.

CS0-	CS1-	DA02	DA01	DA00	DIOR- = 0 (Read)	DIOW- = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	LBA low Reg	LBA low Reg.
0	1	1	0	0	LBA mid Reg.	LBA mid Reg.
0	1	1	0	1	LBA high Reg.	LBA high Reg.
0	1	1	1	0	Drive Reg.	Device Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg.
1	0	1	1	1	Drive address Reg.	–

Part 2. Interface specification

8.0 General

8.1 Introduction

This specification describes the host interface of the Travelstar 5K100.

The interface conforms to the Working Document of Information technology, AT Attachment with Packet Interface Extension (ATA/ATAPI-6) Revision 2, dated 2 August 2001, with certain limitations described in Section 9.0, “Deviations from standard” on page 61.

The drive supports the following functions as Vendor Specific Functions:

- Address Offset Feature
- Format Unit Function
- SENSE CONDITION command

8.2 Terminology

Device	The Travelstar 5K100 drive
Host	Host indicates the system that the device is attached to.
First Command	The first command which is executed after the power on reset (also known as a hard reset) is the Standby mode command.
INTRQ	Interrupt request (Device or Host)

9.0 Deviations from standard

The device conforms to the referenced specifications, with deviations described below.

The interface conforms to the Working Document of Information Technology, AT Attachment with Packet Interface Extension (ATA/ATAPI-6) Revision 3, dated 30 October 2001, with the following deviation:

Write Verify	WRITE VERIFY command does not include read verification after write operation. The function is the same as WRITE SECTORS command.
S.M.A.R.T. Return Status	S.M.A.R.T. RETURN STATUS subcommand does not check advisory attributes. This means that the device will not report a threshold exceeded condition unless the prefailure attributes exceed their corresponding thresholds. For example, a Power-On Hours Attribute never results in a negative reliability status.

10.0 Register

Table 37: Register Set

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ (DIOR-)	WRITE (DIOW-)
N	N	x	x	x	Data bus high impedence	Not used
					Control block registers	
N	A	0	x	x	Data bus high impedance	Not used
N	A	1	0	x	Data bus high impedance	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	LBA Low	LBA Low
A	N	0	1	1	LBA bits 0-7	LBA bits 0-7
A	N	1	0	0	LBA Mid	LBA Mid
A	N	1	0	0	LBA bits 8-15	LBA bits 8-15
A	N	1	0	1	LBA High	LBA High
A	N	1	0	1	LBA bits 16-23	LBA bits 16-23
A	N	1	1	0	Device	Device
A	N	1	1	0	LBA bits 24-27	LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Logic conventions: A = signal asserted
N = signal not asserted
x = either A or N

Communication to or from the device is through an I/O Register that routes the input or output data to or from the registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

10.1 Alternate Status Register

Table 38: Alternate Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR

This register contains the same information as the Status Register. The only difference between this register and the Status Register is that reading the Alternate Status Register does not imply an interrupt acknowledge or a clear of a pending interrupt. See Section 10.13 "Status Register," on page 67 for the definition of the bits in this register.

10.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Table 58: "Command Set (1 of 2)," on page 97 and Table 59: "Command Set (2 of 2)," on page 98. All other registers required for the command must be set up before writing to the Command Register.

10.3 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command and the configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ = 1 is in the Status Register.

10.4 Device Control Register

Table 39: Device Control Register

7	6	5	4	3	2	1	0
HOB	-	-	-	1	SRST	-IEN	0

Bit	Definitions
HOB	HOB (high order byte) is defined by the 48-bit Address feature set. A write to any Command Register shall clear the HOB bit to zero.
SRST (RST)	Software Reset. The device is held at reset when RST = 1. Setting RST = 0 again enables the device. To ensure that the device recognizes the reset, the host must set RST = 1 and wait for at least 5 ms before setting RST = 0.
-IEN	Interrupt Enable. When IEN = 0, and the device is selected, the device interrupts to the host will be enabled. When IEN = 1, or the device is not selected, the device interrupts to the host will be disabled.

10.5 Drive Address Register

Table 40: Drive Address Register

7	6	5	4	3	2	1	0
HIZ	WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit	Definitions
HIZ	High Impedance. This bit is not a device and will always be in a high impedance state.
-WTG	Write Gate. This bit is 0 when writing to the disk device is in progress.
-H3, -H2,-H1,-H0-	-H3, -H2,-H1,-H0-Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. Bit -H0 is the least significant.
-DS1	Drive Select 1. The Drive Select bit for device 1 is active low. DS1 = 0 when device 1 (slave) is selected and active.
-DS0	Drive Select 0. The Drive Select bit for device 0 is active low. DS0 = 0 when device 0 (master) is selected and active.

10.6 Device Register

Table 41: Device Head/Register

7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

This register contains the device and head numbers.

Bit	Definitions
L	Binary encoded address mode select. When L = 0, addressing is by CHS mode. When L = 1, addressing is by LBA mode.
DRV	Device. When DRV = 0, device 0 (Master) is selected. When DRV = 1, device 1 (Slave) is selected.
HS3, HS2, HS1, HS0	These contain bits 24-27 of the LBA. At command completion these bits are updated to reflect the current LBA bits 24-27.

10.7 Error Register

Table 42: Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

This register contains the status from the last command executed by the device or a diagnostic code. At the completion of any command except Execute Device Diagnostic, the contents of this register are always valid even if ERR = 0 is in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Table 46: "Diagnostic codes," on page 70 for the definitions.

Bit	Definitions
ICRCE (CRC)	Interface CRC Error. When CRC = 1, it indicates that a CRC error has occurred on the data bus during a Ultra DMA transfer.
UNC	Uncorrectable Data Error. When UNC = 1, it indicates that an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. When IDN = 1, it indicates that the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. When ABT = 1, it indicates that the requested command has been aborted due to a device status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. When T0N = 1, it indicates that track 0 was not found during a recallibrate command.

10.8 Features Register

This register is command specific. This register is used with the Set Features command, the S.M.A.R.T. Function Set command, and the Format Unit command.

10.9 LBA High Register

This register is command specific. This is used with the Set Features command, S.M.A.R.T. Function Set command and Format Unit command.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 16-23, and the "previous content" contains Bits 40-47. The 48-bit Address feature set is described in Section 11.15 "48-bit Address Feature Set," on page 89.

10.10 LBA Low Register

This register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7, and the "previous content" contains Bits 24-31.

10.11 LBA Mid Register

This register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15 and the "previous content" contains Bits 32-39.

10.12 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

10.13 Status Register

Table 43: Status Register

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC	DRQ	CORR	IDX	ERR

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit	Definitions
BSY	Busy. Bit BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. When bit RDY=1 it indicates that the device is capable of responding to a command. Bit RDY will be set to 0 during power on until the device is ready to accept a command.
DF	Device Fault. It DF=1 it indicates that the device has detected a write fault condition. Bit DF is set to 0 after the Status Register is read by the host.
DSC	Device Seek Complete. If DSC=1, it indicates that a Seek has completed and the device head is settled over a track. Bit DSC is set to 0 by the device just before a Seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host and at that time the bit again indicates the current Seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of the drive not spinning up.
DRQ	Data Request. Bit DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR	Corrected Data. Always 0
IDX	IDXIndex. Bit IDX=1 once per revolution. Since IDX=1, only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX bit for timing purposes.
ERR	Error. Bit ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets bit ERR=0 when the next command is received from the host.

11.0 General

11.1 Reset response

ATA has the following three types of resets:

Power On Reset (POR)	The device executes a series of electrical circuitry diagnostics, spins up the head disk assembly, tests speed and other mechanical parametric, and sets default values.
Hard Reset (Hardware Reset)	The RESET signal is negated in the ATA Bus. The device resets the interface circuitry and sets the default values.
Soft Reset (Software Reset)	The SRST bit in the Device Control Register is set and then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in the table below.

Table 44: Reset response table

	POR	hard reset	soft reset
Aborting Host interface	-	o	o
Aborting Device operation	-	(*1)	(*1)
Initialization of hardware	o	x	x
Internal diagnostic	o	x	x
Starting spindle motor	(*5)	x	x
Initialization of registers (*2)	o	o	o
DASP- handshake	o	o	x
PDIAG- handshake	o	o	o
Reverting programmed parameters to default Number of CHS (set by Initialize Device Parameters) Multiple mode Write Cache Read look-ahead ECC bytes Volatile max address Address offset mode	o	o	(*3)
Power mode	(*6)	(*4)	(*4)
Reset Standby timer value (*5)	o	o	o

o – execute x – does not execute

Notes:

(*1) Execute after the data in write cache has been written.

(*2) The default value on POR is shown in Table 45: “Default Register Values” on page 70.

(*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4) In the case of sleep mode, the device goes to standby mode. In other cases, the device does not change current mode.

(*5) After reset the Standby timer value is set to 109 minutes.

(*6) Set according to the initial power mode selection.

11.2 Register initialization

After a power on, a hard reset, or a software reset, the register values are initialized as shown in the table below.

Table 45: Default Register Values

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
LBA Low	01h
LBA Mid	00h
LBA High	00h
Device	A0h
Status	50h
Alternate Status	50h

The meaning of the Error Register diagnostic codes resulting from power on, hard reset, or the Execute Device Diagnostic command are shown in the following table.

Table 46: Diagnostic codes

Code	Description
01h	No error detected
02h	Format device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

11.3 Diagnostic and Reset considerations

The Set Max password, the Set Max security mode and the Set Max unlock counter are not retained over a Power On Reset but are retained over a Hard Reset or Soft Reset.

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset, Hard Reset DASP– is read by Device 0 to determine if Device 1 is present. If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP– to indicate device activity. If Device 1 is not present, Device 0 does not Assert DASP– at POR.

Soft Reset If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors; otherwise, Device 0 shall simply reset and clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command; otherwise, Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate that the device is active.

In each case the interpretation of the Device 0 Error register value is shown in the table below. The "x" indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft Reset, or Device Diagnostic error.

Device 1 present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

11.4 Power-off considerations

11.4.1 Load/Unload

Load/Unload is a functional mechanism of the hard disk drive and is controlled by the drive microcode. Specifically, unloading of the heads is invoked by the following commands.

Table 47: Device behavior by ATA command

Command	Response
Standby	UL -> Comp.
Standby Immediate	UL -> Comp.
Sleep	UL -> Comp.

Reset	Response
Soft Reset	Rdy (*1)
Hard Reset	UL -> Rdy

UL = unload
Comp = complete
Rdy = interface ready
(*1) Load/Unload condition is not changed by Soft Reset

Load is also invoked as the idle command.

The specified start/stop life of the hard disk drive assumes that load/unload is operated normally, NOT in emergency mode.

11.4.2 Emergency unload

When the drive power is interrupted with the heads still loaded, the microcode cannot operate and the normal 5V power is unavailable to unload the heads. In this case, normal unload is not possible, so the heads are unloaded by routing the back EMF of the spinning motor to the voice coil. The actuator velocity is greater than the normal case and the unload process is inherently less controllable without a normal seek current profile.

Emergency unload is intended to be invoked in rare situations. Because this operation is inherently uncontrolled, it is more mechanically stressful than a normal unload.

A single emergency unload operation is more stressful than 100 normal unloads. Use of emergency unload reduces the start/stop life of the drive at a rate at least 100 times faster than that of normal unload and may damage the drive.

11.4.3 Required power-off sequence

The following are examples of problems which can occur when power is removed on most drives at an arbitrary time:

- Data is lost from the write buffer.
- If the drive is writing a sector, a partially-written sector with an incorrect ECC block results, the sector contents are destroyed, and reading that sector results in a hard error.
- Heads may land in the data zone instead of the landing zone depending on the design of the drive.

You may then turn off the drive in the following order:

1. Issue Standby Immediate or sleep command
2. Wait until COMMAND COMPLETE STATUS is returned. (It may take up to 350 ms in a typical case.)
3. Terminate power to drive

This power-down sequence should be followed for entry into any system power-down state, system suspend state, or system hibernation state. In a robustly designed system, emergency unload is limited to rare scenarios such as battery removal during operation.

11.5 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is done by a logical sector address. The logical CHS address for the drive is different from the actual physical CHS location of the data sector on the disk media.

The drive supports both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. A host system must set the L bit to 1 if the host uses LBA Addressing mode.

11.5.1 Logical CHS addressing mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number, and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but cannot exceed 255 (0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 15 (0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535 (0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

11.5.2 LBA addressing mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following formula is always true:

$$LBA = ((cylinder \times heads\_per\_cylinder + heads) \times sectors\_per\_track) + sector - 1$$

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode, the LBA value is set to the following register:

Device	<- - - LBA bits 27–24
LBA High	<- - - LBA bits 23–16
LBA Mid	<- - - LBA bits 15–8
LBA Low	<- - - LBA bits 7–0

11.6 Power management features

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

The drive implements the following set of functions:

- A Standby timer
- Idle command
- Idle Immediate command
- Sleep command
- Standby command
- Standby Immediate command

11.6.1 Power mode

Sleep Mode	The lowest power consumption when the device is powered on occurs in Sleep Mode. When in Sleep Mode, the device requires a reset to be activated.
Standby Mode	The device interface is capable of accepting commands, but since the media may not be immediately accessible, there is a delay while waiting for the spindle to reach operating speed.
Idle Mode	Refer to Section 11.7 “Advanced Power Management (ABLE-3) feature” on page 75.
Active Mode	The device is in execution of a command or accessing the disk media with the read look-ahead function or the write cache function.

11.6.2 Power management commands

The Check Power Mode command allows a host to determine if a device is currently in, going to, or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The sleep command moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter standby mode.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

11.6.3 Standby/Sleep command completion time

1. Confirm the completion of writing cached data in the buffer to media.
2. Unload the heads on the ramp.
3. Set the DRDY bit and the DSC bit in Status Register.
4. Set the INTRQ (completion of the command).
5. Activate the spindle break to stop the spindle motor.
6. Wait until the spindle motor is stopped.
7. Perform the post process.

11.6.4 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

11.6.5 Status

In the active, idle, and standby modes, the device shall have the RDY bit of the status register set. If the BSY bit is not set, the device shall be ready to accept any command.

In sleep mode, the device's interface is not active. A host shall not attempt to read the status of the device or issue commands to the device.

11.6.6 Interface capability for power modes

Each power mode affects the physical interface as defined in the following table:

Table 48: Power conditions

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	o	1	Yes	Active
Standby	o	1	Yes	Inactive
Sleep	x	x	No	Inactive

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

The interface is inactive in sleep mode, but the access to the interface registers and the validity of INTRQ is guaranteed for two seconds after the Sleep command is completed. After this period, the contents of interface registers may be lost. Since the contents of interface registers may be invalid, the host should NOT check the Status register nor the Alternate Status register prior to issuing a soft reset to wake up a device.

11.6.7 Initial Power Mode at Power On

After power on or hard reset the device goes to IDLE mode or STANDBY mode depending on the option. Refer to section 4.4.3 “Operating modes” on page 16 for the initial power mode selection.

11.7 Advanced Power Management (ABLE-3) feature

This feature provides power saving without performance degradation. The Adaptive Battery Life Extender 3 (ABLE-3) technology intelligently manages transition among power modes within the device by monitoring access patterns of the host.

This technology has three idle modes: Performance Idle mode, Active Idle mode, and Low Power Idle mode.

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands, described in the section of Set Feature command in detail.

This feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

The Advanced Power Management feature is independent of the Standby timer setting. If both Advanced Power Management level and the Standby timer are set, the device will go to the Standby state when the timer times out or the device's Advanced Power Management algorithm indicates that it is time to enter the Standby state.

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contains the current Advanced Power Management level if Advanced Power Management is enabled.

11.7.1 Performance Idle Mode

This mode is usually entered immediately after Active mode command processing is complete, instead of conventional idle mode. In Performance Idle mode, all electronic components remain powered and full frequency servo remains operational. This provides instantaneous response to the next command. The duration of this mode is intelligently managed as described below.

11.7.2 Active Idle Mode

In this mode, power consumption is 45–55% less than that of Performance Idle mode. Additional electronics are powered off and the head is parked near the mid-diameter of the disk without servoing. Recovery time to Active mode is about 20 ms.

11.7.3 Low Power Idle Mode

Power consumption is 60–65% less than that of Performance Idle mode. The heads are unloaded on the ramp but the spindle is still rotated at the full speed. Recovery time to Active mode is about 300 ms.

11.7.4 Transition time

The transition time is dynamically managed by the user's recent access pattern, instead of fixed times. The ABLE-3 algorithm monitors the interval between commands instead of the command frequency of ABLE-2. The algorithm supposes that the next command will come with the same command interval distribution as the previous access pattern. The algorithm calculates the expected average saving energy and response delay for next command in several transition time case based on this assumption. And it selects the most effective transition time with the condition that the calculated response delay is shorter than the value calculated from the specified level by Set Feature Enable Advanced Power Management command.

The optimal time to enter Active Idle mode is variable depending on the recent behavior of the user. It is not possible to achieve the same level of Power savings with a fixed entry time into Active Idle because every user's data and access pattern is different. The optimum entry time changes over time.

The same algorithm works for entering into Low Power Idle mode and Standby mode, which consumes less power but needs more recovery time switching from this mode to Active mode.

11.8 Interface Power Management Mode (Slumber and Partial)

Interface Power Management Mode is only supported Device-initiated interface power management. Please refer to the Serial ATA Specification about Power Management Mode.

11.9 S.M.A.R.T. Function

The intent of Self-monitoring, analysis, and reporting technology (S.M.A.R.T.) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

Since S.M.A.R.T. utilizes the internal device microprocessor and other device resources, there may be some small overhead associated with its operation. However, special care has been taken in the design of the S.M.A.R.T. algorithms to minimize the impact to host system performance. Actual impact of S.M.A.R.T. overhead is dependent on the specific device design and the usage patterns of the host system. To further ensure minimal impact to the user, S.M.A.R.T. capable devices are shipped from the device manufacturer's factory with the S.M.A.R.T. feature disabled. S.M.A.R.T. capable devices can be enabled by the system OEMs at time of system integration or in the field by after-market products.

11.9.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

11.9.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or fault condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or fault condition existing. There is no implied linear reliability relationship corresponding to the numerical relationship between different attribute values for any particular attribute.

11.9.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

11.9.4 Threshold exceeded condition

If one or more attribute values are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

11.9.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

11.9.6 S.M.A.R.T. operation with power management modes

The device saves attribute values automatically on every head unload timing except the emergency unload, even if the attribute auto save feature is not enabled. The head unload is done not only by Standby, Standby Immediate, Sleep command, and Hard Reset, but also by the Standby timer. So it is not necessary for a host system to enable the attribute auto save feature when it utilizes the power management. If the attribute auto save feature is enabled, attribute values will be saved after 30 minutes have passed since the last saving, besides above condition.

11.10 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to a device even if it is removed from the computer.

New commands are supported for this feature as listed below:

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

11.10.1 Security mode

The following security modes are provided:

Device Locked Mode	The device disables media access commands after power on. Media access commands are enabled by either a Security Unlock command or a Security Erase Unit command.
Device Unlocked Mode	The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a Security Unlock or a Security Erase Unit command.
Device Frozen Mode	The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

11.10.2 Security level

The following security levels are provided:

High level security	When the device lock function is enabled and the User Password is forgotten, the device can be unlocked via a Master Password.
Maximum level security	When the device lock function is enabled and the User Password is forgotten, then only the Master Password with a Security Erase Unit command can unlock the device. Then the user data is erased.

11.10.3 Password

This function can have two types of passwords as described below.

Master Password	When the Master Password is set, the device does NOT enable the Device Lock Function, and the device CANNOT be locked with the Master Password, but the Master Password can be used for unlocking the locked device.
User Password	The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on the next power on reset or hard reset.

The system manufacturer or dealer who intends to enable the device lock function for end users must set the master password even if only single level password protection is required. Otherwise, the default master password which is set by Hitachi Global Storage Technologies can unlock a device that is locked with a user password

11.10.4 Master Password Revision Code

This Master Password Revision Code is set by Security Set Password command with the master password. And this revision code field is returned in the Identify Device command word 92. The valid revision codes are 0001h to FFFEh. The default value of Master Password Revision Code is FFFEh. Values 0000h and FFFFh are reserved.

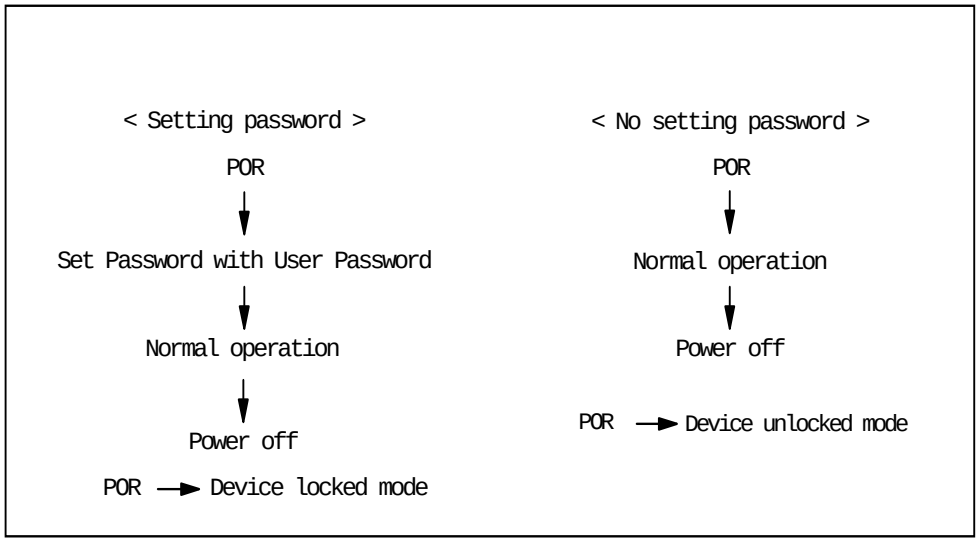
11.10.4.1 Master Password setting

The system manufacturer or dealer can set an initial Master Password using the Security Set Password command, without enabling the Device Lock Function.

11.10.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

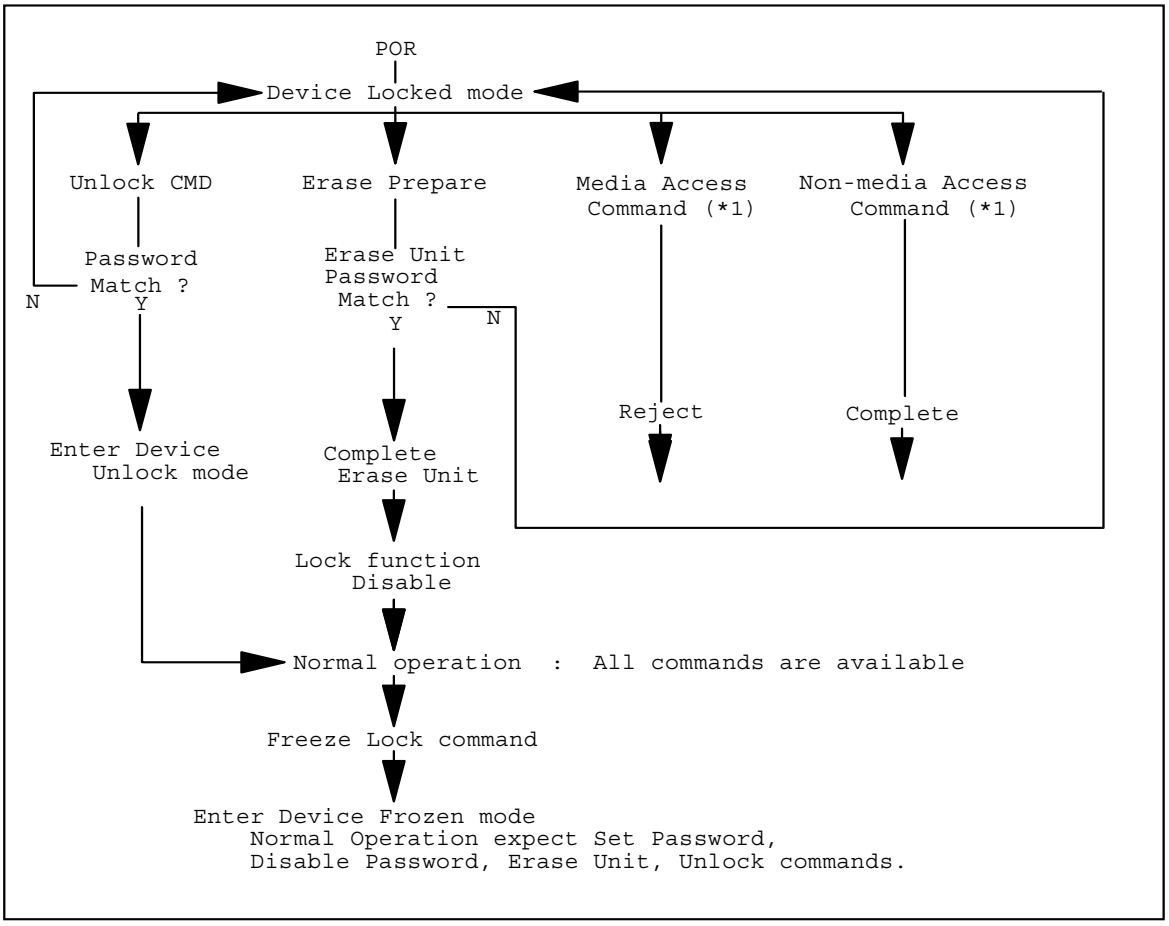
Table 49: Initial setting



11.10.4.3 Operation from POR after user password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

Table 50: Usual operation for POR



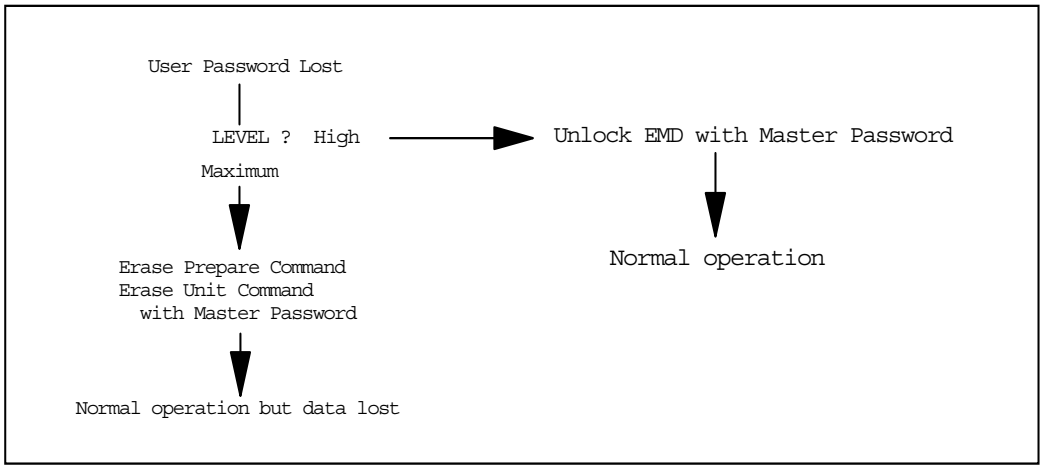
(*1) — refers to the commands in Table 52: “Command table for device lock operation” on page 82.

11.10.4.4 User Password lost

If the User Password is forgotten and High level security is set, the system user cannot access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

Table 51: Password lost



11.10.4.5 Attempt limit for the SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit, the purpose of which is to prevent someone from attempting to unlock the drive with various passwords numerous times.

The device counts the password mismatch. If the password does not match, the device counts it without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set, and then the SECURITY ERASE UNIT command and the SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

11.10.5 Command table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Table 52: Command table for device lock operation

Command	Device Mode				Command	Device Mode		
	Locked	Unlocked	Frozen			Locked	Unlocked	Frozen
Check Power Mode	o	o	o		Seek	o	o	o
Device Configuration RESTORE	x	o	o		Sense Condition	o	o	o
Device Configuration FREEZE LOCK	o	o	o		Set Features	o	o	o
Device Configuration IDENTIFY	o	o	o		Set Max ADDRESS	x	o	o
Device Configuration SET	x	o	o		Set Max ADDRESS EXT	x	o	o
Execute Device Diagnostic	o	o	o		Set Max FREEZE LOCK	o	o	o
Flush Cache	x	o	o		Set Max LOCK	o	o	o
Flush Cache EXT	x	o	o		Set Max SET PASSWORD	o	o	o
Format Track	x	o	o		Set Max UNLOCK	o	o	o
Format Unit	x	o	o		Set Multiple Mode	o	o	o
Identify Device	o	o	o		Sleep	o	o	o
Idle	o	o	o		S.M.A.R.T. Disable Operations	o	o	o
Idle Immediate	o	o	o		S.M.A.R.T. Enable/Disable automatic off-line	o	o	o
Initialize Device Parameters	o	o	o		S.M.A.R.T. Enable/Disable Attribute Autosave	o	o	o
Read Buffer	o	o	o		S.M.A.R.T. Enable Operations	o	o	o
Read DMA	x	o	o		S.M.A.R.T. Execute Off-line Immediate	o	o	o
Read DMA EXT	x	o	o		S.M.A.R.T. Read Attribute Values	o	o	o
Read Long	x	o	o		S.M.A.R.T. Read Attribute Thresholds	o	o	o
Read Multiple	x	o	o		S.M.A.R.T. Read log sector	o	o	o
Read Multiple EXT	x	o	o		S.M.A.R.T. Write log sector	o	o	o
Read Native Max ADDRESS	o	o	o		S.M.A.R.T. Return Status		o	o
Read Native Max ADDRESS EXT	o	o	o		S.M.A.R.T. Save Attribute Values	o	o	o
Read Sector(s)	x	o	o		Standby	o	o	o
Read Sector(s) EXT	x	o	o		Standby Immediate	o	o	o
Read Verify Sector(s)	x	o	o		Write Buffer	o	o	o
Read Verify Sector(s) EXT	x	o	o		Write DMA	x	o	o
Recalibrate	o	o	o		Write DMA EXT	x	o	o
Security Disable Password	x	o	x		Write Long	x	o	o
Security Erase Prepare	o	o	o		Write Multiple	x	o	o
Security Erase Unit	o	o	x		Write Multiple EXT	x	o	o
Security Freeze Lock	x	o	o		Write Sector(s)	x	o	o
Security Set Password	x	o	x		Write Sector(s) EXT	x	o	o
Security Unlock	o	o	x		Write Verify	x	o	o

11.11 Protected Area Function

Protected Area Function provides a protected area which cannot be accessed via conventional methods. This protected area is used to contain critical system data such as BIOS or system management information. The contents of the entire system main memory may also be dumped into the protected area to resume after a system power off.

The LBA/CYL changed by the following commands affects the Identify Device Information.

Two commands are defined for this function:

- Read Native Max ADDRESS ('F8'h)
- Set Max ADDRESS ('F9'h)

Four security extension commands are implemented as sub functions of the Set Max ADDRESS:

- Set Max SET PASSWORD
- Set Max LOCK
- Set Max FREEZE LOCK
- Set Max UNLOCK

11.11.1 Example for operation (In LBA Mode)

The following example uses hypothetical values.

Device characteristics:

Capacity (native)	536,870,912 bytes (536MB)
Max LBA (native)	1,048,575 (0FFFFFh)
Required size for protected area	8,388,608 bytes
Required blocks for protected area	16,384 (004000h)
Customer usable device size	528,482,304 bytes (528MB)
Customer usable sector count	1,032,192 (0FC000h)
LBA range for protected area	0FC000h to 0FFFFFh

1. Shipping drives from the drive manufacturer

   When the drive is shipped from the manufacturer, the device has been tested to have a capacity of 536 MB, flagging the media defects not visible by the system.

2. Preparing drives at system manufacturer

   Special utility software is required to define the size of the protected area and to store the data in it. The sequence is:

   Issue Read Native Max ADDRESS command to get the real device max of LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFh regardless of the current setting.

   Make the entire device accessible, including the protected area, by setting the device Max LBA as 0FFFFFh via Set Max ADDRESS command. The option could be either nonvolatile or volatile.

   Test the sectors for protected area (LBA > = 0FC000h) if required.

   Write information data such as BIOS code within the protected area.

   Change maximum LBA using Set Max ADDRESS command to 0FBFFFh with nonvolatile option.

From this point the protected area cannot be accessed until the next Set Max ADDRESS command is issued. Any BIOS, device driver, or application software accesses the drive as if it is a 528 MB device because the device behaves like a 528 MB device.

3. Conventional usage without system software support:

   Because the drive works as a 528 MB device, there is no special care required for normal use of this device.

4. Advanced usage using protected area.

   The data in the protected area is accessed by the following steps.

   1. Issue Read Native Max ADDRESS command to get the real device max LBA/CYL. Returned value shows that native device Max LBA is 0FFFFFh regardless of the current setting.
   2. Make entire device accessible, including the protected area, by setting device Max LBA as 0FFFFFh via Set Max ADDRESS command with the volatile option. By using this option, unexpected power removal or reset will prevent the protected area from remaining accessible.
   3. Read information data from protected area.
   4. Issue hard reset or POR to inhibit any access to the protected area.

11.11.2 Set Max security extension commands

The Set Max SET PASSWORD command allows the host to define the password to be used during the current power on cycle. This password is not related to the password used for the Security Mode Feature set. When the password is set, the device is in the Set Max Unlocked mode.

This command requests a transfer of a single sector of data from the host. The following figure defines the content of this sector of information. The password is retained by the device until the next power cycle. When the device accepts this command, the device is in Set Max Unlocked mode.

Table 53: Set Max SET PASSWORD data content

Word	Content
0	Reserved
1-16	Password (32 bytes)
17-255	Reserved

The Set Max LOCK command allows the host to disable the Set Max commands (except Set Max UNLOCK and Set Max FREEZE LOCK) until the next power cycle or the issuance and acceptance of the Set Max UNLOCK command. When this command is accepted, the device is in the Set Max Locked mode.

The Set Max UNLOCK command changes the device from the Set Max Locked mode to the Set Max Unlocked mode.

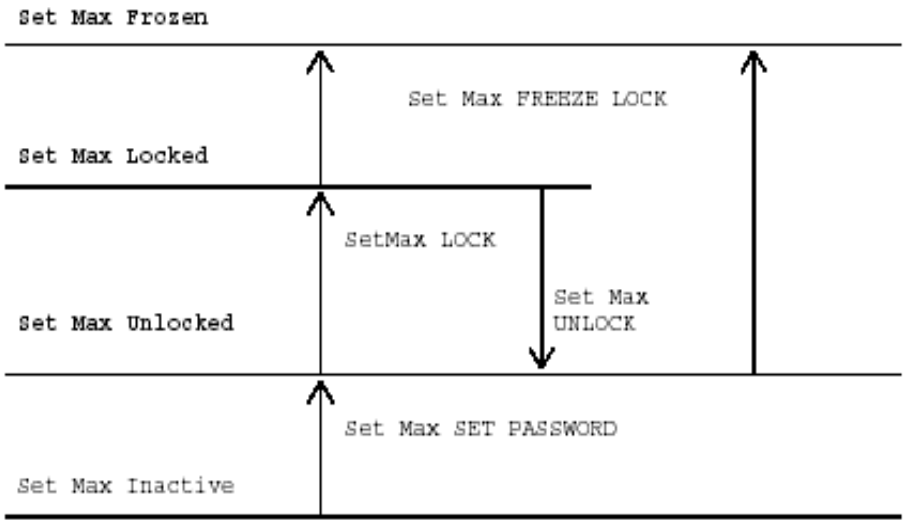
This command requests a transfer of a single sector of data from the host. The figure shown above defines the content of this sector of information. The password supplied in the sector of data transferred is compared with the stored Set Max password. If the password compare fails, then the device returns command aborted and decrements the unlock counter. On the acceptance of the Set Max LOCK command, this counter is set to a value of five and is decremented for each password mismatch when Set Max UNLOCK is issued and the device is locked. When this counter reaches zero, then the Set Max UNLOCK command returns command aborted until a power cycle.

The Set Max FREEZE LOCK command allows the host to disable the SET MAX commands (including Set Max UNLOCK) until the next power cycle. When this command is accepted the device is in the Set Max Frozen mode.

The password, the Set Max security mode, and the unlock counter do not persist over a power cycle but persist over a hardware or software reset.

NOTE: If this command is immediately preceded by a Read Native MAX ADDRESS command, it shall be interpreted as a Set Max ADDRESS command regardless of Feature register value.

Table 54: Set Max security mode transition



11.12 Address Offset Feature (vendor specific)

Computer systems perform initial code loading (booting) by reading from a predefined address on a disk drive. To allow an alternate bootable operating system to exist in a reserved area on a disk drive this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire disk drive address space remains addressable in offset mode. The Set Max pointer is set to the end of the reserved area to protect the data in the user area when operating in offset mode. This protection can be removed by a Set Max Address command to move the Set Max pointer to the end of the drive. But any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by a Set Max Address command.

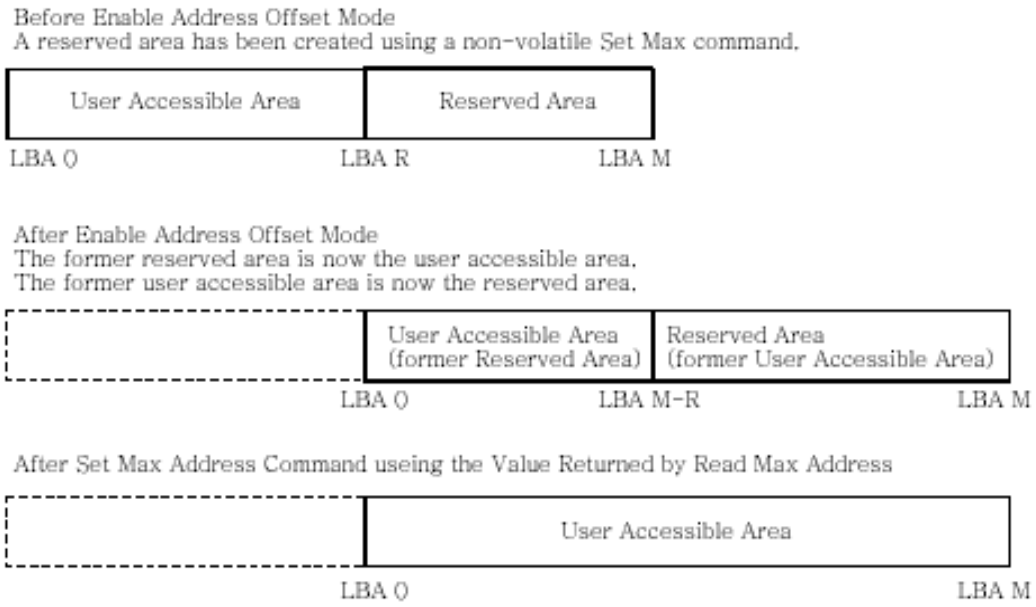
11.12.1 Enable/Disable Address Offset Mode

Subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, LBA 0, to the start of the nonvolatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by the Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a nonvolatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command, the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last nonvolatile Set Max Address command.

Table 55: Device address map before and after Set Feature



11.12.2 Identify Device Data

Identify Device data, word 83, bit 7 indicates the device supports the Address Offset Feature. Identify Device data, word 86, bit 7 indicates the device is in Address Offset mode.

11.12.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error, even if the access protection is removed by a Set Max Address command.

Read Look Ahead operation and Write Cache Function are not carried out in Address Offset mode, even if they are enabled by the Set Feature command.

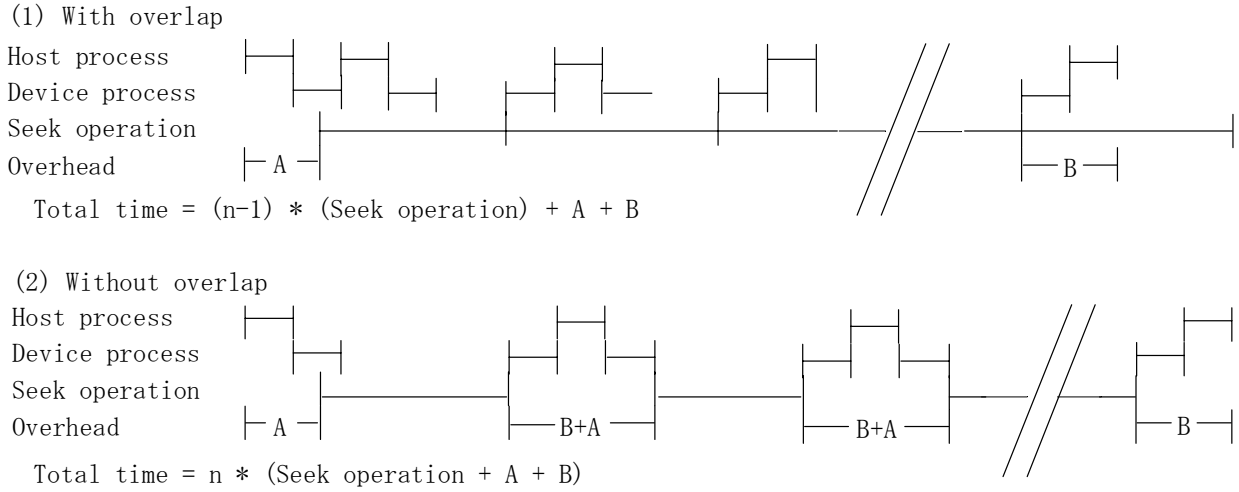
11.13 Seek Overlap

The drive provides accurate seek time measurement method. The seek command is usually used to measure the device seek time by accumulating execution time for a number of seek commands. With typical implementation of the seek command, this measurement must include the device and host command overhead. To eliminate this overhead, the drive overlaps the seek command as described below.

The first seek command completes before the actual seek operation is over. Then the device can receive the next seek command from the host. However, the actual seek operation for the next seek command starts right after completion of the actual seek operation for the first seek command. The execution of two seek commands overlaps excluding the actual seek operation.

With this overlap, total elapsed time for a number of seek commands is the total accumulated time for the actual seek operation plus one pre and post overhead. When the number of seeks is large, this overhead can be ignored.

Table 56: Seek overlap



11.14 Write Cache function

Write cache is a performance enhancement whereby the device reports completion of the write command (Write Sector(s) and Write Multiple) to the host as soon as the device has received all of the data in its buffer. The device assumes responsibility to write the data subsequently onto the disk.

- Writing data after completed acknowledgment of a write command, soft reset, or hard reset does not affect its operation but power off terminates writing operation immediately and unwritten data is lost.
- Flush cache, Soft reset, Standby, Standby Immediate, and Sleep are executed after the completion of writing to disk media on enabling write cache function. The host system can confirm the completion of Write Cache operation by issuing Flush Cache command, Soft reset, Standby command, Standby Immediate command, or Sleep command, and then confirming the completion of the issued command.

11.15 Reassign Function

The Reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector. The one entry can register 256 consecutive sectors maximum.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare tracks for reassignment are located at regular intervals from Cylinder 0. As a result of reassignment, the physical location of logically sequenced sectors is dispersed.

11.15.1 Auto Reassign Function

The sectors that show some errors may be reallocated automatically when specific conditions are met. The spare tracks for reallocation are located at regular intervals from Cylinder 0. The conditions for auto-reallocation are described below.

Nonrecovered write errors

When a write operation can not be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation fails.

If the number of available spare sectors reaches 16 sectors, the write cache function will be disabled automatically.

Nonrecovered read errors

When a read operation fails after a defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verifications is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector fails once and then is recovered at the specific ERP step, this sector of data is reallocated automatically. A media verification sequence may be run prior to the relocation according to the predefined conditions.

11.16 48-bit Address Feature Set

The 48-bit Address feature set allows devices with capacities up to 281,474,976,710,655 sectors. This allows device capacity up to 144,115,188,075,855,360 bytes. In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector count to 16 bits.

Commands unique to the 48-bit Address feature set are:

- Flush Cache Ext
- Read DMA Ext
- Read Multiple Ext
- Read Native Max Address Ext
- Read Sector(s) Ext
- Read Verify Sector(s) Ext
- Set Max Address Ext
- Write DMA Ext
- Write Multiple Ext
- Write Sector(s) Ext

The 48-bit Address feature set operates in LBA addressing only. Devices also implement commands using 28-bit addressing, and 28-bit and 48-bit commands may be intermixed.

In a device, the Features, the Sector Count, the LBA Low/Mid/High registers are a two-byte-deep FIFO. Each time one of these registers is written, the new content written is placed into the "most recently written" location and the previous content is moved to "previous content" location.

The host may read the "previous content" of the Features, the Sector Count, the LBA Low/Mid/High registers by first setting the High Order Bit (HOB, bit 7) of the Device control register to one and then reading the desired register. If HOB in the Device Control register is cleared to zero, the host reads the "most recently written" content when the register is read. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The "most recently written" content always gets written by a register write regardless of the state of HOB in the Device Control register.

Support of the 48-bit Address feature set is indicated in the Identify Device response bit 10 word 83. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in Identify Device response words 100 through 103.

When the 48-bit Address feature set is implemented, the native maximum address is the value returned by a Read Native Max Address Ext command. If the native maximum address is equal to or less than 268,435,455, a Read Native Max Address shall return the native maximum address. If the native maximum address is greater than 268,435,455, a Read Native Max Address shall return a value of 268,435,455.

12.0 Command protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check to see if BSY = 1, and should proceed no further unless and until BSY = 0. For all commands, the host must also wait for RDY = 1 before proceeding.

A device must maintain either BSY = 1 or DRQ = 1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY = 1 or DRQ = 1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

See Section 14.0, “Time-out values” on page 191 for the device time-out values.

12.1 Data In commands

The following are Data In commands:

- Device Configuration Identify
- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Multiple EXT
- Read Sector(s)
- Read Sector(s) EXT
- S.M.A.R.T. Read Attribute Values
- S.M.A.R.T. Read Attribute Thresholds
- S.M.A.R.T. Read log sector

Execution includes the transfer of one or more 512-byte (> 512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, LBA, Cylinder, and Device Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
   a. The device sets BSY = 1 and prepares for data transfer.
   b. When a sector (or block) of data is available for transfer to the host, the device sets BSY = 0, sets DRQ = 1, and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads one sector (or block) of data via the Data Register.

f. The device sets DRQ = 0 after the sector (or block) has been transferred to the host.

4. For the Read Long command:
   a. The device sets BSY = 1 and prepares for data transfer.
   b. When the sector of data is available for transfer to the host, the device sets BSY = 0 and DRQ=1 and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads the sector of data including ECC bytes via the Data Register.
   f. The device sets DRQ = 0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, it aborts the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an error occurs, the device sets BSY = 0, ERR = 1, and DRQ = 1. The device then stores the error status in the Error Register and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported using CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register upon issuing the command.

If an Uncorrectable Data Error (UNC = 1) occurs, the defective data is transferred from the media to the sector buffer and is available for transfer to the host at the host's option. In case of a Read Multiple command, the host should complete transfer of the block which includes the error from the sector buffer and terminate whatever type of error that occurred.

All data transfers to the host through the Data Register are 16 bits except ECC bytes which are 8 bits.

12.2 Data Out Commands

The following are Data Out commands:

- Device Configuration SET
- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Set Max SET PASSWORD
- Set Max UNLOCK
- S.M.A.R.T. Write log sector
- Write Buffer
- Write Long
- Write Multiple
- Write Multiple EXT

- Write Sector(s)
- Write Sector(s) EXT
- Write Verify

Execution includes the transfer of one or more 512 byte (> 512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, LBA, and Device Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY = 1.
4. For each sector (or block) of data to be transferred:
   a. The devices BSY = 0 and DRQ = 1 when it is ready to receive a sector (or block).
   b. The host writes one sector (or block) of data via the Data Register.
   c. The device sets BSY = 1 after it has received the sector (or block).
   d. When the device has finished processing the sector (or block), it sets BSY = 0 and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt to the Status Register being read.
5. For the Write Long Command:
   a. The device sets BSY = 0 and DRQ = 1 when it is ready to receive a sector.
   b. The host writes one sector of data including ECC bytes via the Data Register.
   c. The device sets BSY = 1 after it has received the sector.
   d. After processing the sector of data, the device sets BSY = 0 and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it aborts the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an uncorrectable error occurs, the device sets BSY = 0 and ERR = 1, stores the error status in the Error Register, and interrupts the host. The registers will contain the location of the sector in error. The error location will be reported with CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register on issuing the command.

All data transfers to the host through the Data Register are 16 bits except for the ECC bytes which are 8 bits.

12.3 Non-data commands

The following are Non-data commands:

- Check Power Mode
- Device Configuration FREEZE LOCK
- Device Configuration RESTORE
- Execute Device Diagnostic
- Flush Cache

- Flush Cache EXT
- Format Unit
- Idle
- Idle Immediate
- Initialize Device Parameters
- Read Native Max ADDRESS
- Read Native Max ADDRESS EXT
- Read Verify Sector(s)
- Read Verify Sector(s) EXT
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Sense Condition
- Set Features
- Set Max ADDRESS
- Set Max ADDRESS EXT
- Set Max LOCK
- Set Max FREEZE LOCK
- Set Multiple Mode
- Sleep
- S.M.A.R.T. Disable Operations
- S.M.A.R.T. Enable/Disable Attribute Auto save
- S.M.A.R.T. Enable/Disable Automatic Off-line
- S.M.A.R.T. Enable Operations
- S.M.A.R.T. Execute Off-line Immediate
- S.M.A.R.T. Return Status
- S.M.A.R.T. Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer:

a. The host writes any required parameters to the Features, Sector Count, LBA High, LBA Mid, LBA Low, and Device Registers.

b. The host writes the command code to the Command Register.

c. The device sets BSY = 1.

d. When the device has finished processing the command, it sets BSY = 0 and interrupts the host.

e. In response to the interrupt, the host reads the Status Register.

f. The device clears the interrupt in response to the Status Register being read.

12.4 DMA Data Transfer commands:

The following are DMA Data Transfer commands:

- Read DMA
- Read DMA EXT
- Write DMA
- Write DMA EXT

Data transfers using DMA commands differ in two ways from PIO transfers:

- Data transfers are performed using the Slave DMA channel
- No intermediate sector interrupts are issued on multisector commands.

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands with one exception: the host initializes the Slave DMA channel prior to issuing the command.

The interrupt handler for DMA transfers differs in two ways:

- No intermediate sector interrupts are issued on multisector commands.
- The host resets the DMA channel prior to reading status from the device

The DMA protocol allows high performance multitasking operating systems to eliminate processor overhead associated with PIO transfers.

1. The host initializes the Slave DMA channel.
2. The host writes any required parameters to the Features, Sector Count, LBA High, LBA Mid, LBA Low, and Device registers.
3. The host writes command code to the Command Register.
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. The host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. The host resets the Slave DMA channel.
8. The host reads the Status Register and, optionally, the Error Register.

Refer to Section 7.0, “Electrical interface specification” on page 39 for further details.

13.0 Command descriptions

The table below shows the commands that are supported by the device. Table 59: “Command Set (subcommand)” on page 100 shows the subcommands that are supported by each command or feature.

Table 57: Command Set (1 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Check Power Mode	E5	1 1 1 0 0 1 0 1
3	Check Power Mode*	98	1 0 0 1 1 0 0 0
3	Device Configuration RESTORE	B1	1 0 1 0 0 0 0 1
3	Device Configuration FREEZE LOCK	B1	1 0 1 0 0 0 0 1
1	Device Configuration IDENTIFY	B1	1 0 1 0 0 0 0 1
2	Device Configuration SET	B1	1 0 1 0 0 0 0 1
3	Execute Device Diagnostic	90	1 0 0 1 0 0 0 0
3	Flush Cache	E7	1 1 1 0 0 1 1 1
3	Flush Cache EXT	EA	1 1 1 0 1 0 1 0
2	Format Track	50	0 1 0 1 0 0 0 0
3+	Format Unit	F7	1 1 1 1 0 1 1 1
1	Identify Device	EC	1 1 1 0 1 1 0 0
3	Idle	E3	1 1 1 0 0 0 1 1
3	Idle*	97	1 0 0 1 0 1 1 1
3	Idle Immediate	E1	1 1 1 0 0 0 0 1
3	Idle Immediate*	95	1 0 0 1 0 1 0 1
3	Initialize Device Parameters	91	1 0 0 1 0 0 0 1
1	Read Buffer	E4	1 1 1 0 0 1 0 0
4	Read DMA	C8	1 1 0 0 1 0 0 0
4	Read DMA	C9	1 1 0 0 1 0 0 1
4	Read DMA EXT	25	0 0 1 0 0 1 0 1
1	Read Long	22	0 0 1 0 0 0 1 0
1	Read Long	23	0 0 1 0 0 0 1 1
1	Read Multiple	C4	1 1 0 0 0 1 0 0
3	Read Native Max ADDRESS	F8	1 1 1 1 1 0 0 0
3	Read Native Max ADDRESS EXT	27	0 0 1 0 0 1 1 1
1	Read Sector(s)	20	0 0 1 0 0 0 0 0
1	Read Sector(s)	21	0 0 1 0 0 0 0 1
3	Read Sector(s)EXT	24	0 0 1 0 0 1 0 0
3	Read Verify Sector(s)	40	0 1 0 0 0 0 0 0
3	Read Verify Sector(s)	41	0 1 0 0 0 0 0 1
3	Read Verify Sector(s)EXT	42	0 1 0 0 0 0 1 0
3	Recalibrate	1x	0 0 0 1 - - - -
2	Security Disable Password	F6	1 1 1 1 1 0 1 0
3	Security Erase Prepare	F3	1 1 1 1 0 0 1 1
2	Security Erase Unit	F4	1 1 1 1 0 1 0 0
3	Security Freeze Lock	F5	1 1 1 1 0 1 0 1
2	Security Set Password	F1	1 1 1 1 0 0 0 1
2	Security Unlock	F2	1 1 1 1 0 0 1 0
3	Seek	7x	0 1 1 1 - - - -
3	Sense Condition	F0	1 1 1 1 0 0 0 0

Table 58: Command Set (2 of 2)

Proto-col	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0

3	Set Features	EF	1 1 1 0 1 1 1 1
3	Set Max ADDRESS	F9	1 1 1 1 1 0 0 1
3	Set Max ADDRESS EXT	37	0 0 1 1 0 1 1 1
3	Set Max FREEZE LOCK	F9	1 1 1 1 1 0 0 1
3	Set Max LOCK	F9	1 1 1 1 1 0 0 1
2	Set Max SET PASSWORD	F9	1 1 1 1 1 0 0 1
2	Set Max UNLOCK	F9	1 1 1 1 1 0 0 1
3	Set Multiple Mode	C6	1 1 0 0 0 1 1 0
3	Sleep	E6	1 1 1 0 0 1 1 0
3	Sleep*	99	1 0 0 1 1 0 0 1
3	S.M.A.R.T. Disable Operations	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable/Disable Attribute Auto save	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable/Disable Automatic Off-line	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Enable Operations	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Execute Off-line Immediate	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Attribute Values	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Attribute Thresholds	B0	1 0 1 1 0 0 0 0
1	S.M.A.R.T. Read Log Sector	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Return Status	B0	1 0 1 1 0 0 0 0
3	S.M.A.R.T. Save Attribute Values	B0	1 0 1 1 0 0 0 0
2	S.M.A.R.T. Write Log Sector	B0	1 0 1 1 0 0 0 0
3	Standby	E2	1 1 1 0 0 0 1 0
3	Standby*	96	1 0 0 1 0 1 1 0
3	Standby Immediate	E0	1 1 1 0 0 0 0 0
3	Standby Immediate*	94	1 0 0 1 0 1 0 0
2	Write Buffer	E8	1 1 1 0 1 0 0 0
4	Write DMA	CA	1 1 0 0 1 0 1 0
4	Write DMA	CB	1 1 0 0 1 0 1 1
4	Write DMA EXT	35	0 0 1 1 0 1 0 1
2	Write Long	32	0 0 1 1 0 0 1 0
2	Write Long	33	0 0 1 1 0 0 1 1
2	Write Multiple	C5	1 1 0 0 0 1 0 1
2	Write Multiple EXT	39	0 0 1 1 1 0 0 1
2	Write Sector(s)	30	0 0 1 1 0 0 0 0
2	Write Sector(s)	31	0 0 1 1 0 0 0 1
2	Write Sector(s)EXT	34	0 0 1 1 0 1 0 0
2	Write Verify	3C	0 0 1 1 1 1 0 0

Commands marked * are alternate command codes for previously defined commands

Protocol: 1 : PIO data IN command 3 : Non data command + : Vendor specific command
2 : PIO data OUT command 4 : DMA command

Table 59: Command Set (subcommand)

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
S.M.A.R.T. Function		
S.M.A.R.T. Read Attribute Values	B0	D0
S.M.A.R.T. Read Attribute Thresholds	B0	D1
S.M.A.R.T. Enable/Disable Attribute Autosave	B0	D2
S.M.A.R.T. Save Attribute Values	B0	D3
S.M.A.R.T. Execute Off-line Immediate	B0	D4
S.M.A.R.T. Read Log Sector	B0	D5
S.M.A.R.T. Write Log Sector	B0	D6
S.M.A.R.T. Enable Operations	B0	D8
S.M.A.R.T. Disable Operations	B0	D9
S.M.A.R.T. Return Status	B0	DA
S.M.A.R.T. Enable/Disable Automatic Off-line	B0	DB
Set Features		
Enable Write Cache	EF	02
Set Transfer mode	EF	03
Enable Advanced Power Management feature	EF	05
Enable Power-Up in Standby feature	EF	06
Power-Up in Standby feature device Spin-Up	EF	07
Enable Address Offset mode	EF	09
Enable Automatic Acoustic management (AAM)	EF	42
51 bytes of ECC apply on Read/Write Long	EF	44
Disable read look-ahead feature	EF	55
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management feature	EF	85
Disable Power-Up in Standby feature	EF	86
Disable Address Offset mode	EF	89
Enable read look-ahead feature	EF	AA
4 bytes of ECC apply on Read/Write Long	EF	BB
Disable AAM	EF	C2
Enable reverting to power on defaults	EF	CC
Set Max Security Extension		
Set Max SET PASSWORD	F9	01
Set Max LOCK	F9	02
Set Max UNLOCK	F9	03
Set Max FREEZE LOCK	F9	04
Device Configuration Overlay		
Device Configuration RESTORE	B1	CO
Device Configuration FREEZE LOCK	B1	C1
Device Configuration IDENTIFY	B1	C2
Device Configuration SET	B1	C3

The "Command set" table beginning on page page 98 shows the commands that are supported by the device. The "Command Set (Subcommand)" table above shows the sub-commands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Input registers

0	This indicates that the bit is always set to 0.
1	This indicates that the bit is always set to 1.
H	Head number. This indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
V	Valid. This indicates that the bit is part of an input parameter and will be set by the device to 0 or 1.
N	Not recommended condition for start up. Indicates that the condition of the device is not recommended for start up.
-	This indicates that the bit is not part of an input parameter.

Out put registers

0	This indicates that the bit must be set to 0.
1	This indicates that the bit must be set to 1.
D	The device number bit. This indicates that the device number bit of the Device Register should be specified. Zero selects the master device and one selects the slave device.
H	Head number. This indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
L	LBA mode. This indicates the addressing mode. Zero specifies CHS mode and one specifies LBA addressing mode.
R	Retry. Original meaning is already obsolete, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)
B	Option Bit. This indicates that the Option Bit of the Sector Count Register be specified. (This bit is used by Set Max ADDRESS command.)
V	Valid. This indicates that the bit is part of an output parameter and should be specified.
x	This indicates that the hex character is not used.
-	This indicates that the bit is not used.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

13.1 Check Power Mode (E5h/98h)

Table 60: Check Power Mode Command (E5h/98h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	V V V V V V V V
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	0	0	-	-	0	-	V

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input parameters from the device

Sector Count This indicates the power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register is set to 0.

13.2 Device Configuration Overlay (B1h)

Table 61: Device Configuration Overlay Command (B1h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	1 0 1 0 V V V V		Error	see below
Sector Count	- - - - - - - -		Sector Count	V V V V V V V V
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Low	V V V V V V V V
LBA High	- - - - - - - -		LBA High	V V V V V V V V
Device	- - - D - - - -		Device	- - - - - - - -
Command	1 0 1 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		V	V	0	-	V	-	-	V

Individual Device Configuration Overlay feature set commands are identified by the value placed in the Features register. The table below shows these Features register values.

Table 62: Device Configuration Overlay Features register values

Value	Command
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE LOCK
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET
other	Reserved

13.2.1 DEVICE CONFIGURATION RESTORE (subcommand C0h)

The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command.

13.2.2 DEVICE CONFIGURATION FREEZE LOCK (subcommand C1h)

The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the device. The DEVICE CONFIGURATION FREEZE LOCK condition shall be cleared by a power-down. The DEVICE CONFIGURATION FREEZE LOCK condition shall not be cleared by hardware or software reset.

13.2.3 DEVICE CONFIGURATION IDENTIFY (subcommand C2h)

The DEVICE CONFIGURATION IDENTIFY command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command will reflect the reduced set of capabilities, while the DEVICE CONFIGURATION IDENTIFY command will reflect the entire set of selectable capabilities.

The format of the Device Configuration Overlay data structure is shown in Table 63: “Device Configuration Overlay Data structure” on page 105.

13.2.4 DEVICE CONFIGURATION SET (subcommand C3h)

The DEVICE CONFIGURATION SET command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The DEVICE CONFIGURATION SET command transfers an overlay that modifies some of the bits set in words 63, 82, 83, 84, and 88 of the IDENTIFY DEVICE command response. When the bits in these words are cleared, the device no longer supports the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit.

The format of the overlay transmitted by the device is described in the table in Table 63: “Device Configuration Overlay Data structure” on page 105. The restrictions on changing these bits is described in the text following that table. If any of the bit modification restrictions described are violated or any setting is changed with DEVICE CONFIGURATION SET command, the device shall return command aborted. In that case, error reason code is returned to sector count register, invalid word location is returned to LBA high register, and invalid bit location is returned to LBA Mid register. The Definition of error information is shown in Table 64: “DCO error information definition.” on page 105.

ERROR INFORMATION EXAMPLE 1:

After establishing a protected area with SET MAX address, if a user attempts to change maximum LBA address (DC SET or DC RESTORE), the device aborts that command and returns error reason code as below.

LBA High	:	03h	= word 3 is invalid
LBA Mid	:	00h	this register is not assigned in this case
Sector count	:	06h	= Protected area is now established

ERROR INFORMATION EXAMPLE 2:

When the device is enabled and the Security feature is set, if the user attempts to disable that feature, the device aborts that command and returns an error reason code as below.

LBA High	:	07h	= word 7 is invalid
LBA Mid	:	03h	= bit 3 is invalid
Sector count	:	04h	= now Security feature set is enabled

Table 63: Device Configuration Overlay Data structure

Word	Content	
0	0001h	Data Structure revision
1	Multiword DMA modes supported	
	15-3	Reserved
	2	1 = Multiword DMA mode 2 and below are supported
	1	1 = Multiword DMA mode 1 and below are supported
	0	1 = Multiword DMA mode 0 is supported
2	Ultra DMA modes supported	
	15-6	Reserved
	5	1 = Ultra DMA mode 5 and below are supported
	4	1 = Ultra DMA mode 4 and below are supported
	3	1 = Ultra DMA mode 3 and below are supported
	2	1 = Ultra DMA mode 2 and below are supported
	1	1 = Ultra DMA mode 1 and below are supported
	0	1 = Ultra DMA mode 0 is supported
3-6	Maximum LBA address	
7	Command set/feature set supported	
	15-9	Reserved
	8	1 = 48-bit Addressing feature set supported
	7	Reserved
	6	1 = Automatic acoustic management supported
	5	Reserved
	4	1 = Power-Up in Standby feature set supported
	3	1 = SMART feature set supported
	2	1 = SMART error log supported
	1	1 = SMART sefl-test supported
	0	1 = SMART feature set supported
8-254	Reserved	
255	Integrity word *See note below*	
	15-8	Checksum
	7-0	Signature (A5h)

Note: Bits 7–0 of this word contain the value A5h. Bits 15–8 of this word contain the data structure checksum. The data structure checksum is the two's complement of the sum of all byte in words 0through 254 and the byte consisting of bits 7–0 of word 255. Each byte is added with unsigned arithmetic, and overflow is ignored. The sum of all bytes is zero when the checksum is correct.

Table 64: DCO error information definition.

LBA High	invalid word location
LBA Mid	invalid bit location (bits 7:0)
Sector count	error reason code & description (bits 15:8) 01h DCO feature is frozen 02h Device is now Security Locked mode 03h Device's feature is already modified with DCO 04h User attempt to disable any feature enabled 05h Device is now SET MAX Locked or Frozen mode 06h Protected area is now established 07h DCO is not supported 08h Subcommand code is invalid FFh other reason

13.3 Execute Device Diagnostic (90h)

Table 65: Execute Device Diagnostic command (90h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 - - - - -		Device	- - - - - - - -
Command	1 0 0 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	V	V	V	V		0	0	0	-	-	0	-	0

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Table 46: “Diagnostic codes” on page 70 for the definition.

13.4 Flush Cache (E7h)

Table 66: Flush Cache command (E7h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns a status of RDY = 1 and DSC = 1 (50h) after the following sequence:

- Data in the write cache buffer is written to the disk media.
- Return a successful completion

13.5 Flush Cache EXT (EAh)

Table 67: Flush Cache command (E7h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - -		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
LBA Low	Current	- - - - - - - -		LBA Low	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
LBA Mid	Current	- - - - - - - -		LBA Mid	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
LBA High	Current	- - - - - - - -		LBA High	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Device/Head		- - - D - - - -		Device/Head		- - - - - - - -
Command		1 1 1 0 1 0 1 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

13.6 Format Track (50h: vendor specific)

Table 68: Format Track command (50h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	0 1 0 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with the write operation. At this time, the read operation does not verify the correct initialization of the data sector. Any data previously stored on the track will be lost.

Output parameters to the device

LBA Low In LBA mode this register specifies that LBA address bits 0–7 are to be formatted. (L=1).

LBA High/Mid This indicates the cylinder number of the track to be formatted. (L = 0)

In LBA mode this register specifies that LBA address bits 8–15 (Mid) and bits 16–23 (High) are to be formatted. (L = 1)

H This indicates the head number of the track to be formatted (L = 0). In LBA mode this register specifies that LBA address bits 24–27 are to be formatted. (L= 1)

Input parameters from the device

LBA Low In LBA mode this register specifies the current LBA address bits as 0–7 (L = 1).

LBA High/Mid In LBA mode this register specifies the current LBA address bits as 8–15 (Mid) and bits 16–23 (High).

H In LBA mode this register specifies the current LBA address bits as 24–27 (L=1).

In LBA mode this command formats a single logical track including the specified LBA.

13.7 Format Unit (F7h: vendor specific)

Table 69: Format Unit command (F7h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Format Unit command initializes all user data sectors after merging the reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available immediately after the completion of this command. They are also used on the next power on reset or hard reset. This command erases both previous information data from the device.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA is set by Initialize Drive Parameter or Set MAX ADDRESS command is ignored. The protected area by Set MAX ADDRESS command is also initialized.

The Security Erase Prepare command should be completed immediately prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command, the device aborts the Format Unit command.

If the Feature register is NOT 11h, the device returns an Abort error to the host.

This command does not request a data transfer.

Output parameters to the device

Feature This indicates the Destination code for this command

11H The merge reassigned location into the defect information.

The execution time of this command is shown below.

Model number	Execution time
HTS541010G9AT00	64 min
HTS541080G9AT00	52 min
HTS541060G9AT00	40 min
HTS541040G9AT00	26 min
HTS541030G9AT00	22 min
HTS541020G9AT00	14 min

13.8 Identify Device (ECh)

Table 70: Identify Device command (ECh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 1 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Table 71 beginning on page 112.

Table 71: Identify device information. (Part 1 of 7)

Word	Content		Description	
00	045AH		**drive classification**	**bit assignments**
			15(=0)	1=ATAPI device, 0=ATA device
		*	14(=0)	1=format speed tolerance gap required
		*	13(=0)	1=track offset option available
		*	12(=0)	1=data strobe offset option available
		*	11(=0)	1=rotational speed tolerance > 0.5%
		*	10(=1)	1=disk transfer rate > 10 Mbps
		*	9(=0)	1=disk transfer rate > 5 Mbps but <= 10 Mbps
		*	8(=0)	1=disk transfer rate <= 5 Mbps
			7(=0)	1=removable cartridge drive
			6(=1)	1=fixed drive
		*	5(=0)	1=spindle motor control option implemented
		*	4(=1)	1=head switch time > 15 ms
		*	3(=1)	1=not MFM encoded
			2(=0)	1=identify data incomplete
		*	1(=1)	1=hard sectored
			0(=0)	Reserved
01	(Note 1)		Number of cylinders in default translate mode	
02	xxxxH		Specific configuration	
			C837h	SET FEATURES subcommand is not required to spin-up and IDENTIFY DEVICE response is complete
			37C8h	SET FEATURES subcommand is required to spin-up and IDENTIFY DEVICE response is complete
03	(Note 1)		Number of heads in default translate mode	
04-05	0	*	Reserved	
06	003FH		Number of sectors per track in default translate mode	
07-09	0		Reserved	
10-19	XXXX		Serial number in ASCII (0 = not specified)	
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read	
21	(Note 1)	*	Buffer size in 512-byte increments	
22	00XXH	*	Number of ECC bytes as currently selected via the set feature command	
23-26	XXXX		Micro code version in ASCII	
27-46	(Note 1)		Model number in ASCII	
47	8010H		Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands 15-8: (=80h) 7-0: Maximum number of sectors that can be transferred per interrupt.	

* indicates the use of those parameters that are vendor specific.

Note 1. See Table 78: “Number of cylinders/heads/sectors by model.” on page 119.

Table 72: Identify device information. (Part 2 of 7)

Word	Content		Description
48	0000H	*	Capable of double word I/O, '0000'= cannot perform
49	0F00H		Capabilities, bit assignments: 15-14(=0) Reserved 13(=0) Standby timer value are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) Reserved 8(=0) Reserved
		*	7-0(=0) Reserved
50	4000H		Capabilities 15(=0) 0=the contents of word 50 are valid 14(=1) 1=the contents of word 50 are valid 13- 1(=0) Reserved 0(=0) 1=the device has a minimum Standby timer value that is device specific
51	0200H	*	PIO data transfer cycle timing mode
52	0200H	*	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0007H		Validity flag of the word 15- 3(=0) Reserved 2(=1) 1 Word 88 is Valid 1(=1) 1=Word 64-70 are Valid 0(=1) 1=Word 54-58 are Valid
54	XXXXH		Number of current cylinders
55	XXXXH		Number of current heads
56	XXXXH		Number of current sectors per track
57-58	XXXXH		Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH		Current Multiple setting. Bit assignments: 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	(Note 1)		Total Number of User Addressable Sectors Word 60 specifies the low word of the number FFFFFFFh=the 48-bit native max address is greater than 268,435,455
62	0000H	*	Reserved
63	0X07H		Multiword DMA Transfer Capability 15-11 (=0) Reserved 10 1=Multiword DMA mode 2 is selected 9 1=Multiword DMA mode 1 is selected 8 1=Multiword DMA mode 0 is selected 7- 3 (=0) Reserved 2 1=Multiword DMA mode 2 is supported 1 1=Multiword DMA mode 1 is supported 0 1=Multiword DMA mode 0 is supported

* indicates the use of those parameters that are vendor specific.

Note 1. See Table 78: “Number of cylinders/heads/sectors by model.” on page 119.

Table 73: Identify device information. (Part 3 of 7)

Word	Content	Description
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=F0h) Cycle time in nanoseconds (240 ns, 8.3 MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
69-79	0000H	Reserved
80	007CH	Major version number - ATA-1,2,3 and ATA/ATAPI-4,5,6
81	0019h	Minor version number - ATA/ATAPI-6 T13 1410D Revision 3a
82	746BH	Command set supported 15(=0) Reserved 14(=1) 1=NOP command supported 13(=1) 1=READ BUFFER command supported 12(=1) 1=WRITE BUFFER command supported 11(=0) Reserved **10(=1) 1=Host Protected Area Feature Set supported 9(=0) 1=DEVICE RESET command supported 8(=0) 1=SERVICE interrupt supported 7(=0) 1=release interrupt supported 6(=1) 1=look-ahead supported 5(=1) 1=write cache supported 4(=0) 1=supports PACKET Command Feature Set 3(=1) 1=supports Power Management Feature Set 2(=0) 1=supports Removable Media Feature Set ** 1(=1) 1=supports Security Feature Set ** 0(=1) 1=supports S.M.A.R.T. Feature Set

** indicates a feature that is able to be unsupported by the Device Configuration Overlay command.

Table 74: Identify device information. (Part 4 of 7)

Word	Content		Description
83	7FE8H	*	Command set supported 15(=0) Always 14(=1) Always 13(=1) 1=FLUSH CACEH EXT command supported 12(=1) 1=FLUSH CACHE command supported 11(=1) 1=Device Configuration Overlay command supported 10(=1) 1=48-bit Address feature set supported 9(=1) 1=Automatic Acoustic Management supported ** 8(=1) 1=SET MAX security extension supported ** 7(=1) 1=Address Offset feature supported 6(=1) 1=SET FEATURES subcommand required to spin-up 5(=1) 1=Power-Up In Standby feature set supported 4(=0) 1=Removable Media Status Notification Feature Set supported 3(=1) 1=Advanced Power Management Feature Set supported 2(=0) 1=CFA Feature Set supported 1(=0) 1=READ/WRITE DMA QUEUED supported 0(=0) 1=DOWNLOAD MICROCODE command supported
84	4023H		Command set/feature supported extension 15(=0) Always 14(=1) Always 13- 6(=0) Reserved 5(=1) 1=General Purpose Logging feature set supported 4-2(=0) Reserved ** 1(=1) 1=SMART self-test supported ** 0(=1) 1=SMART error logging supported
85	F4XXH		Command set/feature enabled 15(=1) Reserved 14(=1) 1=NOP command supported 13(=1) 1=READ BUFFER command supported 12(=1) 1=WRITE BUFFER command supported 11(=0) Reserved **10(=1) 1=Host Protected Area Feature Set supported 9(=0) 1=DEVICE RESET command supported 8(=0) 1=SERVICE interrupt enabled 7(=0) 1=release interrupt enabled 6(=X) 1=look-ahead enabled 5(=X) 1=write cache enabled 4(=0) 1=supports PACKET Command Feature Set 3(=X) 1=supports Power Management Feature Set 2(=0) 1=supports Removable Media Feature Set 1(=X) 1=Security Feature Set enabled 0(=X) 1=S.M.A.R.T. Feature Set enabled

* indicates the use of those parameters that are vendor specific.

** indicates a feature that is able to be unsupported by the Device Configuration Overlay command.

Table 75: Identify device information. (Part 5 of 7

Word	Content		Description
86	3XXXH		Command set/feature enabled
		*	15-14(=0) Reserved
			13(=1) 1=FLUSH CACHE EXT command supported
		*	12(=1) 1=FLUSH CACHE command supported
			11(=x) 1=Device Configuration Overlay supported
		*	10(=1) 1=48-bit Address feature set supported
			9(=X) 1=Automatic Acoustic Management enabled
			8(=X) 1=SET MAX security extension enabled
			7(=X) 1=Address Offset mode enabled
			6(=1) 1=SET FEATURES subcommand required to spin-up
			5(=X) 1=Power-Up In Standby feature set has been enabled via the SET FEATURES command
			4(=0) 1=Removable Media Status Notification Feature Set enabled
			3(=X) 1=Advanced Power management Feature Set enabled
			2(=0) 1=CFA Feature Set supported
			1(=0) 1=READ/WRITE DMA QUEUED command supported
			0(=0) 1=DOWNLOAD MICROCODE command supported
87	4023H		Command set/feature enabled
			15(=0) Always
			14(=1) Always
			13-6(=0) Reserved
			5(=1) 1=General Purpose Logging feature set supported
			4-2(=0) Reserved
			1(=1) 1=SMART self-test supported
			0(=1) 1=SMART error logging supported
88	XX3FH		Ultra DMA Transfer mode (mode 5 supported)
			15-14(=0) Reserved
			13(=X) 1=UltraDMA mode 5 is selected
			12(=X) 1=UltraDMA mode 4 is selected
			11(=X) 1=UltraDMA mode 3 is selected
			10(=X) 1=UltraDMA mode 2 is selected
			9(=X) 1=UltraDMA mode 1 is selected
			8(=X) 1=UltraDMA mode 0 is selected
			7- 6(=0) Reserved
			**5(=1) 1=UltraDMA mode 5 is selected
			**4(=1) 1=UltraDMA mode 4 is supported
			**3(=1) 1=UltraDMA mode 3 is supported
			**2(=1) 1=UltraDMA mode 2 is supported
			**1(=1) 1=UltraDMA mode 1 is supported
			0(=1) 1=UltraDMA mode 0 is supported
89	XXXXH		Time required for security erase unit completion
			Time= value (XXXXh)*2 [minutes]
90	0000H		Time required for Enhanced security erase completion
			0000 : Not supported

* indicates the use of those parameters that are vendor specific.

** indicates a feature that is able to be unsupported by the Device Configuration Overlay command.

Table 76: Identify device information. (Part 6 of 7)

Word	Content	Description
91	40XXH	Current Advanced Power Management level 15- 8(=40h) Reserved 7- 0(=xxh) Current Advanced Power Management level set by Set Features Command (01h to FEh)
92	XXXXH	Current Master Password Revision Codes
93	XXXXH	Hardware reset results 15-13 Device detected result 15(=0) Reserved 14(=1) Always 13(=X) 1=Device detected CBLID- above V_{iH} 0=Device detected CBLID- below V_{iL} 12- 8 Device 1 hardware reset result Device 0 clear these bits to 0 12(=0) Reserved 11(=X) 1=Device 1 passed diagnostic 10-9(=X) How Device 1 determined the device number: 00= Reserved 01= a jumper was used 10= the CSEL signal was used 11= some other method used or method unknown 8(=1) Always 7- 0 Device 0 hardware reset result Device 1 clears these bits to 0 7(=0) Reserved 6(=X) 1=Semi-duplex mode is enabled 5(=X) 1=Device 0 detected Device 1 4(=X) 1=Device 1 passed diagnostic 3(=X) 1=Device 0 passed diagnostic 2-1(=X) how Device 0 determined the device number: 00=Reserved 01=a jumper was used 10=the CSEL signal was used 11=some other method used or the method unknown 0(=1) Always
94	80XXH	Automatic Acoustic Management value 15- 8 Vendor’s Recommended Acoustic Management level 7- 0 Current Automatic Acoustic Management level Default value if FEh
95-99	0000H	Reserved
100-103	Note 1	Maximum user LBA address for 48-bit Address feature set
104-126	0000H	Reserved
127	0000H	Removable Media Status Notification feature set

Note 1. See Table 78: “Number of cylinders/heads/sectors by model.” on page 119.

Table 77: Identify device information. (Part 7 of 7)

Word	Content		Description
128	0XXXH		Security Mode Feature. Bit assignments 15-9(=0) Reserved 8(=X) Security Level: 1= Maximum, 0= High 7-6(=0) Reserved 5(=0) 1=Enhanced security erase supported 4(=0) 1=Security count expired 3(=0) 1=Security Frozen 2(=0) 1=Security Locked 1(=0) 1=Security Enabled **0(=0) 1=Security Support
129	000XH	*	Current Set Feature Option. Bit assignments 15-4(=0) Reserved 3(=X) 1=Auto reassign enabled 2(=X) 1=Reverting enabled 1(=X) 1=Read Look-ahead enabled 0(=X) 1=Write Cache enabled
130	XXXXH	*	Reserved
131	000XH	*	Initial Power Mode Selection. Bit assignments 15-2(=0) Reserved 1(=1) Always 0(=X) Initial Power Mode: 1=Standby, 0=Idle
132-254	XXXXH	*	Reserved
255	XXA5H		Integrity word 15-8(=XXh) Checksum 7-0(=A5h) Signature

* indicates the use of those parameters that are vendor specific.

Table 78: Number of cylinders/heads/sectors by model.

Microcode revision	MBxIAxx	MBx0Axxx	MBxAAxxx
HTS541010G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	BA52230h	BA52230h	BA52230h
HTS541080G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	950F8B0h	950F8B0h	950F8B0h
HTS541060G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	6FC7C80h	6FC7C80h	6FC7C80h
HTS541040G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	4A85300h	4A85300h	4A85300h
HTS541030G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	37E3E40h	37E3E40h	37E3E40h
HTS541020G9AT00			
Number of cylinders	3FFFh	3FFFh	3FFFh
Number of heads	10h	10h	10h
Buffer size	3AE6h	3AE6h	3AE6h
Total number of user addressable sectors	2542980h	37E3E40h	37E3E40h

For the microcode revision refer to word 23-26 in 13.8 “Identify Device (ECh)” on page 111. This is 8 characters in ASCII.

13.9 Idle (E3h/97h)

Table 79: Idle command (E3h/97h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 0 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

When the power save mode is Standby mode, the Idle command causes the device to enter Performance Idle mode immediately and sets the auto power down time-out Parameter (standby timer). At the set of the auto power down time-out parameter (standby timer) the point timer starts counting down. When the power save mode is already any idle mode, the device remains in that mode.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and is ready to respond to host commands immediately.

Input parameters to the device

Sector Count This indicates the Time-out Parameter. If it is zero, the time-out interval (Standby Timer) is disabled. If it is other than zero, the time-out interval is set for (Time-out Parameter × 5) seconds.

The device will enter Standby mode automatically if the time-out interval expires with no device access from the host. The time-out interval will be reinitialized if there is a device access before the time-out interval expires.

13.10 Idle Immediate (E1h/95h)

Table 80: Idle Immediate command (E1h/95h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Idle Immediate command causes the device to enter Performance Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to the host commands immediately.

The Idle Immediate command will not affect the auto power down time-out parameter.

13.11 Initialize Device Parameters (91h)

Table 81: Initialize Device Parameters command (91h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	- - - - - - - -
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D H H H H		Device	- - - - - - - -
Command	1 0 0 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	0	0	-	-	0	-	V

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54–58 in Identify Device Information reflects these parameters.

The parameters remain in effect until the following events occur:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- A hard reset occurs.
- A soft reset occurs and the Set Feature option of CCh is set.

Output parameters to the device

Sector Count This indicates the number of sectors per track. Zero (0) indicates 0 sectors per track instead of 256 sectors per track. It means that there are no sectors per track.

H This indicates the number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

13.12 Read Buffer (E4h)

Table 82: Read Buffer (E4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Read Buffer command transfers a sector of data from the sector buffer of the device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

13.13 Read DMA (C8h/C9h)

Table 83: Read DMA command (C8h/C9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - - H H H H
Command	1 1 0 0 1 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Read DMA command reads one or more sectors of data from disk media and then transfers the data from the device to the host. It transfers the sectors through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by the DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that the data transfer has terminated and that status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, 256 sectors will be transferred.

LBA Low This indicates the sector number of the first sector to be transferred. (L = 0).

In LBA mode, this register specifies that LBA address bits 0–7 are to be transferred (L = 1)

LBA High/Mid This indicates the cylinder number of the first sector to be transferred. (L = 0).

In LBA mode this register specifies LBA address bits 8–15 (Mid) and 16–23 (High) to be transferred. (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0).

In LBA mode this register specifies the LBA bits 24–27 to be transferred. (L = 1)

R This indicates the retry bit, but this bit is ignored.

Input parameters from the device

Sector Count	This indicates the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
LBA Low	This indicates the sector number of the last transferred sector. (L = 0). In LBA mode this register contains the current LBA bits 0–7. (L = 1)
LBA High/Low	This indicates the cylinder number of the last transferred sector. (L = 0). In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits16–23 (High). (L=1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.14 Read DMA EXT (25h)

Table 84: Read DMA EXT (25h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 0 1 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector

Output parameters to the device

Sector Count Current This indicates the number of sectors to be transferred low order, bits (7-0)

Sector Count Previous This indicates the number of sectors to be transferred high order, bits (15-8). If 0000h in the Sector Count register is specified, 65.536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High (HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.15 Read Log Ext (2Fh)

Table 85: Read Log Ext command (2Fh)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 1 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

Output parameters to the device

Sector CountCurrent The number of sectors to be read from the specified log low order, bits (7:0). The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.

Sector Count Previous The number of sectors to be read from the specified log high orders, bits (15:8).

LBA Low Current The log to be returned as described in Figure

LBA Mid Current The first sector of the to be read low order, bits (7:0).

LBA Mid Previous The first sector of the log to be read high order, bit (15:8)

Table 86: Log address definition

Log address	Content	Feature set	Type
00h	Log directory	N/A	Read Only
03h	Extended Comprehensive SMART error log	SMART error logging	Read Only
06h	SMART self-test log	SMART self-test	See Note
07h	Extended SMART self-test log	SMART self-test	Read Only
80h-9Fh	Host vendor specific	SMART	Read/Write

Note: If log address 06h is accessed using the Read Log Ext or Write Ext commands, command abort shall be returned.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log sector shall also be included in the Comprehensive SMART self-test log sector with the 48-bit entries.

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted.

13.15.1 General purpose log Directory

Description	Bytes	Offset
General Purpose Logging Version	2	00h
Number of sectors in the log at log address 01h (7:0)	1	02h
Number of sectors in the log at log address 01h (15:8)	1	03h
Number of sectors in the log at log address 02h (7:0)	1	04h
Number of sectors in the log at log address 02h (15:8)	1	05h
...		
Number of sectors in the log at log address 80h (7:0)	1	100h
Number of sectors in the log at log address 80h (15:8)	1	101h
...		
Number of sectors in the log at log address FFh (7:0)	1	1FEh
Number of sectors in the log at log address FFh (15:8)	1	1FFh
	512	

The value of the General Purpose Logging Version word shall be 0001h. A value of 0000h indicates that there is no General Purpose Log Directory. The Logs at log addresses 80h-9Fh are defined as 16 sectors long.

13.15.2 Extended comprehensive SMART error log

defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. Error log data structure shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or in valid addresses.

Table 87: Extended comprehensive SMAERT error log

Description	Bytes	Offset
SMART error log version	1	00h
Reserved	1	01h
Error log index (7:0)	1	02h
Error log index (15:8)	1	03h
1st error log data structure	124	04h
2nd error log data structure	124	80h
3rd error log data structure	124	FCh
4th error log data structure	124	178h
Device error count	2	1F4h
Reserved	9	1F6h
Data structure checksum	1	1FFh
	512	

13.15.3 Error Log version

The value of this version shall be 01h.

13.15.3.1 Error Log index

This indicates the error log data structure representing the most recent error. If there have been no error log entries, it is cleared to 0. Valid values for the error log index are 0 to 4.

13.15.3.2 Extended Error log data structure

An error log data structure shall be presented for each of the last four errors reported by the device. These error log data structure entries are viewed as a circular buffer. The fifth error shall create an error log structure that replaces the first error log data structure. The next error after that shall create an error log data structure that replaces the second error log structure, etc.

Unused error log data structures shall be filled with zeros.

Data format of each error log structure is shown below.

Description	Bytes	Offset
1st command data structure	18	00h
2nd command data structure	18	12h
3rd command data structure	18	24h
4th command data structure	18	36h
5th command data structure	18	48h
Error data structure	34	5Ah
	124	

Command data structure: Data format of each command data structure is shown below.

Table 88: Command data structure

Description	Bytes	Offset
Device Control register	1	00h
Features register (7:0) (see Note)	1	01h
Features register (15:8)	1	02h
Sector count register (7:0)	1	03h
Sector count register (15:8)	1	04h
Sector number register (7:0)	1	05h
Sector number register (15:8)	1	06h
Cylinder Low register (7:0)	1	07h
Cylinder Low register (15:8)	1	08h
Cylinder High register (7:0)	1	09h
Cylinder High register (15:8)	1	0Ah
Device/Head register	1	0Bh
Command register	1	0Ch
Reserved	1	0Dh
Timestamp (milliseconds from Power-on)	4	0Eh
	18	

Note bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register.

State shall contain a value indicating the state of the device when the command was issued to the device or the reset occurred as described below.

Value State

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific

Note: The value of x is vendor specific.

13.15.3.3 Device error count

This field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached the count shall remain at the maximum value when additional errors are encountered and logged.

13.15.4 Extended Self-test log sector

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined in "Self-test log data structure" shall also be included in the Extended SMART self-test log with all 48-bit entries.

Table 89: Extended Self-test log data structure

Description	Bytes	Offset
Self-test log data structure revision number	1	00h
Reserved	1	01h
Self-test descriptor index (7:0)	1	02h
Self-test descriptor index (15:8)	1	03h
Descriptor entry 1	26	04h
Descriptor entry 2	26	1Eh
...		
Descriptor entry 18	26	1D8h
Vendor specific	2	1F2h
Reserved	11	1F4h
Data structure checksum	1	1FFh
	512	

These descriptor entries are viewed as a circular buffer. The nineteenth self-test shall create a descriptor entry that replaces descriptor entry 1. The next self-test after that shall create a descriptor entry that replaces descriptor entry 2, etc. All unused self-test descriptors shall be filled with zeros.

13.15.4.1 Self-test log data structure revision number

The value of this revision number shall be 01h.

13.15.4.2 Self-test descriptor index

The indicates the most recent self-test descriptor. If there have been no self-tests, this is set to zero. Valid values for the self-test descriptor index are 0 to 18.

13.15.4.3 Extended self-test log descriptor entry

The content of the self-test descriptor entry is shown below.

Table 90: Extended self-test log descriptor entry

Description	Bytes	Offset
Self-test number	1	00h
Self-test execution status	1	01h
Power-on life timestamp in hours	2	02h
Self-test failure check point	1	04h
Failing LBA (7:0)	1	05h
Failing LBA (15:8)	1	06h
Failing LBA (23:16)	1	07h
Failing LBA (31:24)	1	08h
Failing LBA (39:32)	1	09h
Failing LBA (47:40)	1	0Ah
Vendor specific	15	0Bh
	26	

13.16 Read Long (22h/23h)

Table 91: Read Long (22h/23h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - - H H H H
Command	0 0 1 0 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media. It then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 51 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

LBA Low This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 0–7. (L = 1)

LBA High/Mid This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 24–27. (L = 1)

R This indicates the retry bit; this bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred

LBA Low	This indicates the sector number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 0–7. (L = 1)
LBA High/Low	This indicates the cylinder number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)
H	This indicates the head number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 24–27. (L = 1)

The device internally uses 51 bytes of ECC data on all data written or read from the disk. The 4-byte mode of operation is provided by means of an emulation. Use of the 51 byte ECC mode is recommended for testing the effectiveness and integrity of the ECC functions of the device.

13.17 Read Multiple (C4h)

Table 92: Read Multiple (C4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - - H H H H
Command	1 1 0 0 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read Multiple command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. The command execution is identical to the Read Sectors command with one exception: an interrupt is generated for each block—as defined by the Set Multiple command—instead of for each sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, 256 sectors will be transferred.

LBA Low This indicates the sector number of the first sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 0–7. (L = 1)

LBA High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 8–15 (Mid), 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 24–27. (L = 1)

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. This number is zero unless an unrecoverable error occurs.

LBA Low This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode, this register contains current LBA bits 0–7. (L = 1)

LBA High/Low	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 8–15 (Mid), 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 24–27. (L = 1)

13.18 Read Multiple EXT (29h)

Table 93: Read Multiple EXT (29h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 1 0 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

Output parameters to the device

Sector Count Current This indicates the number of sectors to be transferred low order, bits (7-0)

Sector Count Previous This indicates the number of sectors to be transferred high order, bits (15-8). If 0000h in the Sector Count register is specified, 65.536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High (HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.19 Read Native Max ADDRESS (F8h)

Table 94: Read Native Max ADDRESS (F8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	V V V V V V V V
LBA Mid	- - - - - - - -		LBA Mid	V V V V V V V V
LBA High	- - - - - - - -		LBA High	V V V V V V V V
Device	1 L 1 D - - - -		Device	- - - - - H H H H
Command	1 1 1 1 1 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command returns the native max LBA/CYL of the drive which is not effected by the Set Max ADDRESS command. Even if the Address Offset mode is enabled, the native max LBA/CYL is returned.

The 48-bit native max address is greater than 268,435,455, the Read Native Max Address command returns a value of 268,435,455.

Output parameters to the device

L LBA mode. This indicates the addressing mode. L = 0 specifies CHS mode and L = 1 specifies the LBA addressing mode.

D This is the device number bit. Indicates that the device number bit of the Device/Head Register should be specified. D = 0 selects the master device and D = 1 selects the slave device.

- Indicates that the bit is not used.

Input parameters from the device

LBA Low In LBA mode this register contains the native max LBA bits 0–7. (L = 1)

In CHS mode this register contains the native max LBA Low. (L = 0)

LBA High/Mid In LBA mode this register contains the native max LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)

In CHS mode this register contains the native max cylinder number. (L = 0)

H In LBA mode this register contains the native max LBA bits 24–27. (L = 1)

In CHS mode this register contains the native maximum head number. (L = 0)

V Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.

- This indicates that the bit is not used

13.20 Read Native Max ADDRESS EXT (27h)

Table 95: Read Native Max ADDRESS EXT (27h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - -		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
LBA Low	Current	- - - - - - - -		LBA Low	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
LBA Mid	Current	- - - - - - - -		LBA Mid	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
LBA High	Current	- - - - - - - -		LBA High	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 0 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command returns the native max LBA of HDD which is not effected by Set Max ADDRESS EXT command.

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the Native max areas.

LBA Low (HOB=1) LBA (31-24) of the address of the Native max areas.

LBA Mid (HOB=0) LBA (15-8) of the address of the Native max areas.

LBA Mid (HOB=1) LBA (39-32) of the address of the Native max areas.

LBA High (HOB=0) LBA (23-16) of the address of the Native max areas.

LBA High (HOB=1) LBA (47-40) of the address of the Native max areas.

13.21 Read Sectors (20h/21h)

Table 96: Read Sectors (20h/21h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - - H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read Sectors command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. If an uncorrectable error occurs the read will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, then 256sectors will be transferred.

LBA Low This is the sector number of the first sector to be transferred. (L =0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/Low This is the cylinder number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23(High).(L = 1)

H This is the head number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This is the retry bit; this bit is ignored.

Input parameters from the device

Sector Count This is the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

LBA Low This is the sector number of the last transferred sector. (L = 0)
In LBA mode this register contains the current LBA bits 0–7. (L = 1)

LBA High/Low This is the cylinder number of the last transferred sector. (L = 0)
In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High).(L = 1)

H This is the head number of the last transferred sector. (L = 0)
In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.22 Read Sector(s) EXT (24h)

Table 97: Read Sector(s) EXT Command (24h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 0 1 0 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Sector(s) Ext command reads from 1 to 65,536 sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output parameters to the device

Sector Count Current This indicates the number of sectors to be transferred low order, bits (7-0)

Sector Count Previous This indicates the number of sectors to be transferred high order, bits (15-8). If 0000h in the Sector Count register is specified, 65.536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High(HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.23 Read Verify Sectors (40h/41h)

Table 98: Read Verify Sectors (40h/41h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - - H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read Verify Sector(s) command verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) command and Read Verify Sector(s) command is that data is transferred to the host during a Read Sectors command and data is not transferred to the host during a Read Verify Sectors command.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output parameters to the device

Sector Count This is the number of continuous sectors to be verified. If zero is specified, 256 sectors will be verified.

LAB Low This is the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/Low This is the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)

H This is the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This is the retry bit; this bit is ignored.

Input parameters from the device

Sector Count This is the number of requested sectors not transferred. This number will be zero, unless an unrecoverable error occurs.

LBA Low This is the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

LBA High/Low	This is the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)
H	This is the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.24 Ready Verify Sector(s) EXT (42h)

Table 99: Read Verify Sector(s) EXT Command (42h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		1 1 1 D - - - -		Device		V - - - - - - -
Command		0 0 1 0 0 1 0 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Read Verify Sector(s) Ext verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) Ext command and the Read Verify Sector(s) Ext command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the Read Verify Sector(s) Ext will be terminated at the failing sector.

Output parameters to the device

Sector Count Current This indicates the number of sectors to be transferred low order, bits (7-0)

Sector Count Previous This indicates the number of sectors to be transferred high order, bits (15-8). If 0000h in the Sector Count register is specified, 65,536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High(HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.25 Recalibrate (1xh)

Table 100: Recalibrate (1xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	0 0 0 1 - - - -		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	V	0		0	V	0	V	-	0	-	V

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

13.26 Security Disable Password (F6h)

Table 101: Security Disable Password (F6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in the table below. The device then checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be reactivated later by setting User Password. This command should be executed in device unlock mode.

Table 102: Password Information for Security Disable Password command

Word	Description
00	Control word bit 0 : Identifier (1-Master, 0- User) bits 1-15 : Reserved
01-16	Password (32 bytes)
17- 255	Reserved

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

13.27 Security Disable Password (F6h)

Table 103: Security Disable Password (F6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 0 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in "Password Information for Security Disable Password command" on page 104. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be re-activated later by setting User Password. This command should be executed in device unlock mode.

Word	Description	
00	Control word	
	bit 0	: Identifier (1-Mater, 0-User)
	bit 1-15	: Reserved
01-16	Password	(32 bytes)
17-255	Reserved	

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

13.28 Security Erase Unit (F4h)

Table 104: Security Erase Unit (F4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Security Erase Unit command initializes all user data sectors and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. The Host MAX LBA is set by the Initialize Drive Parameter or the Set MAX ADDRESS command is ignored. The protected area by the Set MAX ADDRESS command is also initialized.

This command requests the transfer of a single sector of data from the host including information specified in the table below.

If the password does not match, the device rejects the command with an Aborted error.

Table 105: Erase Unit information

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). After completing of this command, all the user data will be initialized to zero with a write operation. At this time, the data write is not verified with a read operation to determine if the data sector is initialized correctly. At this time the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command, the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however, the master password is still stored internally within the device and may be reactivated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the Master Password and the User Password. The device only erases all user data.

The execution time of this command for each model is shown below:

HTS541010G9AT00	64 min
HTS541080G9AT00	52 min
HTS541060G9AT00	40 min
HTS541040G9AT00	26 min
HTS541030G9AT00	22 min
HTS541020G9AT00	14 min

13.29 Security Freeze Lock (F5h)

Table 106: Security Freeze Lock (F5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by a Power off.

The following commands are rejected when the device is in frozen mode. Refer to Table 53: “Command table for device lock operation” on page 82.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

13.30 Security Set Password (F1h)

Table 107: Security Set Password (F1h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Security Set Password command enables the security mode feature (device lock function) and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command and the device is not locked immediately. The device is locked after the next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally. The device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in the table below.

The data transferred controls the function of this command.

Table 108: Security Set Password information

Word	Description
00	Control Word bit 0 : Identifier (1-Master, 0-User) bit 1-7 : Reserved bit 8 : Security level (1-Maximum, 0-High) bit 9-15 : Reserved
01-16	Password (32 bytes)
17-18	Master Password Revision Code (valid if Word0bit 0 = 1)
19-255	Reserved

Identifier
Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

Security Level
A zero indicates a High level, a one indicates a Maximum level. If the host sets the High level and the password is forgotten then the Master Password can be used to unlock the device. If the host sets the Maximum level and the user password is forgotten, only a Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password
The 32 bytes are always significant in the text of the password.

Master Password Revision Code
The Revision Code field is set with Master password. If Identifier is User, the Revision Code is not set. The Revision Code field is returned in Identify Device word 92. The valid Revision Codes are 0000h to FFFDh. The Default Master Password Revision Code is FFFEh. The code FFFFh is reserved.

The setting of the Identifier and Security level bits interact as follows:

Identifier = User / Security level = High
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by either the user password or the previously set master password.

Identifier = Master / Security level = High
This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier = User / Security level = Maximum
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by only the user password. The master password previously set is still stored in the drive but may NOT be used to unlock the device.

Identifier = Master / Security level = Maximum
This combination will set a master password but will NOT enable the security mode feature (lock function).

13.31 Security Unlock (F2h)

Table 109: Security Unlock (F2h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 1 0 0 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command unlocks the password and causes the device to enter device unlock mode. If a power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in the table below.

If the Identifier bit is set to master and the drive is in high security mode, the password supplied will be compared with the stored master password. If the drive is in maximum security mode, the security unlock will be rejected.

If the Identifier bit is set to user, the drive compares the supplied password with the stored user password.

If the password compare fails, the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero, all password protected commands are rejected until there is a hard reset or a power off.

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Identifier
A zero indicates that the device regards Password as the User Password. A one indicates that the device regards Password as the Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password since this is the only reason that an abort error will be returned by the drive AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the drive, then another problem exists.

13.32 Seek (7xh)

Table 110: Seek (7xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	0 1 1 1 - - - -		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Seek command initiates a seek to the designated track and selects the designated head. The device does not need to be formatted for a seek to execute properly.

Output parameters to the device

LBA Low In LBA mode this register specifies the LBA address bits 0–7 for seek. (L = 1)

LBA High/Mid This is the cylinder number of the seek. In LBA mode this register specifies the LBA address bits 8–15 (Low) and bits 16–23 (High) for seek. (L = 1)

H This indicates the head number of the seek. In LBA mode this register specifies the LBA address bits 24–27 for seek. (L = 1)

Input parameters from the device

LBA Low In LBA mode this register contains the current LBA bits 0–7. (L = 1)

LBA High/Mid In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits16–23 (High). (L = 1)

H In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.33 Sense Condition (F0h: vendor specific)

Table 111: Sense Condition (F0h: vendor specific)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 0 0 0 0 1		Error	see below
Sector Count	- - - - - - - -		Sector Count	V V V V V V V V
LBA Low	- - - - - - - -		LBA Low	- - - - - - - N
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - D - - - -
Command	1 1 1 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		V	V	V	-	V	-	-	V

The Sense Condition command is used to sense temperature in a device. This command is executable without spinning up even if a device is started with No Spin Up option. If this command is issued at the temperature out of range which is specified for operating condition, the error might be returned with IDN bit 1.

Output parameters to the device

Feature The Feature register must be set to 01h. All other values are rejected with setting ABORT bit in status register.

Input parameters from the device

Sector Count The Sector Count register contains result value.

Value	Description
00h	Temperature is equal to or lower than –20°C
01h–FEh	Temperature is (Value/2–20)°C
FFh	Temperature is higher than 107°C

N Not recommendable condition for start up. If over stressed condition is detected, this bit will be set to one.

13.34 Set Features (EFh)

Table 112: Set Features (EFh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	see note 1		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 1 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in the table below.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

After the power on reset or hard reset the device is set to the following features as default.

Write cache	Enable
ECC bytes	4 bytes
Read look-ahead	Enable
Reverting to power on defaults	Disable
Address Offset mode	Disable

Output parameters to the device

Feature	Destination code for this command
02H	Enable write cache (See note 2)
03H	Set transfer mode based on value in sector count register
05H	Enable Advanced Power Management
06H	Enable Power-Up in Standby feature set
07H	Power-Up in Standby feature set device spin-up
09H	Enable Address Offset mode
42H	Enable Automatic Acoustic Management feature set
44H	51 bytes of ECC apply on Read Long/Write Long commands
55H	Disable read look-ahead feature
66H	Disable reverting to power on defaults
82H	Disable write cache
85H	Disable Advanced Power Management (see note 3)

86H	Disable Power-Up in Standby feature set
89H	Disable Address Offset mode
BBH	4 bytes of ECC apply on Read Long/Write Long commands
C2H	Disable Automatic Acoustic Management feature set
CCH	Enable reverting to power on defaults

Note 1. When the Feature register is 03h (= Set Transfer mode) the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

	bits (7:3)	bits (2:0)	
PIO Default Transfer Mode	00000	000	
PIO Default Transfer Mode, Disable IORDY	00000	001	
PIO Flow Control Transfer Mode X	00001	nnn	(nnn=000,001,010,011,100)
Multiword DMA mode x	00100	nnn	(nnn=000,001,010)
Ultra DMA mode x	01000	nnn	(nnn=000,001,010,011,100)

When the Feature Register is 05h (=Enable Advanced Power Management) the Sector Count Register specifies the Advanced Power Management level.

C0h-FEh	The deepest Power Saving Mode is Active Idle
80h-BFh	The deepest Power Saving Mode is Low Power Idle
01h-7Fh	The deepest Power Saving Mode is Standby
00h, FFh	Aborted

Note 2. If the number of auto reassigned sectors reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command (with Feature register = 02h) without error, the write cache function will remain disabled. For the current write cache function status, refer to the Identify Device Information (129 word) by the Identify Device command.

Hard reset or power off must not be done during the first 5 seconds after write command completion when write cache is enabled.

Note 3. When the Feature register is 85h (=Disable Advanced Power Management), the deepest Power Saving mode becomes Active Idle.

13.35 Set Max ADDRESS (F9h)

Table 113: Set Max ADDRESS (F9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	- - - - - - - B		Sector Count	- - - - - - - -
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Set Max ADDRESS command overwrites the max LBA/CYL of the drive in a range of actual device capacities. Once the device receives this command, all accesses beyond that LBA/CYL are rejected by setting the ABORT bit in the status register. Identify the device command and Identify the device DMA command returns the LBA/CYL which is set via this command as a default value.

This command implement SET MAX security extension commands as subcommands. But regardless of Feature register value, the case this command is immediately preceded by a Read Native Max ADDRESS command, it is interpreted as a Set Max ADDRESS command.

The Read Native Max ADDRESS command should be issued and completed immediately prior to issuing the Set Max ADDRESS command. If it is not, this command is interpreted as a Set Max security extension command which is designated by feature register.

If Set Max security mode is in the Locked or Frozen, the Set Max ADDRESS command is aborted. For more information, see section 11.10.2 “Set Max security extension commands” on page 84.

In CHS mode LBA High and LBA Mid specify the maximum cylinder number. The Head number of DEVICE and LBA Low are ignored. The default value (see default CHS in Identify device information) is used for that.

In LBA mode the Head number of Device, LBA High, LBA Mid and LBA Low specify the max LBA. This command sets this LBA as the max LBA of the device.

After a successful command completion, Identify Device response words (61:60) shall reflect the maximum address set with this command.

If the 48-bit Address feature set is supported, the value placed in Identify Device response words (103:100) shall be the same as the value placed in words (61:60). However, if the device contains greater than 268,435,455 sectors, the capacity addressable with 28-bit commands, and the address requested is 268,435,455, the max address shall be changed to the native maximum address, the value placed in words (61:60) shall be 268,435,455 and the value placed in words (103:100) shall be the native maximum address.

If a host protected area has been established by a Set Max Address Ext command, the device shall return command aborted

Output parameters to the device

Feature	Destination code for this command
01h	SET MAX SET PASSWORD
02h	SET MAX LOCK
03h	SET MAX UNLOCK
04h	SET MAX FREEZE LOCK
	When the Set Max ADDRESS command is executed, this register is ignored.
B	This indicates the option bit for selection whether nonvolatile or volatile. B = 0 is the volatile condition. When B = 1, MAX LBA/CYL—which is set by the Set Max ADDRESS command—is preserved by POR and HARD RESET. When B = 0, MAX LBA/CYL—which is set by Set Max ADDRESS command—will be lost by POR and HARD RESET. B = 1 is not valid when the device is in Address Offset mode and the command is aborted.
LBA Low	In LBA mode, this register contains LBA bits 0 - 7 which is to be input (L=1). In CHS mode, this register is ignored. (L=0)
LBA High/Mid	In LBA mode, this register contains LBA bits 8 - 15 (Mid), 16 - 23 (High) which is to be set. (L=1)
	In CHS mode, this register contains max cylinder number which is to be set. (L=0)
H	In LBA mode this register contains LBA bits 24–27 which are to be input. (L = 1)
	In CHS mode this register is ignored. (L = 0)
L	This indicates the LBA addressing mode. L = 0 specifies the CHS mode and L=1 specifies the LBA addressing mode.
D	This indicates the device number bit. The device number bit of the Device/Head should be specified. D = 0 selects the master device and D = 1 selects the slave device.

Input parameters from the device

LBA Low	In LBA mode this register contains the Adjusted max. LBA bits 0–7.(L = 1)
	In CHS mode this register contains the maximum LBA Low (= 63). (L = 0)
LBA High/Mid	In LBA mode this register contains the Adjusted max. LBA bits 8–15 (Mid) and bits 16-23 (High). (L = 1)
	In CHS mode this register contains the max cylinder number which is set. (L=0)
H	In LBA mode this register contains the Adjusted max. LBA bits 24–27. (L = 1)
	In CHS mode this register contains the maximum head number (= 15). (L = 0)

13.36 Set Max ADDRESS EXT (37h)

Table 114: Set Max ADDRESS EXT Command (37h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - B		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		- 1 - D - - - -		Device		V - - - - - - -
Command		0 0 1 1 0 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0		V

This command is immediately preceded by a Read Native Max Address Ext command.

This command overwrites the maximum number of Address of HDD in a range of actual device capacity. Once device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register.

When the address requested is greater than 268,435,455, words (103:100) shall be modified to reflect the requested value, but words (61:60) shall not modified. When the address requested is equal to or less than 268,435,455, words (103:100) shall be modified to reflect the requested value, and words (61:60) shall also be modified.

If this command is not supported, the maximum value to be set exceeds the capacity of the device, a host protected area has been established by a Set Max Address command, the command is not immediately preceded by a Read Native Max Address Ext command, or the device is in the Set Max Locked or Set Max Frozen state, the device shall return command aborted.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

The device returns the command aborted for a second non-volatile Set Max Address Ext command until next power on or hardware reset.

Output parameters to the device

B	Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX Address which is set by Set Max Address Ext command is preserved by POR. When B=0, MAX Address which is set by Set Max Address Ext command will be lost by POR. B=1 is not valid when the device is in Address Offset mode.
LBA Low Current	Set Max LBA (7-0)
LBA Low Previous	Set Max LBA (31-24)
LBA Mid Current	Set Max LBA (15-8)
LBA Mid Previous	Set Max LBA (39-32)
LBA High Current	Set Max LBA (23-16)
LBA High Previous	Set Max LBA (47-40)

Input parameters from the device

LBA Low (HOB=0)	Set Max LBA (7-0)
LBA Low (HOB=1)	Set Max LBA (31-24)
LBA Mid (HOB=0)	Set Max LBA (15-8)
LBA Mid (HOB=1)	Set Max LBA (39-32)
LBA High (HOB=0)	Set Max LBA (23-16)
LBA High(HOB=1)	Set Max LBA (47-40)

13.37 Set Multiple (C6h)

Table 115: Set Multiple command (C6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 0 0 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

The default block size after power up or hard reset is 0. The Read Multiple and Write Multiple commands are disabled.

If an invalid block size is specified, an Abort error will be returned to the host. The Read Multiple and Write Multiple commands will be disabled.

Output parameters to the device

Sector Count This indicates the block size to be used for the Read Multiple and the Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then the Read Multiple and the Write Multiple commands are disabled.

13.38 Sleep (E6h/99h)

Table 116: Sleep (E6h/99h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command is the only way to cause the device to enter Sleep Mode.

When this command is issued, the device confirms the completion of the cached write commands before it asserts INTRQ. Then the device is spun down, and the interface becomes inactive. The only way to recover from Sleep Mode is with a software reset or a hardware reset.

The use of hardware reset to recover from Sleep Mode may be incompatible with continued operation of the host system.

If the device is already spun down, the spin down sequence is not executed.

13.39 S.M.A.R.T. Function Set (B0h)

Table 117: S.M.A.R.T. Function Set (B0h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	0 1 0 0 1 1 1 1		LBA Mid	- - - - - - - -
LBA High	1 1 0 0 0 0 1 0		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 0 1 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The S.M.A.R.T. Function Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the device's Features Register when the S.M.A.R.T. Function Set command is issued by the host. In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	S.M.A.R.T. Read Attribute Values
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/disable Attribute Autosave
D3h	S.M.A.R.T. Save Attribute Values
D4h	S.M.A.R.T. Execute Off-line Immediate
D5h	S.M.A.R.T. Read Log Sector
D6h	S.M.A.R.T. Write Log Sector
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status
DBh	S.M.A.R.T. Enable/Disable Automatic Off-line

13.39.1 S.M.A.R.T. Function Subcommands

13.39.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated Attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

13.39.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the S.M.A.R.T. Read Attribute Thresholds subcommand from the host, the device asserts BSY, reads the Attribute Thresholds from the Attribute Threshold sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device via the Data Register.

13.39.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)

This subcommand enables and disables the attribute auto save feature of the device. The S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector at the timing of the first transition to Active idle mode and after 30 minutes after the last saving of Attribute Values. This subcommand causes the auto save feature to be disabled. The state of the Attribute Autosave feature—either enabled or disabled—will be preserved by the device across the power cycle.

A value of 00h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or a power-down.

A value of F1h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be enabled. Any other nonzero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will not change the current Autosave status. The device will respond with the error code specified in Table 129: “S.M.A.R.T. Error Codes” on page 185.

The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

13.39.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

13.39.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The LBA Low register shall be set to specify the operation to be executed.

LBA Low	Operation to be executed
0	Execute S.M.A.R.T. off-line data collection routine immediately
1	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
2	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
3	Reserved
4	Execute SMART selective self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute S.M.A.R.T. Short self-test routine immediately in captive mode
130	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode
131	Reserved
132	Execute SMART selective self-test routine immediately in captive mode

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (see Table 119: “Device Attribute Data Structure” on page 174) and ATA registers and then executes the command completion. See definitions below.

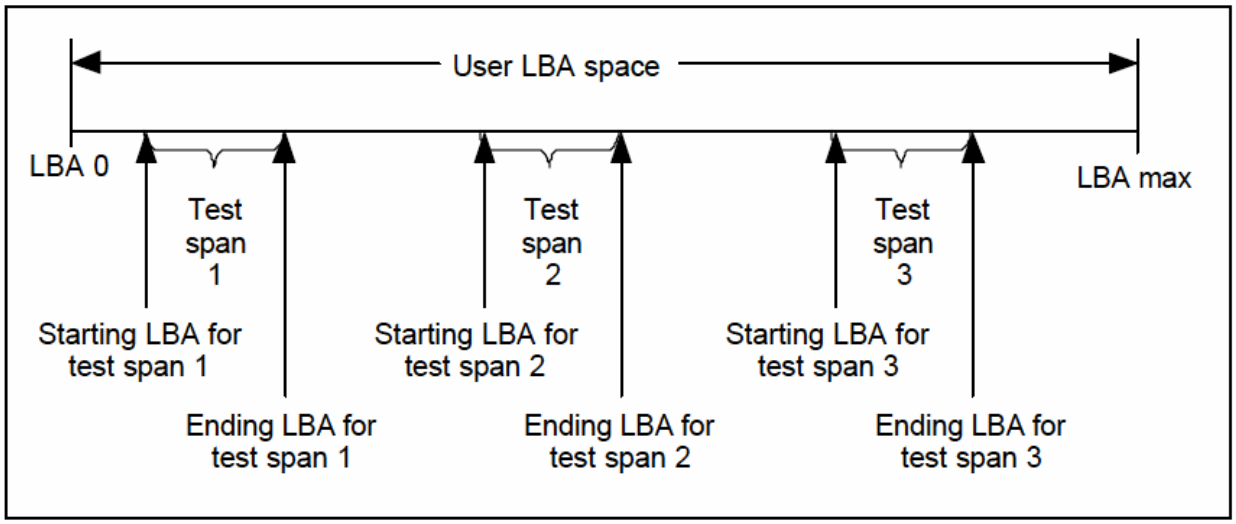
Status	Set ERR to one when the self-test has failed
Error	Set ABRT to one when the self-test has failed
LBA Low	Set to F4h when the self-test has failed
LBA High	Set to 2Ch when the self-test has failed

SMART Selective self-test routine

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This self-test routine shall include the initial tests performed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress.

The user may choose to do read scan only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Table 118 shows an example of a Selective self test definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.

Table 118: Selective self-test span example



After the scan of the selected spans described above, a user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the device shall then set the offline scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall completed as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the device is powered-down before the off-line scan is completed, the off-line scan shall resume when the device is again powered up. From power-up, the resumption of the scan shall

be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion.

During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log.

A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log (see section 13.39.6). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

13.39.1.6 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes of data are returned at a command and the Sector Count value shall be set to one. The LBA Low shall be set to specify the log sector address.

Log sector address	Content	Type
01h	S.M.A.R.T. Error Log	Read Only
03h	Extended Comprehensive	Read Only
07h	Extended self-test error log	See note
09h	Selective self-test log	Read/write
80h-9Fh	Host vendor specific	Read/Write

13.39.1.7 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. The 512 bytes of data are transferred at a command and the LBA Low value shall be set to one. The LBA Low shall be set to specify the log sector address (See Table 117: “S.M.A.R.T. Function Set (B0h)” on page 168). If a Read Only log sector is specified, the device returns ABRT error.

13.39.1.8 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

13.39.1.9 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute auto save feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.

Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled, and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand— returning the error code as specified in Table 129: “S.M.A.R.T. Error Codes” on page 185.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command.

13.39.1.10 S.M.A.R.T. Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the S.M.A.R.T. Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the LBA Mid register, C2h into the LBA High register, clears BSY, and asserts INTRQ.

If the device detects a Threshold Exceeded Condition for prefailure attributes, the device loads F4h into the LBA Mid register, 2Ch into the LBA High register, clears BSY, and asserts INTRQ. Advisory attributes never result in a negative reliability condition.

13.39.1.11 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities.

The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count	Feature Description
00h	Disable Automatic Off-line
01h	Disable Off-line Read Scanning
F8h	Enable Automatic Off-line
F9h	Enable Off-line Read Scanning

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence.

A value of one written by the host into the device's Sector Count register before issuing this subcommand shall cause the off-line read scanning feature to be disabled. The Device does not perform the off-line read scanning at the off-line data collection activities which is initiated by the S.M.A.R.T. Execute Off-line Immediate (Subcommand D4h) or automatically if the off-line read scanning feature is disabled.

A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled.

A value of F9 written by the host into the device's Sector Count register before issuing this subcommand shall cause the off-line read scanning feature to be enabled. The Device perform the off-line read scanning at the off-line data collection activities which is initiated by the S.M.A.R.T. Execute Off-line Immediate (Subcommand D4h) even if the automatic off-line feature is disabled.

Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in Table 129: “S.M.A.R.T. Error Codes” on page 185.

13.39.2 Device Attribute Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specification for byte ordering, namely, that the least significant byte occupies the lowest numbered byte address location in the field.

Table 119: Device Attribute Data Structure

Description	Byte	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0010h
1st Device Attribute	12	02h	(*1)	(*2)
...				
30th Device Attribute	12	15Eh	(*1)	(*2)
Off-line data collection status	1	16Ah	(*1)	(*2)
Self-test execution status	1	16Bh	(*1)	(*2)
Total time in seconds to complete off-line data collection activity	2	16Ch	(*1)	(*2)
Current segment pointer	1	16Eh	(*1)	(*2)
Off-line data collection capability	1	16Fh	(*1)	1Bh
S.M.A.R.T. capability	2	170h	(*1)	0003h
S.M.A.R.T. device error logging capability	1	172h	(*1)	01h
Self-test failure check point	1	173h	(*1)	(*2)
Short self-test completion time in minutes	1	174h	(*1)	(*2)
Extended self-test completion time in minutes	1	175h	(*1)	(*2)
Reserved	12	176h		(*3)
Vendor specific	125	182h		(*3)
Data structure checksum	1	1FFh	(*1)	(*2)
	512			

(*1) – See following definitions
(*2) – This value varies due to actual operating condition.
(*3) – Filled with 00h.

13.39.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

13.39.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Byte	Offset	Value
Attribute ID Number (01h to FFh)	1	00h	binary
Status Flags	2	01h	bit flags
Bit 0 Pre-Failure/Advisory			
Bit 1 On-line Collection			
Bit 2-5 Reserved (may be either 0 or 1)			
Bit 6-15 Reserved (all 0)			
Attribute Value (valid values from 01h to FEh)	1	03h	binary
00h invalid for attribute value -not to be used			
01h minimum value			
64h initial value for all attributes prior to any data collection			
FDh maximum value			
FEh value is not valid			
FFh invalid for attribute value-not to be used			
Reserved (may not be 0)	1	04h	binary
Reserved (may not be 0)	6	05h	binary
Reserved (00h)	1	0Bh	binary
Total Bytes	12		

Attribute ID Numbers: Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers. The names marked with (*) indicate that the corresponding Attribute Values can be either collected on-line or off-line.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate (*)
2	Throughput Performance (*)
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time Performance (*)
9	Power-On Hours Count
10	Spin Retry Count
12	Device Power Cycle Count
191	G Sense Error Rate
192	Power Off Retract Count
193	Load/Unload Cycle Count
194	Device Temperature
196	Reallocation Event Count
197	Current Pending Sector Count
198	Off-Line Scan Uncorrectable Sector Count
199	Ultra DMA CRC Error Count

Table 120: Status Flag definitions

Bit	Flag Name	Definition
0	Pre-Failure/ Advisory bit	If bit = 0, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates an Advisory condition where the usage or age of the device has exceeded its intended design life period. If bit = 1, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates a Pre-Failure condition where imminent loss of data is being predicted.
1	On-Line Collective bit	If bit = 0, the Attribute Value is updated only during Off-Line testing. If bit = 1, the Attribute Value is updated during On-Line testing or during both On-Line and Off-Line testing.
2-5	Reserved bits	May either be 0 or 1
6-15	Reserved bits	Always 0

Normalized values: The device will perform conversion of the raw Attribute Values to transform them into normalized values which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value. In normalizing the raw data, the device will perform any necessary statistical validity checks to ensure that an instantaneous raw value is not improperly reflected in the normalized Attribute Value (i.e., one read error in the first 10 reads being interpreted as exceeding the read error rate threshold when the subsequent 1 billion reads all execute without error). The end points for the normalized values for all Attributes will be 1 (01h) at the low end and 100 (64h) at the high end for the device. For Performance and Error Rate Attributes, values greater than 100 are also possible. The maximum value possible is 253 (FDh).

13.39.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7 Automatic Off-line Data Collection Status

0 Automatic Off-line Data Collection is disabled.

1 Automatic Off-line Data Collection is enabled.

Bits 0–6 represent a hexadecimal status value reported by the device.

Value **Definition**

0 Off-line data collection never started.

2 All segments completed without errors. In this case the current segment pointer is equal to the total segments required.

4 Off-line data collection is suspended by the interrupting command.

5 Off-line data collecting is aborted by the interrupting command.

6 Off-line data collection is aborted with a fatal error.

13.39.2.4 Self-test execution status

Bit	Definition
0-3	Percent Self-test remaining. An approximation of the percent of the self-test routine remaining until completion given in ten percent increments. Valid values are 0 through 9.
4-7	Current Self-test execution status.
	0 The self-test routine completed without error or has never been run.
	1 The self-test routine was aborted by the host.
	2 The self-test routine was interrupted by the host with a hard or soft reset.
	3 The device was unable to complete the self-test routine due to a fatal error or unknown test error.
	4 The self-test routine was completed with an unknown element failure.
	5 The self-test routine was completed with an electrical element failure.
	6 The self-test routine was completed with a servo element failure.
	7 The self-test routine was completed with a read element failure.
	15 The self-test routine is in progress.

13.39.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

13.39.2.6 Current segment pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1, 01h is always returned in this field.

13.39.2.7 Off-line data collection capability

Bit	Definition
0	Execute Off-line Immediate implemented bit
	0 S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented
	1 S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/disable Automatic Off-line implemented bit
	0 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented
	1 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented
2	Abort/restart off-line by host bit
	0 The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
	1 The device will abort off-line data collection activity upon receipt of a new command

3 Off-line Read Scanning implemented bit

- **0** The device does not support Off-line Read Scanning
- **1** The device supports Off-line Read Scanning

4 Self-test implemented bit

- **0** Self-test routing is not implemented
- **1** Self-test routine is implemented

5-7 Reserved (0)

13.39.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute auto save capability. If bit = 1, the device supports the S.M.A.R.T. ENABLE/ DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

13.39.2.9 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit = 1, the device supports the Error Logging

13.39.2.10 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

13.39.2.11 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

13.39.2.12 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

13.39.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specification for byte ordering, that is, that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Table 121: Device Attribute Thresholds Data Structure

Description	Byte	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0010h
1st Device Attribute	12	02h	(*1)	(*2)
...	..			
...	..			
30th Device Attribute	12	15Eh	(*1)	(*2)
Reserved	18	16Ah		(*3)
Vendor specific	131	17Ch		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See the following definitions
(*2) – Value varies by actual operating condition
(*3) – Filled with 00h

13.39.4 S.M.A.R.T Log Directory

Table 121 defines the 512 bytes that make up the S.M.A.R.T Log Directory. The S.M.A.R.T Log Directory is on S.M.A.R.T Log Address zero and is defined as one sector long.

Table 122: S.M.A.R.T. Log Director

Description	Bytes	Offset
S.M.A.R.T. Logging Version	2	01h
Number of sectors in the log at log address 1	1	02h
Reserved	1	03H
Number of sectors in the log at log address 2	1	04H
Reserved	1	05h
...	...	...
Number of sectors in the log at log address 255	1	1FEh
	512	

13.39.4.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

13.39.4.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Table 123: Individual Threshold Data Structure

Description	Byte	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Attribute Threshold (for comparison with Attribute Values from 00h to FFh)	1	01h	binary
00h - "always passing" threshold value to be used for code test purposes			
01h - minimum value for normal operation			
FDh - maximum value for normal operation			
FEh - invalid for threshold value			
FFh - "always failing" threshold value to be used for code test purposes			
Reserved (00h)	10	02h	binary
Total Bytes	12		

13.39.4.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

13.39.4.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use the "S.M.A.R.T. Write Attribute Threshold" subcommand to override these preset values in the Threshold sectors.

13.39.4.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of simple 8-but addition of the first 511 bytes in the data structure.

13.39.5 S.M.A.R.T. error log sector

The following defines the 512 bytes that make up the S.M.A.R.T. error log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specifications for byte ordering.

Description	Byte	Offset
S.M.A.R.T. error log version	1	00h
Error log pointer	1	01h
1st error log data structure	90	02h
2nd error log data structure	90	5Ch
3rd error log data structure	90	B6h
4th error log data structure	90	110h
5th error log data structure	90	16Ah
Device error count	2	1C4h
Reserved	57	1C6h
Data structure checksum	1	1FFh
	512	

13.39.5.1 S.M.A.R.T. error log version

This value is set to 01h.

13.39.5.2 Error log pointer

This points to the most recent error log data structure. Only values 1 through 5 are valid.

13.39.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

13.39.5.4 Error log data structure

The data format of each error log structure is shown below.

Table 124: Command data structure.

Description	Byte	Offset
1st command data structure	12	00h
2nd command data structure	12	0Ch
3rd command data structure	12	18h
4th command data structure	12	24h
5th command data structure	12	30h
Error data structure	30	3Ch
	90	

Table 125: Command data structure

Description	Byte	Offset
Device Control register	1	00h
Features register	1	01h
Sector count register	1	02h
LBA Low register	1	03h
LBA Mid register	1	04h
LBA High register	1	05h
Device register	1	06h
Command register	1	07h
Time stamp (milliseconds from Power On)	4	08h
	12	

Table 126: Error data structure

Description	Byte	Offset
Reserved	1	00h
Error register	1	01h
Sector count register	1	02h
LBA Low register	1	03h
LBA Mid register	1	04h
LBA High register	1	05h
Device register	1	06h
Status register	1	07h
Extended error data (vendor specific)	19	08h
State	1	1Bh
Life time stamp (hours)	2	1Ch
	30	

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown

x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	S.M.A.R.T. Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific
	Note: The value of x is vendor specific

13.39.6 Self-test log data structure

The following defines the 512 bytes that make up the Self-test log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-6 specifications for byte ordering.

Table 127: Self-test log data structure

Description	Byte	Offset
Data structure revision	2	00h
Self-test number	1	n*18h+02h
Self-test execution status	1	n*18h+03h
Life time power on hours	2	n*18h+04h
Self-test failure check point	1	n*18h+06h
LBA of first failure	4	n*18h+07h
Vendor specific	15	n*18h+08h
...		
Vendor specific	2	1FAh
Self-test log pointer	1	1FCh
Reserved	2	1FDh
Data structure checksum	1	1FFh
	512	

Note: N is 0 through 20

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors.

After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor.

The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

13.39.7 Selective self-test log data structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the specifications for byte ordering.

Table 128: Selective self-test log

Description	Bytes	Offset	Read/Write
Data structure revision	2	00h	R/W
Starting LBA for test span 1	8	02h	R/W
Ending LBA for test span 1	8	0Ah	R/W
Starting LBA for test span 2	8	12A	R/W
Ending LBA for test span 2	8	1Ah	R/W
Starting LBA for test span 3	8	22h	R/W
Ending LBA for test span 3	8	2Ah	R/W
Starting LBA for test span 4	8	32h	R/W
Ending LBA for test span 4	8	3Ah	R/W
Starting LBA for test span 5	8	42h	R/W
Ending LBA for test span 5	8	4Ah	R/W
Reserved	256	52h	Reserved
Vendor specific	154	152h	Vendor specific
Current LBA under test	8	1ECh	Read
Current span under test	2	1F4h	Read
Feature flags	2	1F6	R/W
Vendor specific	4	1F8h	Vendor specific
Selective self test pending time	2	1FCh	R/W
Reserved	1	1FEh	Reserved
Data structure checksum	1	1FFh	R/W
	51		

13.39.8 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Table 129: S.M.A.R.T. Error Codes

Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the LBA High and LBA Mid registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. Disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h

13.40 Standby (E2h/96h)

Table 130: Standby (E2h/96h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 0 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Standby command causes the device to enter the Standby Mode immediately and to set the auto power down time-out parameter (standby timer).

When this command is issued, the device confirms the completion of the cached write commands before it asserts the INTRQ. Following the INTRQ the interface remains active and the device is spun down. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, however there will be a delay while waiting for the spindle to reach operating speed.

The timer starts counting down when the device returns to Idle mode.

Output parameters to the device

Sector Count The Time-out Parameter. If it is zero, the time-out interval (Standby Timer) is disabled. If it is other than zero the time-out interval is set for (Time-out Parameter × 5) seconds.

When the automatic power down sequence is enabled, the device will enter the Standby mode automatically if the time-out interval expires with no device access from the host. The time-out interval will be reinitialized if there is a device access before the time-out interval expires.

13.41 Standby Immediate (E0h/94h)

Table 131: Standby Immediate (E0h/94h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Standby Immediate command causes the device to enter the Standby mode immediately.

When this command is issued, the device confirms the completion of the cached write commands before it asserts the INTRQ. Following the INTRQ the interface remains active and the device is spun down. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, however there will be a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down time-out parameter.

13.42 Write Buffer (E8h)

Table 132: Write Buffer (E8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
LBA Low	- - - - - - - -		LBA Low	- - - - - - - -
LBA Mid	- - - - - - - -		LBA Mid	- - - - - - - -
LBA High	- - - - - - - -		LBA High	- - - - - - - -
Device	1 - 1 D - - - -		Device	- - - - - - - -
Command	1 1 1 0 1 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

13.43 Write DMA (CAh/CBh)

Table 133: Write DMA (CAh/CBh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	1 1 0 0 1 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write DMA command transfers one or more sectors of data from the host to the device and then the data is written to the disk media.

The sectors of data are transferred through the Data Register16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

LBA Low This indicates the sector number of the first sector to be transferred. (L = 0)In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/Mid This indicates number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Mid) and bits 16–23 (High). (L= 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit, but this bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero unless an unrecoverable error occurs.

LBA Low	This indicates the sector number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 0–7. (L = 1)
LBA High/Mid	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.44 Write DMA EXT (35h)

Table 134: Write DMA (35h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		- 1 - D - - - -		Device		V - - - - - - -
Command		0 0 1 1 0 1 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write DMA Ext command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7-0).

Sector Count Previous The number of continuous sectors to be transferred high order bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High(HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.45 Write Long (32h/33h)

Table 135: Write Long (32h/33h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	0 0 1 1 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are either 4 or 51 according to setting of the Set Feature option. The default number after power on is 4 bytes.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

LBA Low This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/Mid This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Mid) and bits 16–23 (High) (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R The retry bit, but this bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred.

LBA Low This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

LBA High/Mid	This indicates the cylinder number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 24–27. (L = 1)

The drive internally uses 51 bytes of ECC on all data read or writes. The 4-byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 51 byte ECC mode is used for all tests to confirm the operation of the ECC hardware of the drive. Unexpected results may occur if such testing is performed using 4-byte mode.

13.46 Write Multiple (C5h)

Table 136: Write Multiple (C5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	1 1 0 0 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Multiple command transfers one or more sectors from the host to the device. The data is then written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block as defined by the Set Multiple command instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If the Sector Count of zero is specified, 256 sectors will be transferred.

LBA Low This indicates the sector number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/MId This indicates the cylinder number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Mid) and bits 16–23(High).(L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero, unless an unrecoverable error occurs.

LBA Low This indicates the sector number of the last transferred sector. (L = 0)
In LBA mode this register contains current the LBA bits 0–7. (L = 1)

LBA High/Mid This indicates the cylinder number of the last transferred sector. (L = 0)
In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)

H This indicates the head number of the last transferred sector. (L = 0)
In LBA mode this register contains current the LBA bits 24–27. (L = 1)

13.47 Write Multiple EXT (39h)

Write Multiple EXT (39h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		- 1 - D - - - -		Device		V - - - - - - -
Command		0 0 1 1 1 0 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write Multiple Ext command transfers one or more sectors from the host to the device, then the data is written to the disk media.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7-0).

Sector Count Previous The number of continuous sectors to be transferred high order bits (15-8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High(HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.48 Write Sectors (30h/31h)

Table 137: Write Sectors Command (30h/31h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
LBA Low	V V V V V V V V		LBA Low	V V V V V V V V
LBA Mid	V V V V V V V V		LBA Mid	V V V V V V V V
LBA High	V V V V V V V V		LBA High	V V V V V V V V
Device	1 L 1 D H H H H		Device	- - - - H H H H
Command	0 0 1 1 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Sectors command transfers one or more sectors from the host to the device. The data is then written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector, when the auto reassign function is disable.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If the Sector Count of zero is specified, 256 sectors will be transferred.

LBA Low This indicates the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

LBA High/Mid This indicates the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Mid) and bits 16–23 (High) (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit; this bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero unless an unrecoverable error occurs.

LBA Low This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

LBA High/Mid	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Mid) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

13.49 Write Sectors(s) EXT (34h)

Table 138: Write Sector(s) EXT Command (34h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
LBA Low	Current	V V V V V V V V		LBA Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA Mid	Current	V V V V V V V V		LBA Mid	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
LBA High	Current	V V V V V V V V		LBA High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device		- 1 - D - - - -		Device		V - - - - - - -
Command		0 0 1 1 0 1 0 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write Sector(s) Ext command transfers one or more sectors from the host to the device, then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7-0).

Sector Count Previous The number of continuous sectors to be transferred high order bits (15-8). If zero is specified in the Sector Count register, then 65,536 sectors will be transferred.

LBA Low Current LBA (7-0)

LBA Low Previous LBA (31-24)

LBA Mid Current LBA (15-8)

LBA Mid Previous LBA (39-32)

LBA High Current LBA (23-16)

LBA High Previous LBA (47-40)

Input parameters from the device

LBA Low (HOB=0) LBA (7-0) of the address of the first unrecoverable error

LBA Low (HOB=1) LBA (31-24) of the address of the first unrecoverable error

LBA Mid (HOB=0) LBA (15-8) of the address of the first unrecoverable error

LBA Mid (HOB=1) LBA (39-32) of the address of the first unrecoverable error

LBA High (HOB=0) LBA (23-16) of the address of the first unrecoverable error

LBA High(HOB=1) LBA (47-40) of the address of the first unrecoverable error

13.50 Write Verify (3Ch: vendor specific)

In the implementation of the drive the Write Verify command is exactly the same as the Write Sectors command (30h). Read verification is not performed after the write operation. Refer to 13.48, “Write Sectors (30h/31h)” on page 198.

14.0 Timings

The timing of BSY and DRQ in Status Register are shown in the table below.

Table 139: Time-out values

	INTERVAL	START	STOP	TIME-OUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=0 After RST=1	Status Register BSY=0 and RDY=1	31 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT To Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1 Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 μs
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 μs
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec *(Note 1)*
Non-Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec *(Note 2)*
DMA Data Transfer Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns

The abbreviations "ns", "μs", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

We recommend that the host system execute Soft reset and then retry to issue the command if the host system time-out would occur for the device.

Note 1. For SECURITY ERASE UNIT command, the execution time is referred to 13.27, “Security Erase Unit (F4h)” on page 144.

Note 2. For FORMAT UNIT command, the execution time is referred to 13.7, “Format Unit (F7h: vendor specific)” on page 109.

.

15.0 Appendix

15.1 Commands Support Coverage

The table below compares the command support coverage of the Travelstar 5K100 with the ATA-6 defined command set. The third column indicates the capability of the Travelstar 5K100 for those commands.

Table 140: Command coverage (1 of 2)

Code	Command Name	Implementation for Travelstar 5K100	ATA-6 Category Type
00h	NOP	No	Optional
03h	CFA REQUEST EXTENDED ERROR CODE	No	Optional (Note 7)
08h	DEVICE RESET	No	Optional (Note 7)
1xh	RECALIBRATE	Yes	Obsoleted
20h	READ SECTOR(S)	Yes	Mandatory
21h	READ SECTOR(S)	Yes	Obsoleted
24h	READ SECTOR(S) EXT	Yes	Optional
22h	READ LONG	Yes	Obsoleted
23h	READ LONG	Yes	Obsoleted
30h	WRITE SECTOR(S)	Yes	Mandatory
31h	WRITE SECTOR(S)	Yes	Obsoleted
32h	WRITE LONG	Yes	Obsoleted
33h	WRITE LONG	Yes	Obsoleted
38h	CFA TRANSLATE SECTORS W/O ERASE	No	Optional (Note 7)
3Ch	WRITE VERIFY (2)	Vendor specific	Obsoleted
40h	READ VERIFY SECTOR(S)	Yes	Mandatory
41h	READ VERIFY SECTOR(S)	Yes	Obsoleted
50h	FORMAT TRACK	Yes	Obsoleted
7xh	SEEK	Yes	Mandatory
87h	CFA TRANSLATE SECTORS	No	Optional
90h	EXECUTE DEVICE DIAGNOSTIC	Yes	Mandatory
91h	INITIALIZE DEVICE PARAMETERS	Yes	Mandatory
92h	DOWNLOAD MICROCODE	Reserved	Optional
94h-99h	Reserved	Reserved	Reserved
A0h	PACKET	No	Not to be used
A1h	IDENTIFY PACKET DEVICE	No	Not to be used
A2H	SERVICE	No	Not to be used
B0h	S.M.A.R.T. FUNCTION SET	Yes	Optional (Note 5)
C0h	CFA ERASE SECTORS	No	Optional
C4h	READ MULTIPLE	Yes	Mandatory
C5h	WRITE MULTIPLE	Yes	Mandatory
C6h	SET MULTIPLE MODE	Yes	Mandatory
C7h	READ DMA QUEUED	No	Optional

Table 141: Command coverage (2 of 2)

Code	Command Name	Implementation for Travelstar 5K100	ATA-6 Category Type
C8h	READ DMA	Yes	Mandatory
C9h	READ DMA	Yes	Obsoleted
CAh	WRITE DMA	Yes	Mandatory
CBh	WRITE DMA	Yes	Obsoleted
CCh	WRITE DMA QUEUED	No	Optional
CDh	CFA WRITE MULTIPLE W/O ERASE	No	Optional (Note 7)
DAh	GET MEDIA STATUS	No	Optional (Note 7)
DEh	MEDIA LOCK	No	Optional (Note 7)
DFh	MEDIA UNLOCK	No	Optional (Note 7)
E0h	STANDBY IMMEDIATE	Yes	Mandatory
E1h	IDLE IMMEDIATE	Yes	Mandatory
E2h	STANDBY	Yes	Mandatory
E3h	IDLE	Yes	Mandatory
E4h	READ BUFFER	Yes	Optional
E5h	CHECK POWER MODE	Yes	Mandatory
E6h	SLEEP	Yes	Mandatory
E7h	FLUSH CACHE	Yes	Mandatory
E8h	WRITE BUFFER	Yes	Optional
ECh	IDENTIFY DEVICE	Yes	Mandatory
EDh	MEDIA EJECT	No	Optional (Note 7)
EEh	IDENTIFY DEVICE DMA	No	Obsoleted
EFh	SET FEATURES	Yes	Mandatory
F0h	SENSE CONDITION	Vendor specific	Vendor specific
F1h	SECURITY SET PASSWORD	Yes	Optional (Note 6)
F2h	SECURITY UNLOCK	Yes	Optional (Note 6)
F3h	SECURITY ERASE PREPARE	Yes	Optional (Note 6)
F4h	SECURITY ERASE UNIT	Yes	Optional (Note 6)
F5h	SECURITY FREEZE LOCK	Yes	Optional (Note 6)
F6h	SECURITY DISABLE PASSWORD	Yes	Optional (Note 6)
F7h	FORMAT UNIT	Vendor specific	Vendor specific
F8h	READ NATIVE MAX ADDRESS	Yes	Optional
F9h	SET MAX ADDRESS	Yes	Optional
FB-FFh	Vendor specific	Reserved	Vendor specific
	Reserved: all remaining codes	Reserved	Reserved

Note 1. These commands have two command codes and appear in this table twice, once for each command code.

Note 2. The WRITE VERIFY command implemented vendor specific. The operation is the same as WRITE SECTORS and verification is not performed.

Note 3. Protected Area Feature Set

Note 4. Power Management Feature Set

Note 5. S.M.A.R.T. Function Set

Note 6. Security Mode Feature Set

Note 7. Removable

15.2 SET FEATURES Commands Support Coverage

The following table provides a list of Feature Registers, Feature Names, and implementation for the Travelstar 5K100. The third column indicates whether or not the Travelstar 5K100 has the capability of executing the command in comparison to the ATA-6 defined command set. For detailed operation, refer to section 13.33, “Set Features (EFh)”, on page 152.

Table 142: SET FEATURES command coverage

Features Register	Features Name	Implementation for Travelstar 5K100
02h	Enable write cache	Yes
03h	Set transfer mode	Yes
05h	Enable Advanced Power Management	Yes
06h	Enable Power-Up in Standby feature set	Yes
07h	Power-Up in Standby device spin-up	Yes
09h	Enable Address Offset mode	Yes
31h	Disable Media Status Notification	No
42h	Enable Automatic Acoustic Management	Yes
44h	Set vendor specific bytes ECC	Yes
55h	Disable read look-ahead feature	Yes
5Dh	Enable release interrupt	No
5Eh	Enable SERVICE interrupt	No
66h	Disable reverting to power on defaults	Yes
82h	Disable write cache	Yes
85h	Disable Advanced Power Management	Yes
86h	Disable Power-Up in Standby	Yes
89h	Disable Address Offset mode	Yes
95h	Enable Media Status Notification	No
AAh	Enable read look-ahead feature	Yes
BBh	Set 4 bytes ECC	Yes
C2h	Disable Automatic Acoustic Management	Yes
CCh	Enable reverting to power on defaults	Yes
DDh	Disable release interrupt	No
DEh	Disable SERVICE interrupt	No
others	Reserved	Reserved

15.3 Changes from the Travelstar 4K40

The changes between the Travelstar 5K100 and the Travelstar 4K40 are listed below:

- Identify device information data

Index

Hitachi Global Storage Technologies
5600 Cottle Road
San Jose, CA 95193
Produced in the United States

7/06

11 July 2006