DETAILED DESCRIPTION

SPEECH/SOUND QUALITY

The ISD2500 series includes devices offered at 4.0, 5.3, 6.4, and 8.0 KHz sampling frequencies, allowing the user a choice of speech quality options. Increasing the duration within a product series decreases the sampling frequency and bandwidth, which affects sound quality. Please refer to the ISD2532/40/48/64 Summary table on page *ii* to compare filter pass band and product durations.

The speech samples are stored directly into on-chip nonvolatile memory without the digitization and compression associated with other solutions. Direct analog storage provides a very true, natural sounding reproduction of voice, music, tones, and sound effects not available with most solid-state digital solutions.

DURATION

To meet end system requirements, the ISD2532/40/48/64 products offer single-chip solutions at 32, 40, 48, and 64 seconds. Parts may also be cascaded together for longer durations. For longer duration ISD2500 products see data sheet "ISD2560/75/90/120 Products."

EEPROM STORAGE

One of the benefits of ISD's ChipCorder technology is the use of on-chip nonvolatile memory, providing zero-power message storage. The message is retained for up to 100 years typically without power. In addition, the device can be re-recorded typically over 100,000 times.

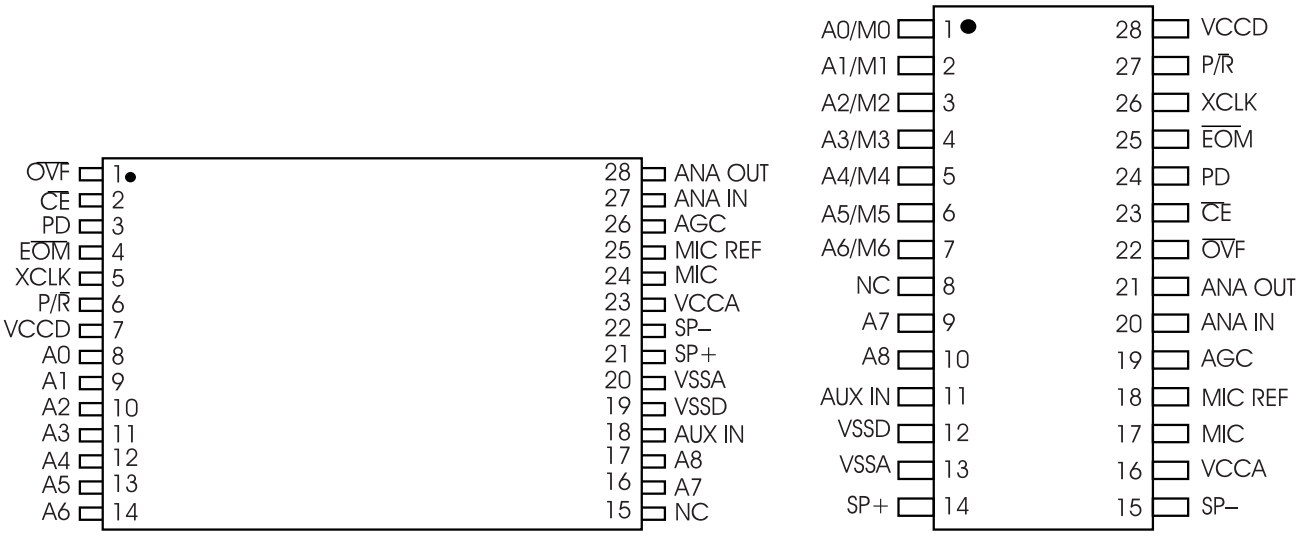
MICROCONTROLLER INTERFACE

In addition to its simplicity and ease of use, the ISD2500 series includes all the interfaces necessary for microcontroller-driven applications. The address and control lines can be interfaced to a microcontroller and manipulated to perform a variety of tasks, including message assembly, message concatenation, predefined fixed message segmentation, and message management.

PROGRAMMING

The ISD2500 series is also ideal for playback-only applications, where single or multiple messages are referenced through buttons, switches, or a microcontroller. Once the desired message configuration is created, duplicates can easily be generated via an ISD programmer.

Figure 1: ISD2532/40/48/64 Device Pinouts



PIN DESCRIPTIONS

VOLTAGE INPUTS (V_{CCA}, V_{CCD})

To minimize noise, the analog and digital circuits in the ISD2500 series devices use separate power busses. These voltage busses are brought out to separate pins and should be tied together as close to the supply as possible. In addition, these supplies should be decoupled as close to the package as possible.

GROUND INPUTS (V_{SSA}, V_{SSD})

The ISD2500 series of devices utilizes separate analog and digital ground busses. These pins should be connected separately through a low-impedance path to power supply ground.

POWER DOWN INPUT (PD)

When not recording or playing back, the PD pin should be pulled HIGH to place the part in a very low power mode (see I_{SB} specification). When overflow ($\overline{OVF}$) pulses LOW for an overflow condition, PD should be brought HIGH to reset the address pointer back to the beginning of the record/playback space. The PD pin has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

CHIP ENABLE INPUT ($\overline{CE}$)

The $\overline{CE}$ pin is taken LOW to enable all playback and record operations. The address inputs and playback/record input (P/$\overline{R}$) are latched by the falling edge of $\overline{CE}$. $\overline{CE}$ has additional functionality in the M6 (Push-Button) Operational Mode described later in the Operational Mode section.

PLAYBACK/RECORD INPUT (P/$\overline{R}$)

The P/$\overline{R}$ input is latched by the falling edge of the $\overline{CE}$ pin. A HIGH level selects a playback cycle while a LOW level selects a record cycle. For a record cycle, the address inputs provide the starting address and recording continues until PD or $\overline{CE}$ is pulled HIGH or an overflow is detected (i.e. the chip is full). When a record cycle is terminated by pulling PD or $\overline{CE}$ HIGH, an End-Of-Message ($\overline{EOM}$) marker is stored at the current address in memory. For a playback cycle, the address inputs provide the starting address and the device will play until an $\overline{EOM}$ marker is encountered. The device can continue past an $\overline{EOM}$ marker in an Operational Mode, or if $\overline{CE}$ is held LOW in address mode. (See page 5 for more Operational Modes).

END-OF-MESSAGE / RUN OUTPUT ($\overline{EOM}$)

A nonvolatile marker is automatically inserted at the end of each recorded message. It remains there until the message is recorded over. The $\overline{EOM}$ output pulses LOW for a period of T_{EOM} at the end of each message.

In addition, the ISD2500 series has an internal V_{CC} detect circuit to maintain message integrity should V_{CC} fall below 3.5 V. In this case, $\overline{EOM}$ goes LOW and the device is fixed in Playback-only mode.

When the device is configured in Operational Mode M6 (Push-Button Mode), this pin provides an active-HIGH RUN signal, indicating the device is currently recording or playing. This signal can conveniently drive an LED for a visual indicator of a record or playback operation in process.

OVERFLOW OUTPUT ($\overline{OVF}$)

This signal pulses LOW at the end of memory space, indicating the device has been filled and the message has overflowed. The $\overline{OVF}$ output then follows the $\overline{CE}$ input until a PD pulse has reset the device. This pin can be used to cascade several ISD2500 devices together to increase record/playback durations.

MICROPHONE INPUT (MIC)

The microphone input transfers its signal to the on-chip preamplifier. An on-chip Automatic Gain Control (AGC) circuit controls the gain of this preamplifier from –15 to 24 dB. An external microphone should be AC coupled to this pin via a series capacitor. The capacitor value, together with the internal 10 KΩ resistance on this pin, determines the low-frequency cutoff for the ISD2500 series passband. See ISD's Application Information for additional information on low-frequency cutoff calculation.

MICROPHONE REFERENCE INPUT (MIC REF)

The MIC REF input is the inverting input to the microphone preamplifier. This provides a noise-canceling or common-mode rejection input to the device when connected to a differential microphone.

AUTOMATIC GAIN CONTROL INPUT (AGC)

The AGC dynamically adjusts the gain of the preamplifier to compensate for the wide range of microphone input levels. The AGC allows the full range of whispers to loud sounds to be recorded with minimal distortion. The "attack" time is determined by the time constant of a 5 KΩ internal resistance and an external capacitor (C2 on the schematic on page 18) connected from the AGC pin to V_{SSA} analog ground. The "release" time is determined by the time constant of an external resistor (R2) and an external capacitor (C2) connected in parallel between the AGC Pin and V_{SSA} analog ground. Nominal values of 470 KΩ and 4.7 μF give satisfactory results in most cases.

ANALOG OUTPUT (ANA OUT)

This pin provides the preamplifier output to the user. The voltage gain of the preamplifier is determined by the voltage level at the AGC pin.

ANALOG INPUT (ANA IN)

The analog input pin transfers its signal to the chip for recording. For microphone inputs, the ANA OUT pin should be connected via an external capacitor to the ANA IN pin. This capacitor value, together with the 3.0 KΩ input impedance of ANA IN, is selected to give additional cutoff at the low-frequency end of the voice passband. If the desired input is derived from a source other than a microphone, the signal can be fed, capacitively coupled, into the ANA IN pin directly.

EXTERNAL CLOCK INPUT (XCLK)

The external clock input for the ISD2500 devices has an internal pull-down device. These devices are configured at the factory with an internal sampling clock frequency centered to ±1 percent of specification. The frequency is then maintained to a variation of ±2.25 percent over the entire commercial temperature and operating voltage ranges. The internal clock has a ±5 percent tolerance over the industrial temperature and voltage range. A regulated power supply is recommended for industrial temperature range parts. If greater precision is required, the device can be clocked through the XCLK pin as follows:

Table 1: External Clock Sample Rates

Part Number	Sample Rate	Required Clock
ISD2532	8.0 KHz	1024 KHz
ISD2540	6.4 KHz	819.2 KHz
ISD2548	5.3 KHz	682.7 KHz
ISD2564	4.0 KHz	512 KHz

These recommended clock rates should not be varied because the antialiasing and smoothing filters are fixed, and aliasing problems can occur if the sample rate differs from the one recommended. The duty cycle on the input clock is not critical, as the clock is immediately divided by two. **If the XCLK is not used, this input must be connected to ground.**

SPEAKER OUTPUTS (SP+/SP-)

All devices in the ISD2500 series include an on-chip differential speaker driver, capable of driving 50 mW into 16 Ω from AUX IN (12.2 mW from memory).

The speaker outputs are held at V_{SSA} levels during record and power down. It is therefore not possible to parallel speaker outputs of multiple ISD2500 devices or the outputs of other speaker drivers.

NOTE *Connection of speaker outputs in parallel may cause damage to the device.*

A single output may be used alone (including a coupling capacitor between the SP pin and the speaker). These outputs may be used individually with the output signal taken from either pin. Using the differential outputs results in a 4 to 1 improvement in output power.

NOTE *Never ground or drive an unused speaker output.*

AUXILIARY INPUT (AUX IN)

The Auxiliary Input is multiplexed through to the output amplifier and speaker output pins when $\overline{CE}$ is HIGH, P/$\overline{R}$ is HIGH, and playback is currently not active or if the device is in playback overflow. When cascading multiple ISD2500 devices, the AUX IN pin is used to connect a playback signal from a following device to the previous output speaker drivers. For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.

ADDRESS/MODE INPUTS (AX/MX)

The Address/Mode Inputs have two functions depending on the level of the two Most Significant Bits (MSB) of the address (A7 and A8).

If either or both of the two MSBs are LOW, the inputs are all interpreted as address bits and are used as the start address for the current record or playback cycle. The address pins are inputs only and do not output internal address information as the operation progresses. Address inputs are latched by the falling edge of $\overline{CE}$.

If both MSBs are HIGH, the Address/Mode Inputs are interpreted as Mode bits according to the Operational Mode table on page 5. There are six operational modes (M0. . . M6) available as indicated in the table. It is possible to use multiple operational modes simultaneously. Operational Modes are sampled on each falling edge of $\overline{CE}$, and thus Operational Modes and direct addressing are mutually exclusive.

OPERATIONAL MODES

The ISD2500 series is designed with several built-in Operational Modes that provide maximum functionality with minimum additional components. These are described in detail below. The Operational Modes use the address pins on the ISD2500 devices, but are mapped outside the valid address range. When the two Most Significant Bits (MSB) are HIGH (A7 and A8), the remaining address signals are interpreted as mode bits and not as address bits. Therefore, Operational Modes and direct addressing are not compatible and cannot be used simultaneously.

There are two important considerations for using Operational Modes. First, all operations begin initially at address 0, which is the beginning of the ISD2500 address space. Later operations can begin at other address locations, depending on the Operational Mode(s) chosen. In addition, the address pointer is reset to 0 when the device is changed from record to playback, playback to record (except M6 mode), or when a Power-Down cycle is executed.

Second, Operational Modes are executed when $\overline{CE}$ goes LOW and the two MSBs are HIGH. This Operational Mode remains in effect until the next LOW-going $\overline{CE}$ signal, at which point the current Address/Mode levels are sampled and executed.

Table 2: Operational Modes

Mode Control	Function	Typical Use	Jointly Compatible[1]
M0	Message cueing	Fast-forward through messages	M4, M5, M6
M1	Delete $\overline{EOM}$ markers	Position $\overline{EOM}$ marker at the end of the last message	M3, M4, M5, M6
M2	Not applicable	Reserved	N/A
M3	Looping	Continuous playback from Address 0	M1, M5, M6
M4	Consecutive addressing	Record/play multiple consecutive messages	M0, M1, M5
M5	$\overline{CE}$ level-activated	Allows message pausing	M0, M1, M3, M4
M6	Push-button control	Simplified device interface	M0, M1, M3

1. Indicates additional Operational Modes which can be used simultaneously with the given mode.

OPERATIONAL MODES DESCRIPTION

The Operational Modes can be used in conjunction with a microcontroller, or they can be hardwired to provide the desired system operation.

M0 — MESSAGE CUEING

Message Cueing allows the user to skip through messages, without knowing the actual physical addresses of each message. Each $\overline{CE}$ LOW pulse causes the internal address pointer to skip to the next message. This mode should be used for playback only, and is typically used with the M4 Operational Mode.

M1 — DELETE $\overline{EOM}$ MARKERS

The M1 Operational Mode allows sequentially recorded messages to be combined into a single message with only one $\overline{EOM}$ marker set at the end of the final message. When this Operational Mode is configured, messages recorded sequentially are played back as one continuous message.

M2 — UNUSED

When Operational Modes are selected, the M2 pin should be LOW.

M3 — MESSAGE LOOPING

The M3 Operational Mode allows for the automatic, continuously repeated playback of the message located at the beginning of the address space. A message can completely fill the ISD2500 device and will loop from beginning to end without $\overline{OVF}$ going LOW.

M4 — CONSECUTIVE ADDRESSING

During normal operations, the address pointer will reset when a message is played through to an $\overline{EOM}$ marker. The M4 Operational Mode inhibits the address pointer reset on $\overline{EOM}$, allowing messages to be played back consecutively.

M5 — $\overline{CE}$-LEVEL ACTIVATED

The default mode for ISD2500 devices is for $\overline{CE}$ to be edge-activated on playback and level-activated on record. The M5 Operational Mode causes the $\overline{CE}$ pin to be interpreted as level-activated as opposed to edge-activated during playback. This is specifically useful for terminating playback operations using the $\overline{CE}$ signal.

In this mode, $\overline{CE}$ LOW begins a playback cycle, at the beginning of the device memory. The playback cycle continues as long as $\overline{CE}$ is held LOW. When $\overline{CE}$ goes HIGH, playback will immediately end. A new $\overline{CE}$ LOW will restart the message from the beginning unless M4 is also HIGH.

M6 — PUSH-BUTTON MODE

The ISD2500 series of devices contain a Push-Button Operational Mode. The Push-Button Mode is used primarily in very low-cost applications and is designed to minimize external circuitry and components, thereby reducing system cost. In order to configure the device in Push-Button Operational Mode, the two most significant address bits must be HIGH, and the M6 mode pin must also be HIGH. A device in this mode always powers down at the end of each playback or record cycle after $\overline{CE}$ goes HIGH.

When this operational mode is implemented, several of the pins on the device have alternate functionality:

Table 3: Alternate Functionality in Pins

Pin Name	Alternate Functionality in Push-Button Mode
$\overline{CE}$	Start/Pause Push-Button (LOW pulse-activated)
PD	Stop/Reset Push-Button (HIGH pulse activated)
$\overline{EOM}$	Active-HIGH Run Indicator

$\overline{CE}$ PIN (START/PAUSE)

In Push-Button Operational Mode, $\overline{CE}$ acts as a LOW-going pulse-activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/$\overline{R}$ pin. A subsequent pulse on the $\overline{CE}$ pin, before an EOM is reached in playback or an overflow condition occurs, will cause the device to pause. The address counter is not reset, and another $\overline{CE}$ pulse will cause the device to continue the operation from the place where it was paused.

PD PIN (STOP/RESET)

In push-button Operational Mode, PD acts as a HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated and the address pointer is reset to address 0, the beginning of the message space.

$\overline{EOM}$ PIN (RUN)

In Push-Button Operational Mode, $\overline{EOM}$ becomes an active-HIGH RUN signal which can be used to drive an LED or other external device. It is HIGH whenever a record or playback operation is in progress.

Recording in Push-Button Mode

1. The PD pin should be LOW, usually using a pull-down resistor.
2. The P/$\overline{R}$ pin is taken LOW.
3. The $\overline{CE}$ pin is pulsed LOW. Recording starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. The $\overline{CE}$ pin is pulsed LOW. Recording pauses, $\overline{EOM}$ goes back LOW. The internal address pointers are not cleared, but an $\overline{EOM}$ marker is stored in memory to point to the message end. The P/$\overline{R}$ pin may be taken HIGH at this time. Any subsequent $\overline{CE}$ would start a playback at address 0.
5. The $\overline{CE}$ pin is pulsed LOW. Recording starts at the next address after the previous set $\overline{EOM}$ marker. $\overline{EOM}$ goes back HIGH.

NOTE *If the M1 Operational Mode pin is also HIGH, the just previously written $\overline{EOM}$ bit is erased, and recording starts at that address.)*

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6. When the recording sequences are finished, the final $\overline{CE}$ pulse LOW will end the last record cycle, leaving a set $\overline{EOM}$ marker at the message end. Recording may also be terminated by a HIGH level on PD, which will leave a set $\overline{EOM}$ marker.

Playback in Push-Button Mode

1. The PD pin should be LOW.
2. The P/$\overline{R}$ pin is taken HIGH.
3. The $\overline{CE}$ pin is pulsed LOW. Playback starts, $\overline{EOM}$ goes HIGH to indicate an operation in progress.
4. If the $\overline{CE}$ pin is pulsed LOW or an $\overline{EOM}$ marker is encountered during an operation, the part will pause. The internal address pointers are not cleared, and $\overline{EOM}$ goes back LOW. The P/$\overline{R}$ pin may be changed at this time. A subsequent record operation would not reset the address pointers and the recording would begin where playback ended.
5. $\overline{CE}$ is again pulsed LOW. Playback starts where it left off, with $\overline{EOM}$ going HIGH to indicate an operation in progress.
6. Playback continues as in steps 4 and 5 until PD is pulsed HIGH or overflow occurs.
7. If in overflow, pulling $\overline{CE}$ LOW will reset the address pointer and start playback from the beginning. After a PD pulse, the part is reset to address 0.

NOTE *Push-button Mode can be used in conjunction with modes M0, M1, and M3.*

GOOD AUDIO DESIGN PRACTICES

ISD products are very high-quality single-chip voice recording and playback systems. To ensure the highest quality voice reproduction, it is important that good audio design practices on layout and power supply decoupling be followed. See the Application Information for details.

ISD1000A COMPATIBILITY

The ISD2500 series of devices is designed to provide upward compatibility with the ISD1000A family. When designing with the ISD2500 series, the following differences should be noted.

The ISD2532/40/48/64 devices have 256K storage cells designed to provide 32 seconds of storage at a sampling rate of 8.0 KHz. This is twice the amount of storage of the ISD1000A family. To enable the same addressing resolution, one additional address pin has been added. The address space of each device is divisible into 320 increments with valid addressing from 00 to 13F Hex.

OVERFLOW

The ISD1000A series combined two functions on the $\overline{EOM}$ pin: end-of-message indication and overflow. The ISD2500 separates these two functions. Pin 25 (PDIP package) remains as $\overline{EOM}$, but outputs only the $\overline{EOM}$ signal indication. Pin 22 (PDIP package) becomes $\overline{OVF}$ and pulses LOW only when the device reaches its end of memory, or is "full." This change allows easy message cueing and addressability across device boundaries. This also means that the M2 Operational Mode found in the ISD1000A family is not implemented in the ISD2500 series.

PUSH-BUTTON MODE

The ISD2500 series includes an additional Operational Mode called Push-Button Mode. This provides an alternative interface to the record and playback functions of the part. The $\overline{CE}$ and PD pins become redefined as edge-activated "push-buttons." A pulse on $\overline{CE}$ initiates a cycle, and if triggered again, pauses the current cycle without resetting the address pointer (i.e., a Start or Pause function). PD stops any current cycle and resets the address pointer to the beginning of the message space (i.e., a Stop and Reset function). Additionally, the $\overline{EOM}$ pin functions as an active-HIGH run indicator, and can be used to drive an LED indicating a record or playback operation is in progress. Devices in the Push-Button Mode cannot be cascaded.

LOOPING MODE

The ISD2500 series can loop with a message that completely fills the memory space.

NOTE *Additional descriptions of ISD2500 device functionality and application examples are provided in the ISD Application Information in this book.*

TIMING DIAGRAMS

Figure 2: Record

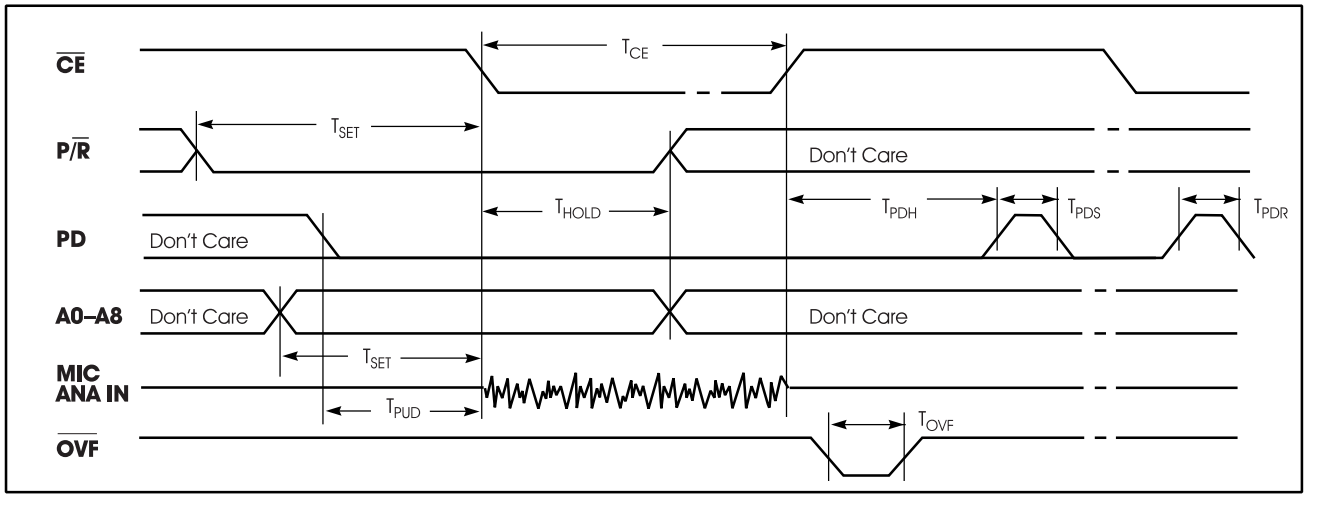

Figure 3: Playback

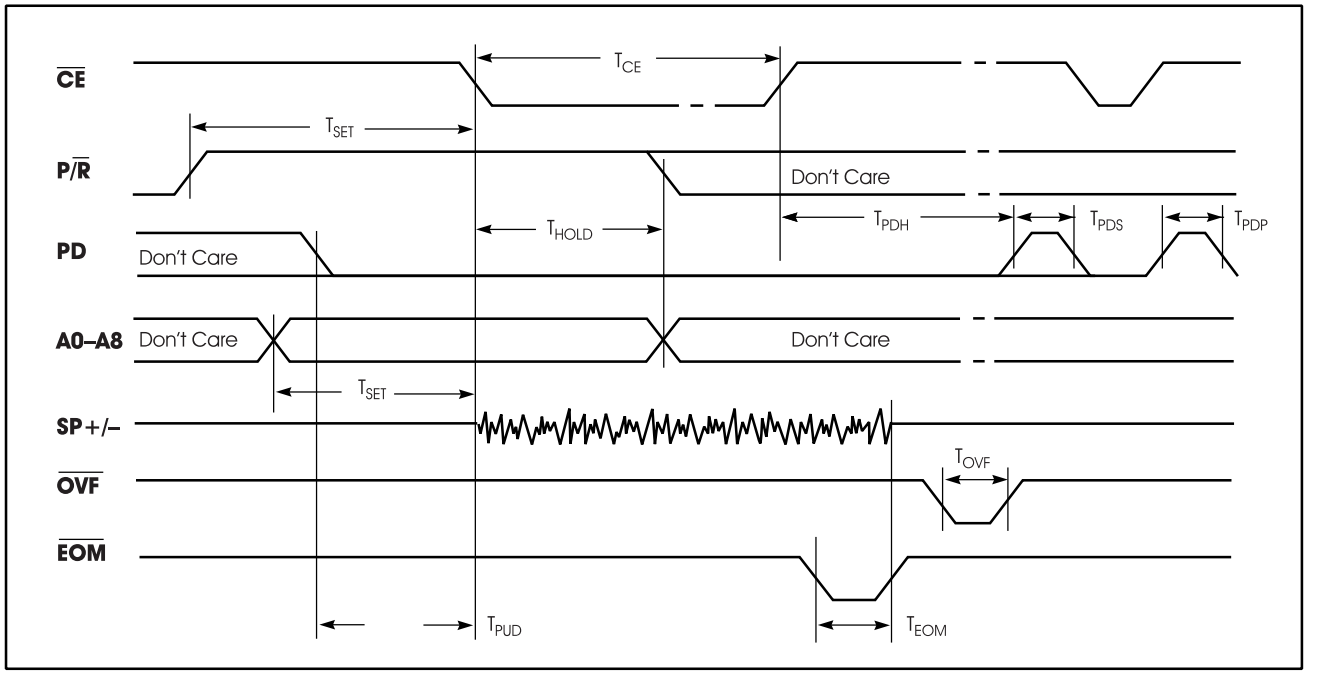

Table 4: Absolute Maximum Ratings (Packaged Parts)[1]

Condition	Value
Junction temperature	150°C
Storage temperature range	–65°C to +150°C
Voltage applied to any pin	(V_{SS} – 0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (Input current limited to ±20 mA)	(V_{SS} – 1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering – 10 seconds)	300°C
V_{CC} – V_{SS}	–0.3 V to +7.0 V

1. *Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions.*

Table 5: Operating Conditions (Packaged Parts)

Condition	Value
Commercial operating temperature range[1]	0°C to +70°C
Industrial operating temperature range[1]	–40°C to +85°C
Supply voltage (V_{CC})[2]	+4.5 V to +5.5 V
Ground voltage (V_{SS})[3]	0 V

1. *Case temperature.*
2. *V_{CC} = V_{CCA} = V_{CCD}.*
3. *V_{SS} = V_{SSA} = V_{SSD}.*

Table 6: DC Parameters (Packaged Parts)

Symbol	Parameters	Min[2]	Typ[1]	Max[2]	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	V_{CC} – 0.4			V	I_{OH} = –10 µA
V_{OH1}	$\overline{OVF}$ Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH2}	$\overline{EOM}$ Output High Voltage	V_{CC} – 1.0	V_{CC} – 0.8		V	I_{OH} = –3.2 mA
I_{CC}	V_{CC} Current (Operating)		25	30	mA	R_{EXT} = ∞ [3]
I_{SB}	V_{CC} Current (Standby)		1	10	µA	[3]
I_{IL}	Input Leakage Current			±1	µA	
I_{ILPD}	Input Current HIGH w/Pull Down			130	µA	Force V_{CC} [4]
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Preamp In Input Resistance	4	9	15	KΩ	MIC and MIC REF Pins
R_{AUX}	AUX INPUT Resistance	5	11	20	KΩ	
$R_{ANA\ IN}$	ANA IN Input Resistance	2.3	3	5	KΩ	
A_{PRE1}	Preamp Gain 1	21	24	26	dB	AGC = 0.0 V