Product Change Notification - SYST-05GIIG496 (Printer Friendly)

Date:

15 Jan 2018

Product Category:

32-bit PIC Microcontrollers

Affected CPNs:

Notification subject:

Data Sheet - PIC32MZ Graphics (DA) Family Datasheet Data Sheet Document Revision

Notification text:

SYST-05GIIG496

Microchip has released a new DeviceDoc for the PIC32MZ Graphics (DA) Family Datasheet of devices. If you are using one of these devices please read the document located at PIC32MZ Graphics (DA) Family Datasheet.

Notification Status: Final

Description of Change: This revision includes the following major changes, which are referenced by their respective chapter in Table A-5. In addition, minor updates to text and formatting were incorporated throughout the document.
1.0 "Device Overview" The PIC32MZ DA Family Block Diagram was updated (see Figure 1-1). The 176-pin LQFP pin number for SDA3 in the I1C1 through I2C5 Pinout I/O Descriptions was updated (see Table 1-10). The 169-pin LFBGA pin numbers for EBIOE and EBIWE in the EBI Pinout I/O Descriptions were updated (see Table 1-13). 2.0 "Guidelines for Getting Started with 32-bit Microcontrollers" The following sections were added: •2.7.1 "Crystal Oscillator Design Consideration" •2.9 "Considerations When Interfacing to Remotely Powered Circuits" 4.0 "Memory Organization" The PIC32MZ DA Family Memory Map was updated (see Figure 4-1). 10.0 "Direct Memory Access (DMA) Controller" CRCTYP bit number references in the DMA CRC Control Register were updated (see Register 10-4, Register 10-5, and Register 10-6). 36.0 "Graphics LCD (GLCD) Controller" The key features for the module were updated. 37.0 "2-D Graphics Processing Unit (GPU)" The key features for the module were updated. The GPURESET bit reference in Note 2 was updated. 38.0 "DDR2 SDRAM Controller" The definition when SCLLBPASS is set to '0' was updated and the SCLPHCAL bit was added (see Register 38-24). The following registers were added: •Register 38-31: "DDRPHYDLLCTRL: DDR PHY Trim Register" •Register 38-32: "DDRPHYDLLR: DDR PHY DLL Recalibrate Register" •Register 38-33: "DDRSCLCFG2: DDR SCL Configuration Register 2" •Register 38-34: "DDRPHYSCLADR: DDR PHY SCL Address Register" 41.0 "Special Features" The Device Configuration Word 0 registers, DEVCFG0/ADEVCFG0, was extensively updated (see Register 41-3). The bit value definitions for the FCKSM<1:0> bits and the POSCMOD<1:0> bits in the Device Configuration Word 1 registers, DEVCFG1/ADEVCFG1, were updated (see Register 41-4). 44.0 "Electrical Characteristics" Parameter DO50 (COSCO) was removed from the Capacitive Loading Requirements on Output Pins (see Table 44-22).

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 15 Jan 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):
PIC32MZ Graphics (DA) Family Datasheet

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