ISL8278M

Digital DC/DC PMBus 33A Module

FN8924
Rev.1.00
Aug 17, 2017

The ISL8278M is a 33A step-down, DC/DC power supply module with an integrated digital PWM controller, synchronous power switches, an inductor, and passives. Only bulk input and output capacitors are needed to finish the design. The 33A of continuous output current can be delivered without the need for airflow or a heatsink. The thermally enhanced HDA module is capable of dissipating heat directly into the PCB.

The ISL8278M uses ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. The ISL8278M comes with a preprogrammed configuration for operating in a pin-strap mode. Output voltage, switching frequency, and the device SMBus address can be programmed with external resistors. More configurations, such as soft-start and fault limits can be easily programmed or changed using a PMBus compliant serial bus interface. PMBus can be used to monitor voltages, current, temperatures, and fault status. The ISL8278M is supported by the PowerNavigator™ software, a Graphical User Interface (GUI) that can be used to configure modules for a desired solution.

The ISL8278M is available in a 41 Ld compact 17mmx19mm HDA module with a very low profile height of 3.6mm, suitable for automated assembly by standard surface mount equipment. The ISL8278M is RoHS compliant by exemption.

Features

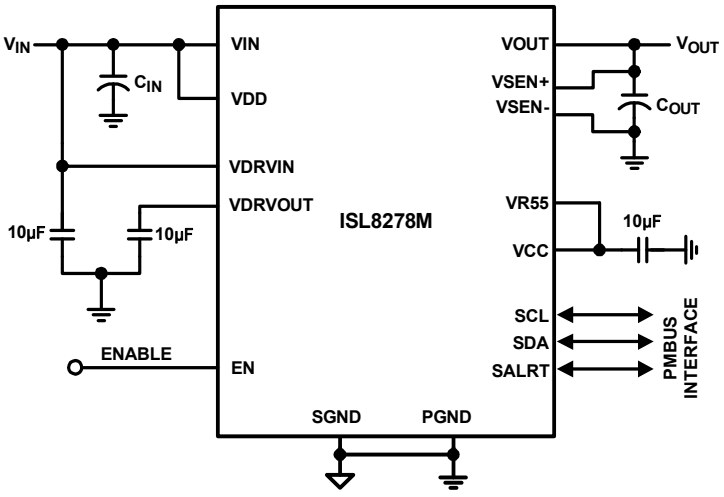
- Complete digital switch-mode power supply
  - Wide V_{IN} range: 4.5V to 14V
  - Programmable V_{OUT} range: 0.6V to 5V
- PMBus compliant I^2C communication interface
  - Programmable V_{OUT}, margining, UV/OV, I_{OUT} limit, soft-start/stop, sequencing, and external synchronization
  - Monitor: V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, switching frequency, and faults
- ChargeMode control architecture
- ±1.0% V_{OUT} accuracy over line, load, and temperature
- Power-good indicator
- Over-temperature protection
- Internal nonvolatile memory and fault logging
- Patented thermally enhanced HDA package
- Intuitive configuration using PowerNavigator

Applications

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

Related Literature

- For a full list of related documents, visit our website
  - ISL8278M product page



NOTE:

1. Only bulk input and output capacitors are required to finish the design.

FIGURE 1. A COMPLETE DIGITAL SWITCH-MODE POWER SUPPLY

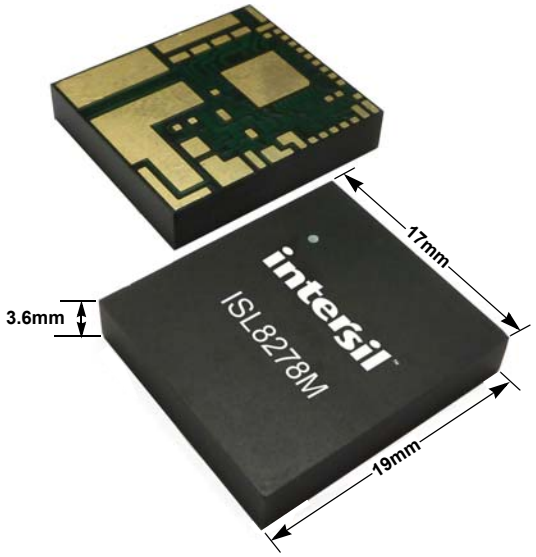


FIGURE 2. A SMALL PACKAGE FOR HIGH POWER DENSITY

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Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8278MAIRZ	ISL8278MA	-40 to +85	41 Ld 17x19 HDA	Y41.17x19
ISL8278MEVAL1Z	Evaluation Board			

NOTES:

2. Add "-T" suffix for 500 unit or "-T1" suffix for 100 unit tape and reel options. Refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see the product information page for ISL8278M. For more information on MSL, see TB363.

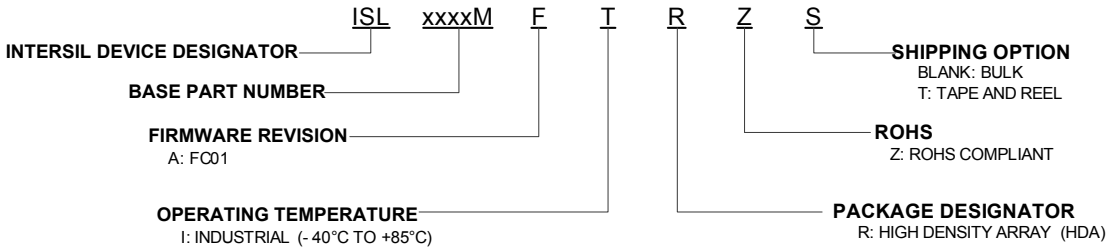
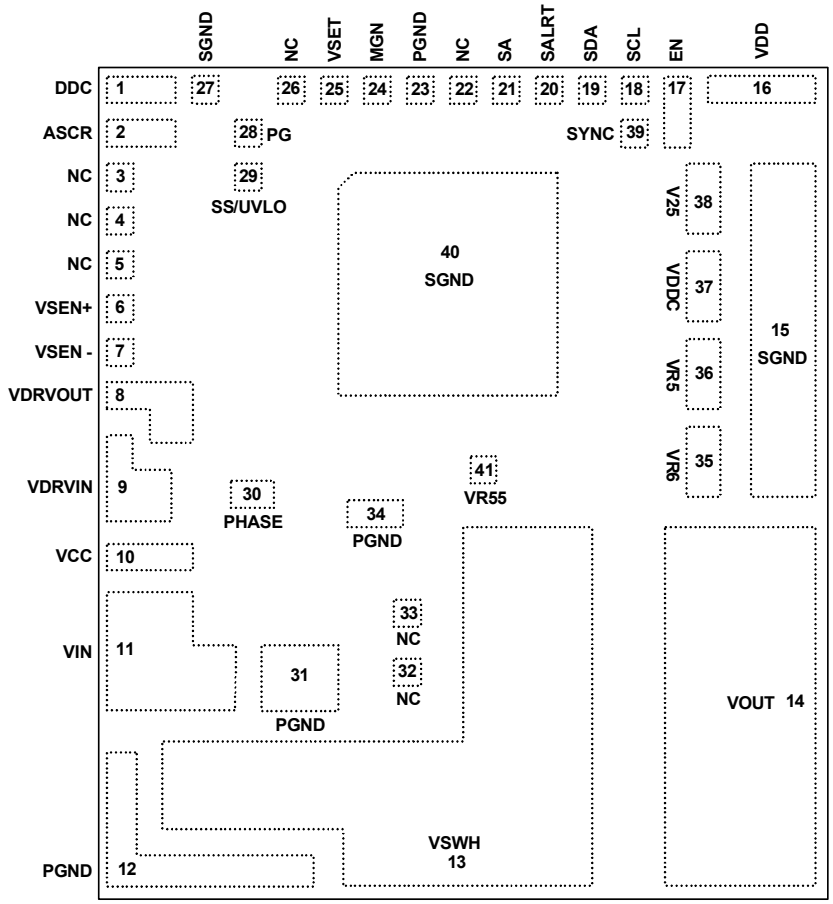


TABLE 1. TABLE OF DIFFERENCES AMONG THE FAMILY OF PARTS

PARAMETERS	ISL8278M	ISL8271M	ISL8270M	ISL8277M
V_{IN} (min) (V)	4.5	4.5	4.5	4.5
V_{IN} (max) (V)	14	14	14	14
V_{OUT} (min) (V)	0.6	0.6	0.6	0.6
V_{OUT} (max) (V)	5	5	5	5
I_{OUT} (max) (A)	33	33	25	25
I_Q (mA)	40	40	40	40
Peak Efficiency (%)	96	96	96	96
POR	Yes	Yes	Yes	Yes
Switching Freq. (min) (MHz)	0.296	0.296	0.296	0.296
Switching Freq. (max) MHz	1.067	1.067	1.067	1.067
Control Type	Digital	Digital	Digital	Digital
SYNCH Capability	Yes	Yes	Yes	Yes
Current Sharing	No	No	No	No
Tracking	No	No	No	No
Digital	Yes	Yes	Yes	Yes
Qualification Level	Standard	Standard	Standard	Standard

Pin Configuration

ISL8278M
(41 LD HDA)
TOP VIEW



Pin Descriptions

PIN	LABEL	TYPE	DESCRIPTION
1	DDC	I/O	A Digital-DC™ bus. This dedicated bus provides the communication channel between devices for features such as sequencing and fault spreading. The DDC pin on all Digital-DC devices should be connected together. A pull-up resistor is required for this application.
2	ASCR	I	ChargeMode control ASCR parameters selection pin. Used to set ASCR gain and residual values.
6	VSEN+	I	Differential output voltage sense feedback. Connect to the positive output regulation point.
7	VSEN-	I	Differential output voltage sense feedback. Connect to the negative output regulation point.
8	VDRVOUT	PWR	Output of internal regulator for powering internal MOSFET driver. Connect a 10µF bypass capacitor to this pin. The regulator output is dedicated to powering internal MOSFET drivers. Do not use this regulator for any other purpose. For applications with V_{IN} less than 5.2V, use an external 5V supply or connect this pad to VIN.
9	VDRVIN	PWR	Input supply to internal regulator for powering internal MOSFET drivers. Connect this pad to VIN.
10	VCC	PWR	Bias pin for internal regulator. Connect VCC pad to VR55 pin directly with a short loop trace. Not recommended to power external circuit.
11	VIN	PWR	Main input supply. Refer to "PCB Layout Guidelines" on page 21 for the decoupling capacitors placement from VIN to PGND.

Pin Descriptions (Continued)

PIN	LABEL	TYPE	DESCRIPTION
12, 23, 31, 34	PGND	PWR	Power ground. Refer to "PCB Layout Guidelines" on page 21 for the PGND pad connections and decoupling capacitors placement.
13	VSWH	PWR	Switch node. Refer to "PCB Layout Guidelines" on page 21 for connecting VSWH pads to electrically isolated PCB copper island to dissipate internal heat.
14	VOUT	PWR	Power supply output. Range: 0.6V to 5V. Refer to "Derating Curves" on page 12 for maximum recommended output current at various output voltages.
15, 27, 40	SGND	PWR	Controller signal ground. Refer to "PCB Layout Guidelines" on page 21 for the SGND pad connections.
16	VDD	PWR	Input supply to digital controller. Connect VDD pad to VIN supply. Refer to "PCB Layout Guidelines" on page 21 for the decoupling capacitors placement from VDD to SGND.
17	EN	I	External enable input. Logic high enables the module.
18	SCL	I/O	Serial clock input. A pull-up resistor is required for this application.
19	SDA	I/O	Serial data. A pull-up resistor is required for this application.
20	SALRT	O	Serial alert. A pull-up resistor is required for this application.
21	SA	I	Serial bus address select pin. Refer to Table 9 on page 18 for list of resistor values to set various serial bus address.
24	MGN	I	External V_{OUT} margin control pin. Active high (>2V) signal at this pin sets V_{OUT} margin high, active low (<0.8V) sets V_{OUT} margin low, and high impedance (float) will bring V_{OUT} back to nominal voltage. Factory default range for margining is nominal V_{OUT} ±5%. When using PMBus to control margin command, leave this pin as no connect.
25	VSET	I	Output voltage selection pin. Refer to Table 4 on page 16 for list of resistor values to set various output voltages.
28	PG	O	Power-good output. Power-good output can be an open drain that requires pull-up resistor or push-pull output that can drive a logic input.
29	SS/UVLO	I	Soft-start/stop and undervoltage lockout selection pin. Used to set turn on/off delay and ramp time as well as input UVLO threshold levels. Refer to Table 5 on page 17 and Table 8 on page 18 for list of resistors.
30	PHASE	PWR	Switch node pad for DCR sensing. Electrically shorted inside to VSWH, but for higher current sensing accuracy connect PHASE pad to VSWH pad externally. Refer to "PCB Layout Guidelines" on page 21.
35	VR6	PWR	6V internal reference supply voltage.
36	VR5	PWR	5V internal reference supply voltage.
37	VDDC	PWR	VDD clean. Noise at the VDD pin is filtered by an internal ferrite bead and capacitor. For VDD > 6V, leave this pin as no connect. For 5.5 ≤ VDD ≤ 6V, connect the VDDC pin to VR6 pin. For 4.5 ≤ VDD < 5.5V, connect the VDDC pin to VR6 and the VR5 pin.
38	V25	PWR	2.5V internal reference supply voltage.
39	SYNC	I/O	The SYNC pin can be input to external clock for frequency synchronization or output to supply clock signal to other modules for synchronization. Refer to Table 6 on page 17 for list of resistor values to program various switching frequencies.
41	VR55	PWR	Internal 5.5V bias for internal regulator use only. Connect VR55 pin directly to VCC pin. Not recommended to power external circuit.
3, 4, 5, 22, 26, 32, 33	NC		These are test pins and are not electrically isolated. Leave these pins as no connect.

ISL8278M Internal Block Diagram

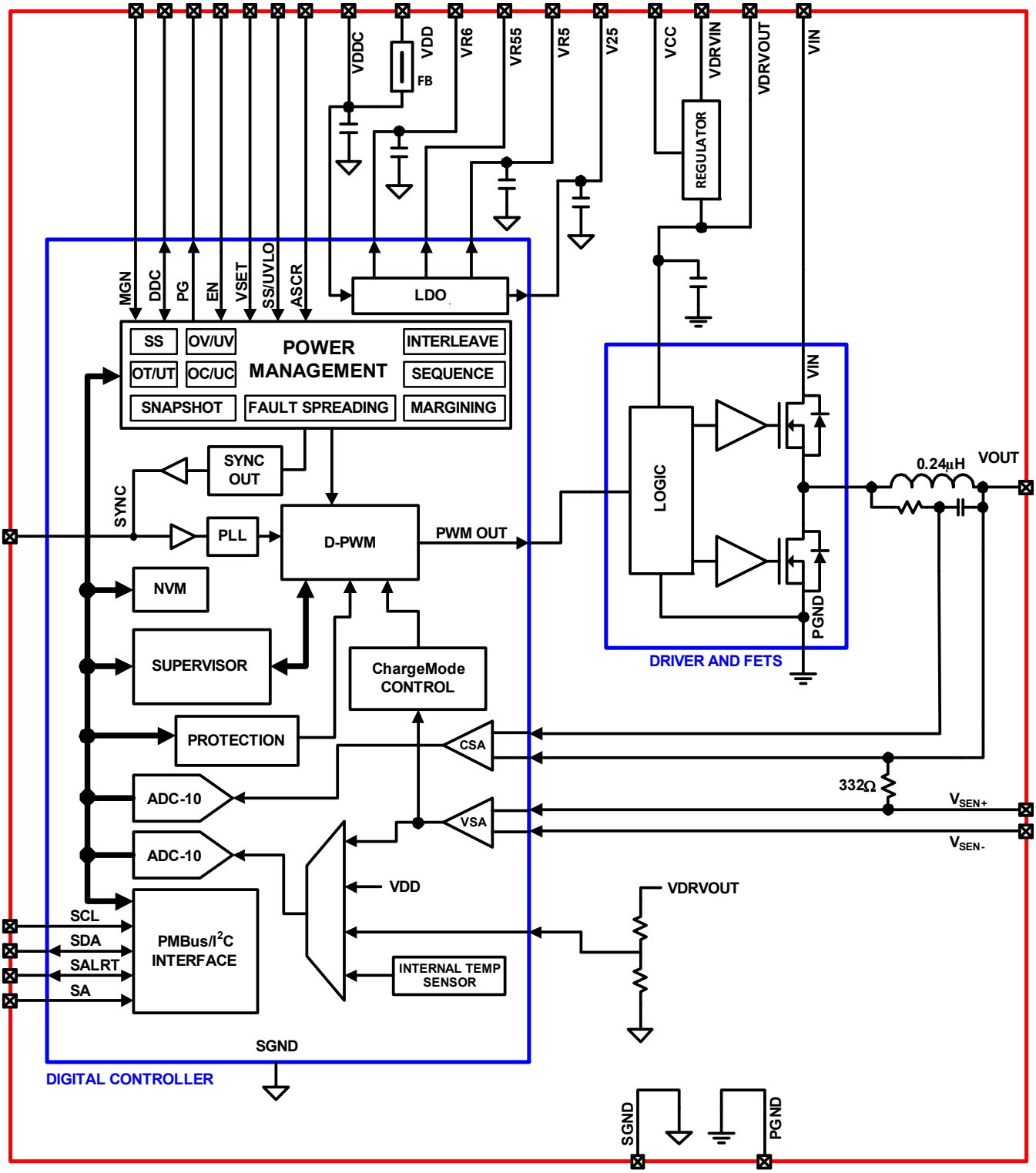


FIGURE 3. ISL8278M INTERNAL BLOCK DIAGRAM

Absolute Maximum Ratings

Input Supply Voltage, VIN Pin . . . . . -0.3V to 17V
Input Supply Voltage for Controller, VDD, VDDC Pin. . . . . -0.3V to 17V
Input Gate Driver Supply Voltage, VDRVIN Pin . . . . . -0.3V to 17V
Output Gate Driver Supply Voltage, VDRVOUT Pin . . . . . -0.3V to 6V
Output Voltage, VOUT Pin . . . . . -0.3V to 6.0V
Switch Node Referenced to PGND Pin, VSWH Pin . . . . . -0.3V to 25V
Switch Node for DCR Sensing Referenced to
SGND Pin, PHASE Pin . . . . . -0.3V to 25V
Input Bias Voltage for Internal Regulator, VCC Pin. . . . . -0.3V to 6.5V
6V Internal Reference Supply Voltage, VR6 Pin . . . . . -0.3V to 6.6V
Internal Reference Supply Voltage, VR5, VR55 Pin . . . . . -0.3V to 6.5V
2.5V Internal Reference Supply Voltage, V25 Pin . . . . . -0.3V to 3V
Logic I/O Voltage for DDC, EN, MGN, PG, ASCR,
SA, SCL, SDA, SALRT, SYNC, SS/UVLO, V_{SET} . . . . . -0.3V to 6.0V
Analog Input Voltages for
V_{SEN+}, X_{TEMP+} . . . . . -0.3V to 6.0V
V_{SEN-}, X_{TEMP-} . . . . . -0.3V to 0.3V
ESD Rating
Human Body Model (Tested per JS-001-2014). 2000V
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JS-002-2014) 750V
Latch-Up (Tested per JESD78E; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
41 LD HDA Package (Notes 5, 6)	7.5	2.2

Maximum Junction Temperature (Plastic Package) . . . . . +125°C
Storage Temperature Range. . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . refer to Figure 31 on page 22

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 4.5V to 14V
Input Supply Voltage Range for Controller, V_{DD} . . . . . 4.5V to 14V
Output Voltage Range, V_{OUT} . . . . . 0.6V to 5V
Output Current Range, $I_{OUT(DC)}$ (Note 9). . . . . 0A to 33A
Operating Junction Temperature Range, T_J. . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the module mounted on an evaluation board 3x4.5 inch in size with 2oz surface and 2oz buried planes and multiple via interconnects as specified in "ISL8278MEVAL1Z Evaluation Board User Guide", on the ISL8278M product page.
6. For θ_{JC}, the "case temp" location is the center of the package underside.

Electrical Specifications

$V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $C_{OUT} = 1340\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
INPUT AND SUPPLY CHARACTERISTICS						
Input Supply Current for Controller	I_{DD}	$V_{IN} = V_{DD} = 12V$, $V_{OUT} = 0V$, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
Internal Regulator Output Voltage	V_{DRVOUT}	V_{CC} connected to V_{R55}		5.2		V
5V Internal Reference Supply Voltage	V_{R5}	$I_{VR5} < 5mA$	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply Voltage	V_{25}		**2.25**	2.50	**2.75**	V
5.5V Internal Reference Supply Voltage	V_{R55}	$V_{DD} > 6V$; 0A to 80mA		5.7		V
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			10		Bits
Input Supply Voltage for Controller Read Back Total Error (Note 10)	$V_{DD\_READ\_ERR}$	PMBus read		±2		%FS
OUTPUT CHARACTERISTICS						
Output Voltage Adjustment Range	V_{OUT_RANGE}	$V_{IN} > V_{OUT} + 1.8V$	**0.54**		**5.5**	V
Output Voltage Set-Point Range	V_{OUT_RES}	Configured using PMbus		±0.025		%
Output Voltage Set-Point Accuracy (Notes 8, 10)	V_{OUT_ACCY}	Includes line, load, and temperature ($-20°C \le T_A \le +85°C$)	**-1**		**+1**	%FS
Output Voltage Readback Resolution	$V_{OUT\_READ\_RES}$			10		Bits

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $C_{OUT} = 1340\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Output Voltage Readback Total Error (Note 10)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**+2**	%FS
Output Current Readback Resolution	$I_{OUT\_READ\_RES}$			10		Bits
Output Current Range (Note 9)	I_{OUT_RANGE}				**33**	A
Output Current Readback Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load		±2		A
SOFT-START AND SEQUENCING						
Delay Time From Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using PMBus	**2**		**5000**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using PMBus	**0.5**		**100**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs
Delay Time From Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using PMBus	**2**		**5000**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms
Output Voltage Fall Time	t_{OFF_FALL}	Configured using PMBus	**0.5**		**100**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
POWER-GOOD						
Power-Good Delay	V_{PG_DELAY}	Configured using PMBus	**0**		**5000**	ms
TEMPERATURE SENSE						
Temperature Sense Range	T_{SENSE_RANGE}	Configurable using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	**-5**		**+5**	°C
External Temperature Sensor Accuracy	$XTEMP_{ACCY}$	Using 2N3904 NPN transistor		±5		°C
FAULT PROTECTION						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 10)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		V_{OUT} + 15		%
		Configured using PMBus	**V_{OUT} + 5**		**V_{OUT_MAX}**	%
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		V_{OUT} - 15		%
		Configured using PMBus	**0**		**V_{OUT} - 5**	%
V_{OUT} OV/UV Threshold Accuracy (Note 8)	V_{OUT_OV/UV_ACCY}		**-2**		**+2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 10)	I_{LIMIT_ACCY}	Tested at I_{OUT}_OC_FAULT_LIMIT = 40A		±10		%FS
Output Current Fault Response Time (Note 11)	I_{LIMIT_DELAY}	Factory default		3		t_{SW}
Over-Temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		125		°C
		Configured using PMBus	**-40**		**125**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C

Electrical Specifications $V_{IN} = V_{DD} = 12V$, $f_{SW} = 533kHz$, $C_{OUT} = 1340\mu F$, $T_A = -40°C$ to $+85°C$, unless otherwise noted. Typical values are at $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
OSCILLATOR AND SWITCHING CHARACTERISTICS						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**+5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC clock equal to 500kHz is not supported	**-10**		**+10**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	DDC, EN, MGN, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V_{MON}, V_{SET}	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus INTERFACE TIMING CHARACTERISTIC						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design.
8. V_{OUT} measured at the termination of the V_{SEN+} and V_{SEN-} sense points.
9. The MAX load current is determined by the thermal "Derating Curves" on page 12.
10. "FS" stand for Full Scale of recommended maximum operation range.
11. "t_{SW}" stands for time period of operation switching frequency.

Typical Performance Curves

Efficiency Performance

Operating condition: T_A = +25°C, No air flow. C_{OUT} = 1340µF. Typical values are used unless otherwise noted.

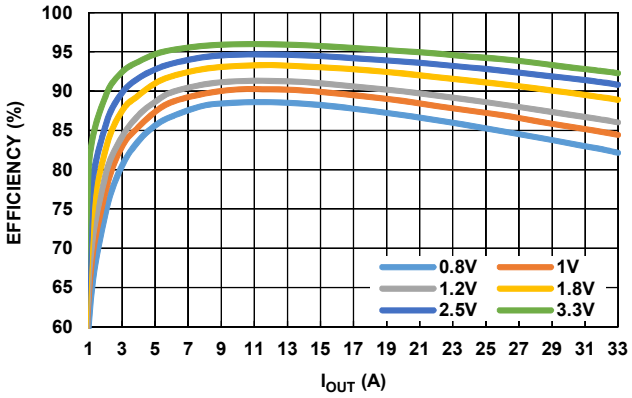


FIGURE 4. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 5V AND f_{SW} = 533kHz FOR VARIOUS OUTPUT VOLTAGES

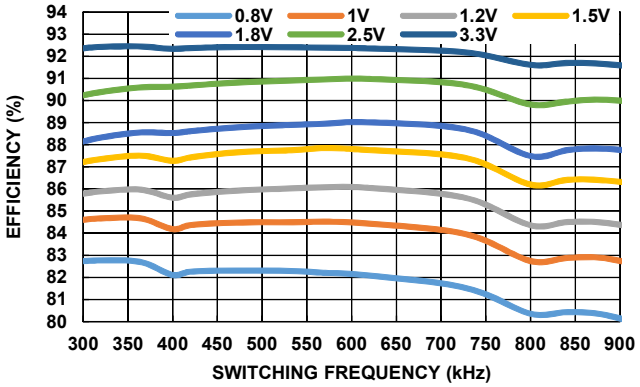


FIGURE 5. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 5V AND I_{OUT} = 33A FOR VARIOUS OUTPUT VOLTAGES

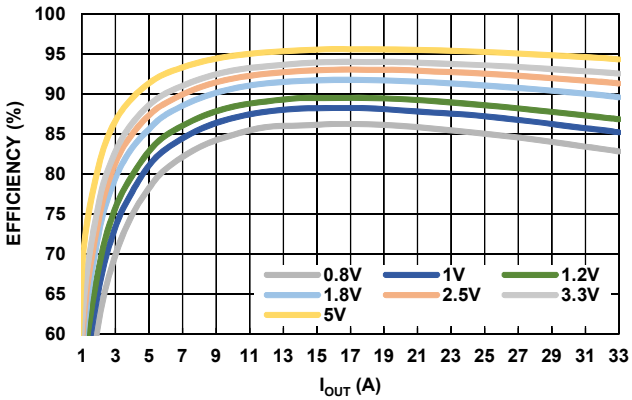


FIGURE 6. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 9V AND f_{SW} = 533kHz FOR VARIOUS OUTPUT VOLTAGES

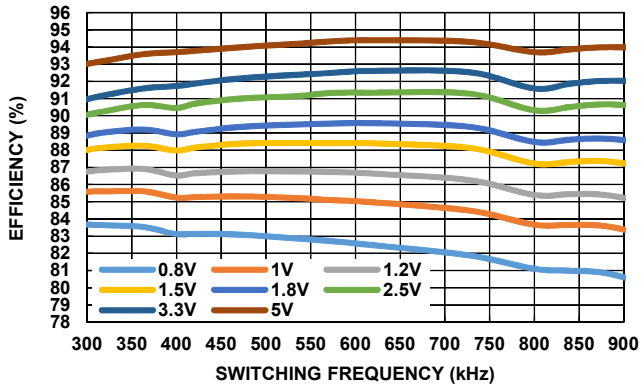


FIGURE 7. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 9V AND I_{OUT} = 33A FOR VARIOUS OUTPUT VOLTAGES

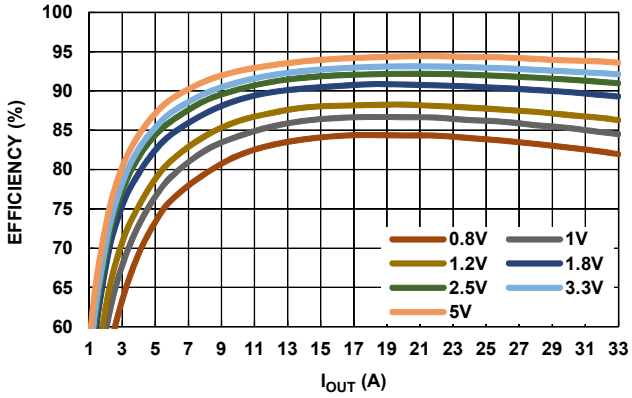


FIGURE 8. EFFICIENCY vs OUTPUT CURRENT AT V_{IN} = 12V AND f_{SW} = 533kHz FOR VARIOUS OUTPUT VOLTAGES

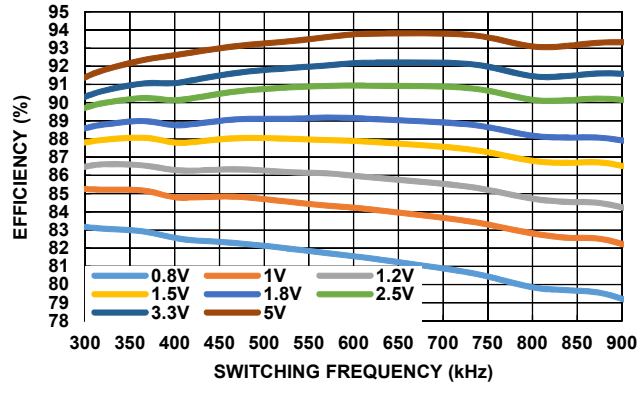


FIGURE 9. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 12V AND I_{OUT} = 33A FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves (Continued)

Transient Response Performance

Operating conditions: I_{OUT} = 0/16.5A, I_{OUT} slew rate >20A/µs, T_A = +25°C, OLFM airflow. Typical values are used unless otherwise noted.

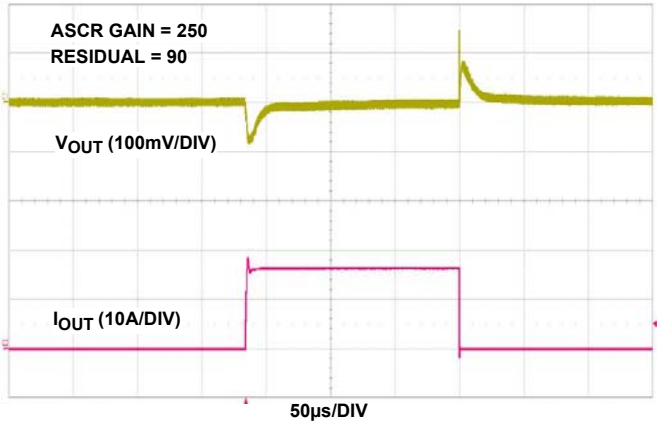


FIGURE 10. $5V_{IN}$ TO $1V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 533kHz, C_{OUT} = 4x100µF CERAMIC + 2x470µF POSCAP

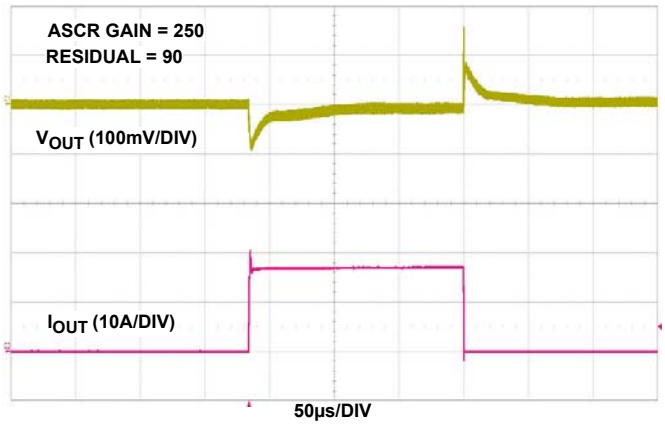


FIGURE 11. $5V_{IN}$ TO $1.8V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 615kHz, C_{OUT} = 3x100µF CERAMIC + 2x470µF POSCAP

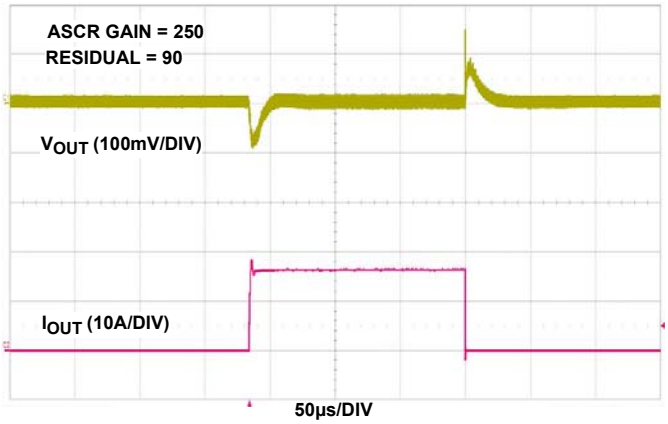


FIGURE 12. $12V_{IN}$ TO $1V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 533kHz, C_{OUT} = 4x100µF CERAMIC + 2x470µF POSCAP

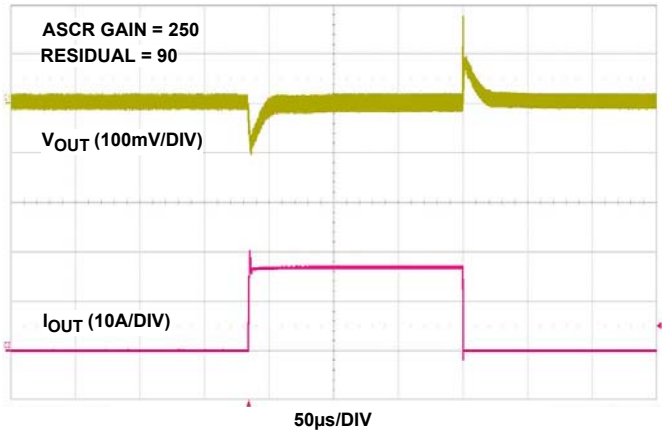


FIGURE 13. $12V_{IN}$ TO $1.8V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 615kHz, C_{OUT} = 3x100µF CERAMIC + 2x470µF POSCAP

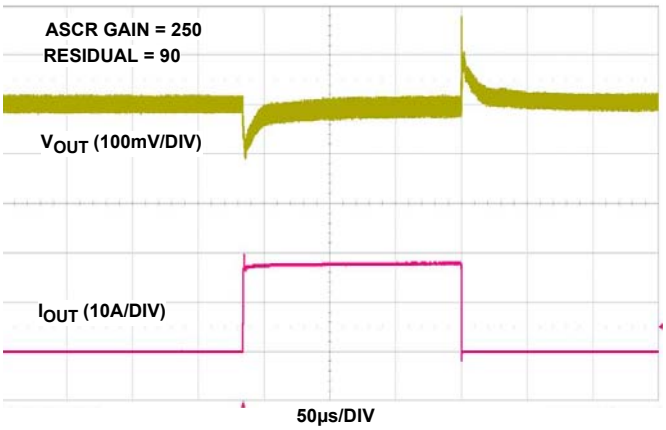


FIGURE 14. $12V_{IN}$ TO $3.3V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 615kHz, C_{OUT} = 3x100µF CERAMIC + 2x470µF POSCAP

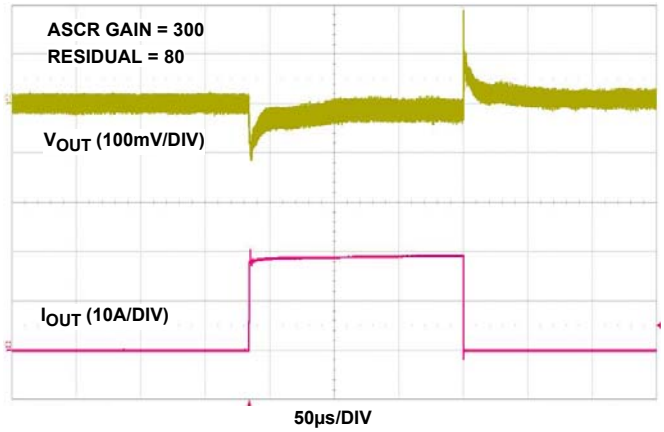


FIGURE 15. $12V_{IN}$ TO $5V_{OUT}$ TRANSIENT RESPONSE, f_{SW} = 727kHz, C_{OUT} = 3x100µF CERAMIC + 2x470µF POSCAP

Typical Performance Curves (Continued)

Derating Curves

All of the following curves were plotted at T_J = +115°C, f_{SW} = 533kHz

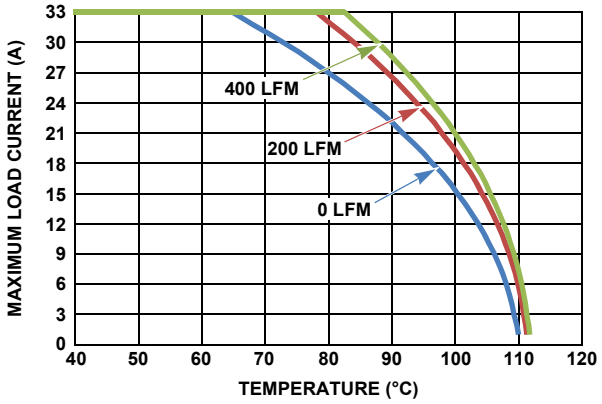


FIGURE 16. $5V_{IN}$ TO $1V_{OUT}$

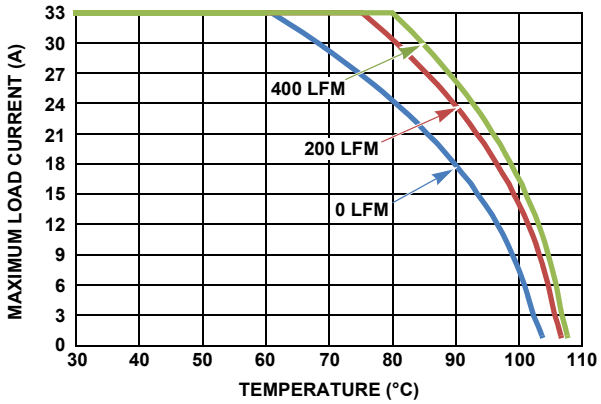


FIGURE 17. $12V_{IN}$ TO $1V_{OUT}$

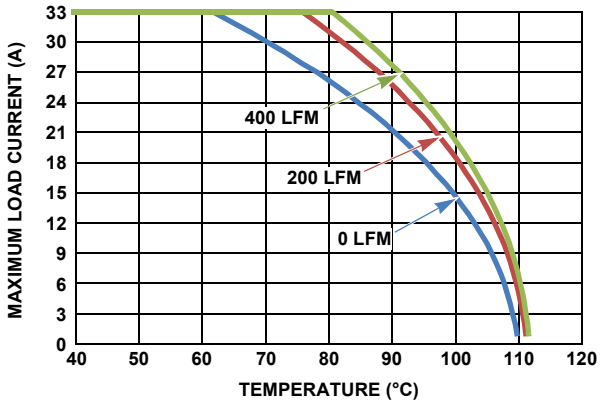


FIGURE 18. $5V_{IN}$ TO $1.2V_{OUT}$

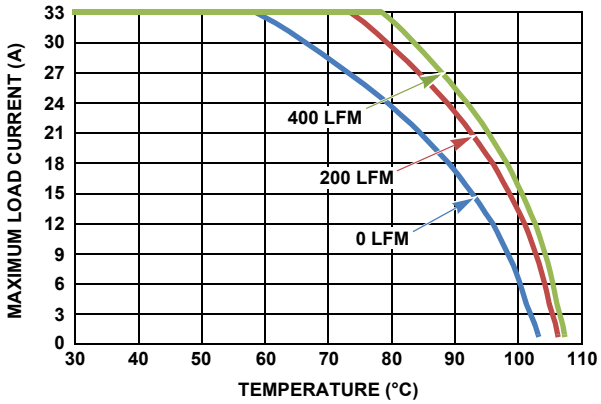


FIGURE 19. $12V_{IN}$ TO $1.2V_{OUT}$

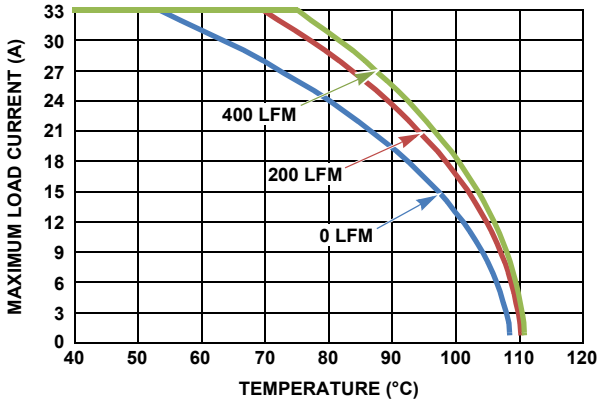


FIGURE 20. $5V_{IN}$ TO $1.8V_{OUT}$

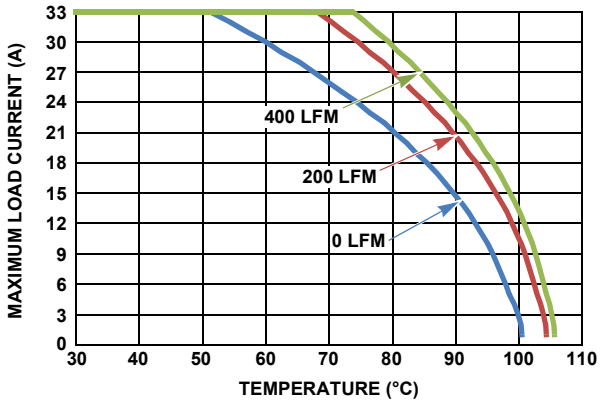


FIGURE 21. $12V_{IN}$ TO $1.8V_{OUT}$

Typical Performance Curves (Continued)

Derating Curves

All of the following curves were plotted at T_J = +115°C, f_{SW} = 533kHz

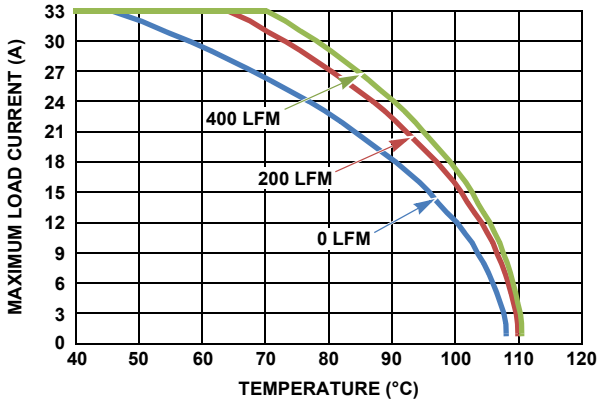


FIGURE 22. $5V_{IN}$ TO $2.5V_{OUT}$

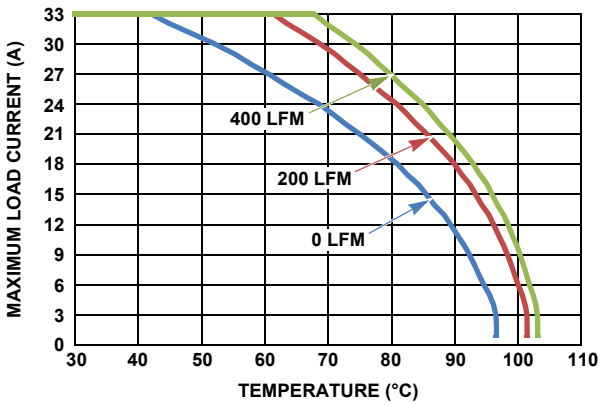


FIGURE 23. $12V_{IN}$ TO $2.5V_{OUT}$

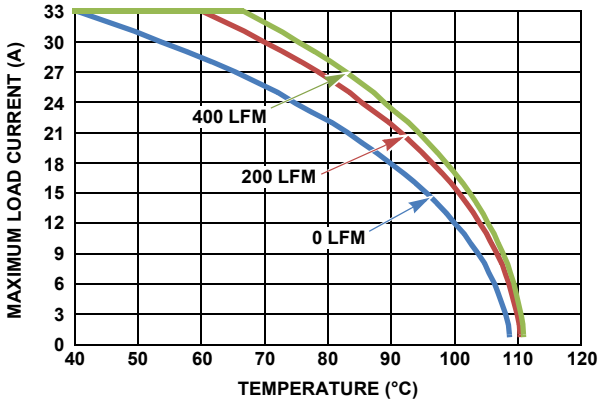


FIGURE 24. $5V_{IN}$ TO $3.3V_{OUT}$

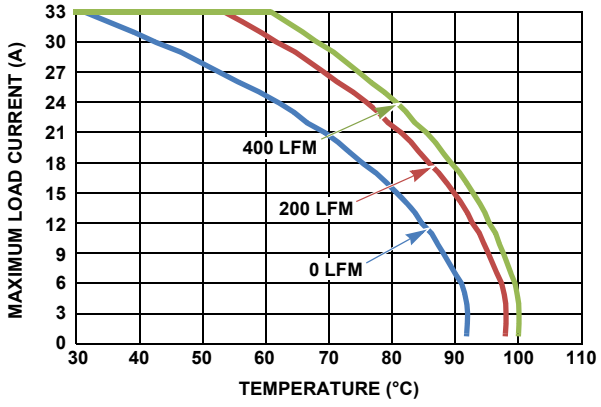


FIGURE 25. $12V_{IN}$ TO $3.3V_{OUT}$

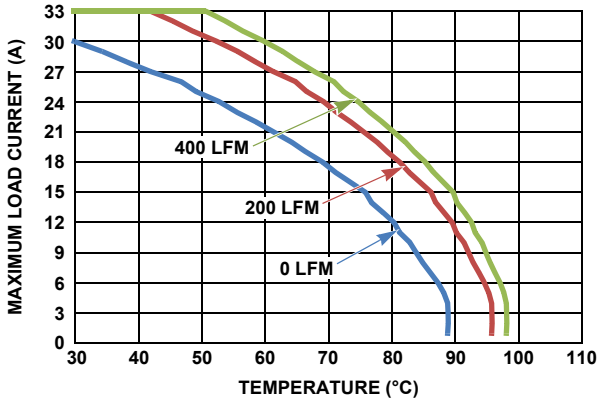
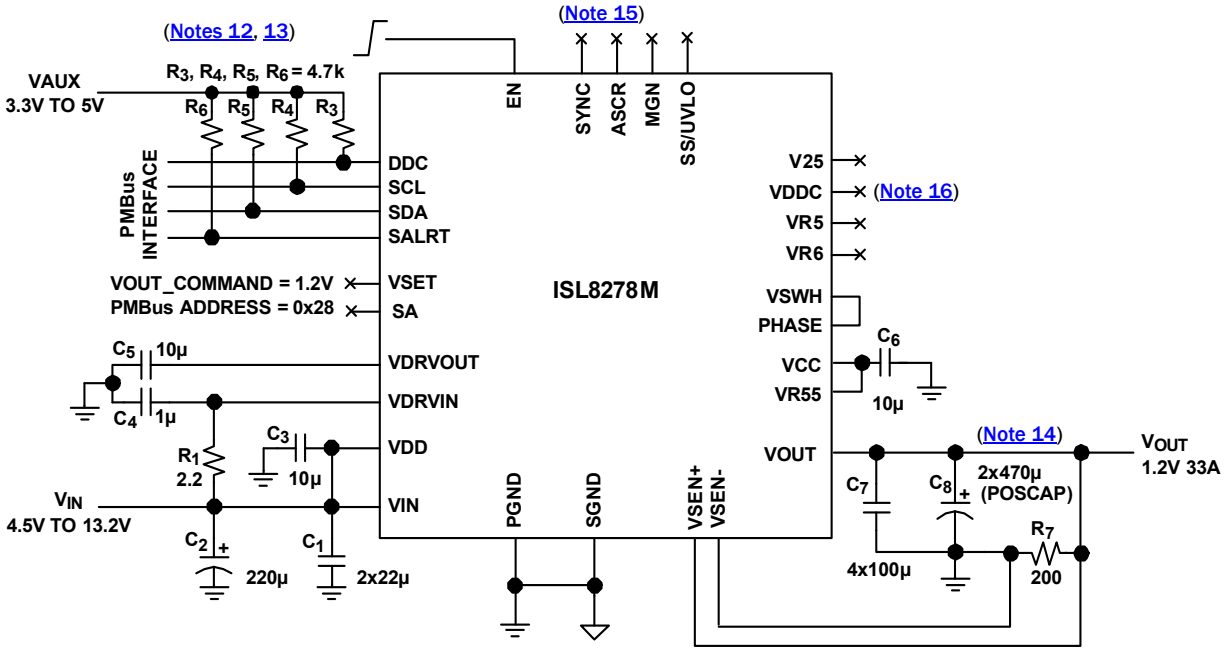


FIGURE 26. $12V_{IN}$ TO $5V_{OUT}$, 700kHz

Typical Application Circuit



NOTES:

12. R_4 and R_5 are not required if the PMBus host already has I^2C pull-up resistors.
13. Only one R_3 per DDC bus is required when DDC bus is shared with other modules.
14. R_7 is optional but recommended to sink possible ~100µA back-flow current from the V_{SEN+} pin. Back-flow current is present only when the module is in a disabled state with power still available at the VDD pin.
15. Unused pins (SYNC, ASCR, MGN, SS/UVLO) can be no connect.
16. Internal reference supply pins (V25, VDDC, VR5, VR6) do not need external capacitors and can be no connect. Refer to "PCB Layout Guidelines" on page 21 for more information.

FIGURE 27. TYPICAL SINGLE-PHASE APPLICATION CIRCUIT FOR 1.2V/33A OUTPUT

TABLE 2. ISL8278M DESIGN GUIDE MATRIX AND OUTPUT VOLTAGE RESPONSE

V_{IN}	V_{OUT}	C_{IN} (BULK) (Note 17)	C_{IN} (CERAMIC)	C_{OUT} (BULK)	C_{OUT} (CERAMIC)	ASCR GAIN (Note 18)	ASCR RESIDUAL (Note 18)	FREQUENCY	V_{OUT} DEVIATION (mV)	RECOVERY TIME (µS)	STEP LOAD (A) (Note 19)
5	0.8	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	140	35	16.5A
5	0.8	2x150µF	3x22µF	2x470µF	4x100µF	200	90	533	100	30	16.5A
5	0.9	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	130	40	16.5A
5	1	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	110	35	16.5A
5	1	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	80	20	16.5A
5	1.05	2x150µF	3x22µF	2x470µF	4x100µF	160	90	421	90	30	16.5A
5	1.1	2x150µF	3x22µF	2x470µF	4x100µF	200	90	471	90	25	16.5A
5	1.2	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	80	20	16.5A
5	1.3	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	80	25	16.5A
5	1.5	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	80	30	16.5A
5	1.8	2x150µF	3x22µF	2x470µF	3x100µF	250	90	615	80	50	16.5A
5	2.5	2x150µF	3x22µF	2x470µF	3x100µF	200	90	615	90	70	16.5A
5	3.3	2x150µF	3x22µF	2x470µF	3x100µF	200	90	615	90	90	16.5A
5	1.8	2x150µF	3x22µF	1x470µF	3x100µF	160	90	615	125	60	16.5A

TABLE 2. ISL8278M DESIGN GUIDE MATRIX AND OUTPUT VOLTAGE RESPONSE

5	2.5	2x150µF	3x22µF	1x470µF	3x100µF	160	90	615	120	70	16.5A
5	3.3	2x150µF	3x22µF	1x470µF	3x100µF	160	70	615	120	70	16.5A
12	0.8	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	140	35	16.5A
12	0.8	2x150µF	3x22µF	2x470µF	4x100µF	200	90	533	100	35	16.5A
12	0.9	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	130	32	16.5A
12	1	2x150µF	3x22µF	2x470µF	4x100µF	120	90	364	110	25	16.5A
12	1	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	85	20	16.5A
12	1.05	2x150µF	3x22µF	2x470µF	4x100µF	160	70	421	90	15	16.5A
12	1.1	2x150µF	3x22µF	2x470µF	4x100µF	160	90	471	95	25	16.5A
12	1.2	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	85	17	16.5A
12	1.3	2x150µF	3x22µF	2x470µF	4x100µF	250	90	533	85	17	16.5A
12	1.5	2x150µF	3x22µF	2x470µF	4x100µF	200	90	533	90	20	16.5A
12	1.8	2x150µF	3x22µF	2x470µF	3x100µF	250	90	615	90	20	16.5A
12	2.5	2x150µF	3x22µF	2x470µF	3x100µF	250	90	615	90	15	16.5A
12	3.3	2x150µF	3x22µF	2x470µF	3x100µF	250	90	615	90	20	16.5A
12	5	2x150µF	3x22µF	2x470µF	3x100µF	300	80	727	90	12	16.5A
12	1.8	2x150µF	3x22µF	1x470µF	3x100µF	160	90	615	160	20	16.5A
12	2.5	2x150µF	3x22µF	1x470µF	3x100µF	160	90	615	150	20	16.5A
12	3.3	2x150µF	3x22µF	1x470µF	3x100µF	160	90	615	160	20	16.5A
12	5	2x150µF	3x22µF	1x470µF	3x100µF	160	90	727	180	50	16.5A

NOTES:

17. C_{IN} bulk capacitor is optional only for energy buffer from the long input power supply cable.
18. ASCR gain and residual are selected to ensure that the phase margin is higher than 60° and gain margin is higher than 6dB at -40°C, +25°C, +85°C, and full load (33A).
19. Output voltage response is tested with load step slew rate higher than 20A/µs.

TABLE 3. RECOMMENDED I/O CAPACITOR IN Table 2

VENDORS	VALUE	PART NUMBER
Murata, Input Ceramic	47µF, 16V, 1210	GRM32ER61C476ME15L
Murata, Input Ceramic	22µF, 16V, 1210	GRM32ER61E226KE15L
Taiyo Yuden, Input Ceramic	47µF, 16V, 1210	EMK325BJ476MM-T
Taiyo Yuden, Input Ceramic	22µF, 25V, 1210	TMK325BJ226MM-T
Murata, Output Ceramic	100µF, 6.3V, 1210	GRM32ER60J107M
TDK, Output Ceramic	100µF, 6.3V, 1210	C3225X5R0J107M
AVX, Output Ceramic	100µF, 6.3V, 1210	12106D107MAT2A
Sanyo POSCAP, Input Bulk	150µF, 16V	16TQC150MYF
Sanyo POSCAP, Output Bulk	470µF, 4V	4TPE470MCL
Sanyo POSCAP, Output Bulk	470µF, 6.3V	6TPF470MAH

Functional Description

SMBus Communications

The ISL8278M provides an SMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ISL8278M can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The ISL8278M accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin be tied to SGND.

The SMBus device address is the only parameter that must be set by external pins. All other device parameters can be set with PMBus commands.

Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 5V provided that the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET pin is used to set the output voltage to levels as shown in Table 4. The R_{SET} resistor is placed between the VSET pin and SGND. A standard 1% resistor is recommend.

TABLE 4. OUTPUT VOLTAGE RESISTOR SETTINGS

V_{OUT} (V)	R_{SET} (kΩ)
0.60	10
0.65	11
0.70	12.1
0.75	13.3
0.80	14.7
0.85	16.2
0.90	17.8
0.95	19.6
1.00	21.5 or connect to SGND
1.05	23.7
1.10	26.1
1.15	28.7
1.20	31.6 or OPEN
1.25	34.8
1.30	38.3
1.40	42.2
1.50	46.4
1.60	51.1
1.70	56.2
1.80	61.9
1.90	68.1
2.00	75
2.10	82.5
2.20	90.9
2.30	100
2.50	110, or connect to V25
2.80	121
3.00	133
3.30	147
4.00	162
5.00	178

The output voltage can also be set to any value between 0.6V and 5V using a PMBus command VOUT_COMMAND.

By default, V_{OUT_MAX} is set 110% higher than V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 5.5V with PMBus Command VOUT_MAX.

Soft-Start Delay and Ramp Times

The ISL8278M follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. After this process is complete, the device is ready to accept commands through the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may want to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL8278M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp times can be programmed to custom values with PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay and ramp-down time for soft-stop/off can be programmed with PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” with the command

ON_OFF_CONFIG, such that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/UVLO pin can be used to program the soft-start/stop delay time and ramp time to some typical values as shown in Table 5.

TABLE 5. SOFT-START/STOP RESISTOR SETTINGS

DELAY TIME (ms)	RAMP TIME (ms)	R_{SET} (kΩ)
5	2	12.1, 26.1, 56.2, or connect to SGND
10	2	16.2, 34.8, 75
5	5	13.3, 28.7, 61.9, or OPEN
10	5	17.8, 38.3, 82.5
20	5	21.5, 46.4, 100
5	10	14.7, 31.6, 68.1
10	10	19.6, 42.2, 90.9, or connect to V25
20	10	23.7, 51.1, 110

Power-Good

The ISL8278M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the polarity of the pin can be changed with PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the ISL8278M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A PG delay can be programmed with PMBus command POWER_GOOD_DELAY.

Switching Frequency and PLL

The device's switching frequency is set from 296kHz to 1067kHz using the pin-strap method as shown in Table 6, or by using a PMBus command FREQUENCY_SWITCH. The ISL8278M incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source that is an external sync to other modules. Refer to "SYNC_CONFIG (E9h)" on page 46 for more information.

TABLE 6. SWITCHING FREQUENCY RESISTOR SETTINGS

f_{SW} (V)	R_{SET} (kΩ)
296	14.7 or connect to SGND
320	16.2
364	17.8
400	19.6
421	21.5
471	23.7
533	26.1 or OPEN
571	28.7
615	31.6
727	34.8
800	38.3
842	42.2
889	46.4
1067	51.1 or connect to V25

Loop Compensation

The module loop response is programmable through PMBus command ASCR_CONFIG or by using the pin-strap method (ASCR pin) according to Table 7. The ISL8278M uses the ChargeMode control algorithm that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

TABLE 7. ASCR RESISTOR SETTINGS

ASCR GAIN	ASCR RESIDUAL	R_{SET} (kΩ)
120	90	10
160	90	11 or connect to SGND
200	90	12.1
250	90	13.3 or OPEN
300	90	14.7
350	90	16.2
400	90	17.8
500	90	19.6
600	90	21.5
120	80	23.7
160	80	26.1
200	80	28.7
250	80	31.6
300	80	34.8
350	80	38.3
400	80	42.2
80	70	46.4
120	70	51.1
160	70	56.2
200	70	61.9

TABLE 7. ASCR RESISTOR SETTINGS (Continued)

250	70	68.1
300	70	75
120	100	82.5
160	100	90.9
200	100	100
250	100	110, or Connect to V25
300	100	121
350	100	133
400	100	147
500	100	162
600	100	178

Input Undervoltage Lockout (UVLO)

The Input Undervoltage Lockout (UVLO) prevents the ISL8278M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V using the pin-strap method as shown in Table 8, or by using a PMBus command VIN_UV_FAULT_LIMIT.

Fault response to an input undervoltage fault can be programmed with PMBus command VIN_UV_FAULT_RESPONSE.

TABLE 8. UVLO RESISTOR SETTINGS

UVLO (V)	R_{UVLO} (kΩ)
4.5	12.1, 13.3, 14.7, 16.2, 17.8, 19.6, 21.5, 23.7, OPEN, connect to V25 and SGND
4.3	26.1
4.59	28.7
5.06	31.6
5.57	34.8
6.13	38.3
6.75	42.2
7.42	46.4
8.18	51.1
10.8	56.2
10.8	61.9
10.8	68.1
10.8	75
10.8	82.5
10.8	90.9
10.8	100

SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 9 lists the available module addresses.

TABLE 9. SMBus ADDRESS RESISTOR SELECTION

R_{SA} (kΩ)	SMBus ADDRESS
10	19h
11	1Ah
12.1	1Bh
13.3	1Ch
14.7	1Dh
16.2	1Eh
17.8	1Fh
19.6	20h
21.5	21h
23.7	22h
26.1	23h
28.7	24h
31.6	25h
34.8 or connect to SGND	26h
38.3	27h
42.2 or OPEN	28h
46.4	29h
51.1	2Ah
56.2	2Bh
61.9	2Ch
68.1	2Dh
75	2Eh
82.5	2Fh
90.9	30h
100	31h

Output Overvoltage Protection

The ISL8278M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the V_{SEN+} and V_{SEN-} pins) to a threshold set to 15% higher than the target output voltage (the default setting). Fault threshold can be programmed to a desired level with PMBus command VOUT_OV_FAULT_LIMIT. If the V_{SEN+} voltage exceeds this threshold, the module will initiate an immediate shutdown without retry. Retry settings can be programmed with PMBus command VOUT_OV_FAULT_RESPONSE.

Internal to the module, two 100Ω resistors are populated from VOUT to V_{SEN+} and SGND to V_{SEN-} to protect from overvoltage conditions in case of open at VSENSE pins and differential remote sense traces due to assembly error. As long as the differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not sacrificed.

Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ISL8278M provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage. However, the total time elapsed from when the delay period expires and when the output reaches its target value will match the preconfigured ramp time (see Figure 28).

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

After the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage, and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition. The device then responds based on the output overvoltage fault response setting programmed with PMBus command VOUT_OV_FAULT_RESPONSE.

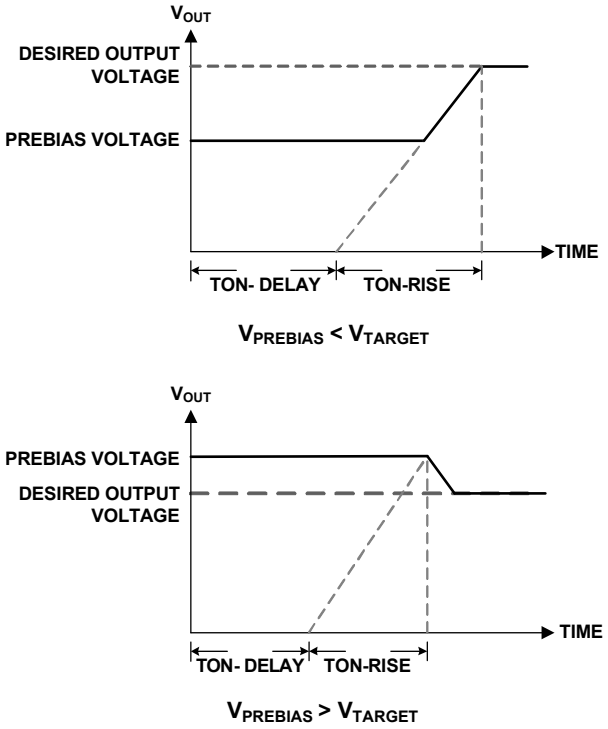


FIGURE 28. OUTPUT RESPONSES TO PREBIAS VOLTAGES

Output Overcurrent Protection

The ISL8278M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The average output overcurrent fault threshold can be programmed with PMBus command IOUT_OC_FAULT_LIMIT. The module automatically programs the peak inductor current fault threshold by reading the real-time input voltage, switching frequency, and VOUT_COMMAND to calculate inductor ripple current. When the peak inductor current crosses the peak inductor current fault threshold for five successive cycle modules, it will initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown without retry. Retry settings can be programmed with PMBus command MFR_IOUT_OC_FAULT_RESPONSE.

Thermal Overload Protection

The ISL8278M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but can be changed with PMBus command OT_FAULT_LIMIT.

The default response from an over-temperature fault is an immediate shutdown without retry. Retry settings can be programmed with PMBus command OT_FAULT_RESPONSE.

If the user has configured the module to retry, the controller waits the preset delay period (if configured to do so) and then checks the module temperature. If the temperature has dropped below a threshold that is approximately 15°C lower than the selected temperature fault limit, the controller attempts to restart. If the temperature still exceeds the fault limit, the controller waits the preset delay period and retries again.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil digital power modules and digital controllers. This dedicated bus provides the communication channel between devices for features such as sequencing and fault spreading. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus to ensure the rise time as shown in Equation 1:

$$\text{Rise Time} = R_{PU} * C_{LOAD} \approx 1\mu s \quad \text{(EQ. 1)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor can be tied to an external 3.3V or 5V supply as long as this voltage is present before or during device power-up. In principle, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well-matched to the total load capacitance.

Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device can also be set to any value between 0° and 360° in 22.5° increments with PMBus command INTERLEAVE.

Output Sequencing

A group of Digital-DC modules or devices can be configured to power-up in a predetermined sequence. This feature is especially useful when powering advanced processors (FPGAs and ASICs that require one supply to reach its operating voltage) before another supply reaches its operating voltage, to avoid latch-up. Multi-device sequencing can be achieved by configuring each device with PMBus command SEQUENCE. Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain, as well as the device that follows in the sequencing chain.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Fault Spreading

Digital DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group with PMBus command DDC_GROUP. When a non-destructive fault occurs and the device is configured to shutdown on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shutdown simultaneously, if configured to do so, and attempt to restart in their prescribed order.

Monitoring Through SMBus

A system controller can monitor a wide variety of different ISL8278M system parameters with PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_EXTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQEUNCY
- MFR_READ_VMON

Snapshot Parameter Capture

The ISL8278M offers a special feature to capture parametric data and some fault status following a fault. A detailed description is provided in "PMBus Commands Description" on page 28 under PMBus command SNAPSHOT and SNAPSHOT_CONTROL.

Nonvolatile Memory

The ISL8278M has internal nonvolatile memory to store user configurations. Integrated security measures ensure that users can only restore the module to a level that has been made available to them. During the initialization process, the ISL8278M checks for stored values contained in its internal nonvolatile memory.

Modules are shipped with factory default configurations. Most settings can be overwritten with PMBus Commands and can be stored in nonvolatile memory with the PMBus command STORE_USER_ALL.

PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

- For V_{DD} > 6V, the recommended PCB layout is shown in Figure 29. Leave V25, VDDC, VR5, and VR6 as “No Connect”.
- For 5.5V ≤ V_{DD} ≤ 6V, connect VDDC pin to VR6 pin. For 4.5 ≤ V_{DD} < 5.5V, connect VDDC pin to VR6 and VR5 pin. An RC filter is required at the input of V_{DRVIN} pin if input supply is shared with VIN pin.
- Establish a separate SGND plane and PGND plane, then connect SGND to the PGND plane as shown in Figure 30 in the middle layer. For making connections between SGND/PGND on the top layer and other layers, use multiple vias for each pin to connect to the inner SGND/PGND layer. Do not connect SGND directly to PGND on a top layer. Connecting SGND directly to PGND without establishing an SGND plane will bypass the decoupling capacitor at internal reference supplies, making the controller susceptible to noise.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND and bypass capacitors between VDD and the ground plane, as close to the module as possible to minimize high frequency noise.
- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. Extra ceramic capacitors at VIN and VOUT can be placed on the bottom layer under VIN and VOUT pads when multiple vias are used for connecting copper pads on top and bottom layers.
- Connect differential remote-sensing traces to the regulation point to achieve a tight output voltage regulation. Route a trace from V_{SEN-} and V_{SEN+} to the point-of-load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENSE signal near VSWH pads.
- For noise sensitive applications, it is recommended that the user connect the VSWH pads only on the top layer only (however, thermal performance gets sacrificed). External airflow might be required to keep module heat at desired level. For applications where switching noise is less critical, an excellent thermal performance can be achieved in the ISL8278M module by increasing copper mass attached to VSWH pad. To increase copper mass on the VSWH node, create copper islands in the middle and bottom layers under VSWH the pad, and connect them to the top layer with multiple vias. Make sure to shield those copper islands with a PGND layer to avoid any interference to noise sensitive signals.

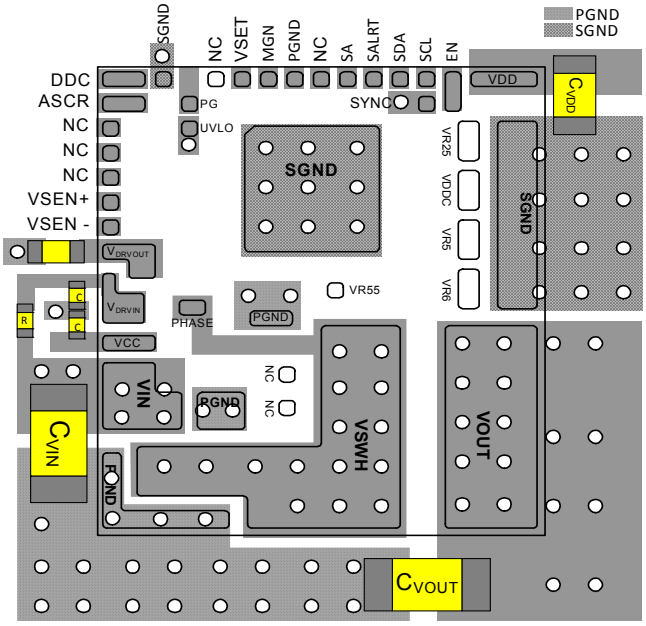


FIGURE 29. RECOMMENDED LAYOUT - TOP PCB LAYER

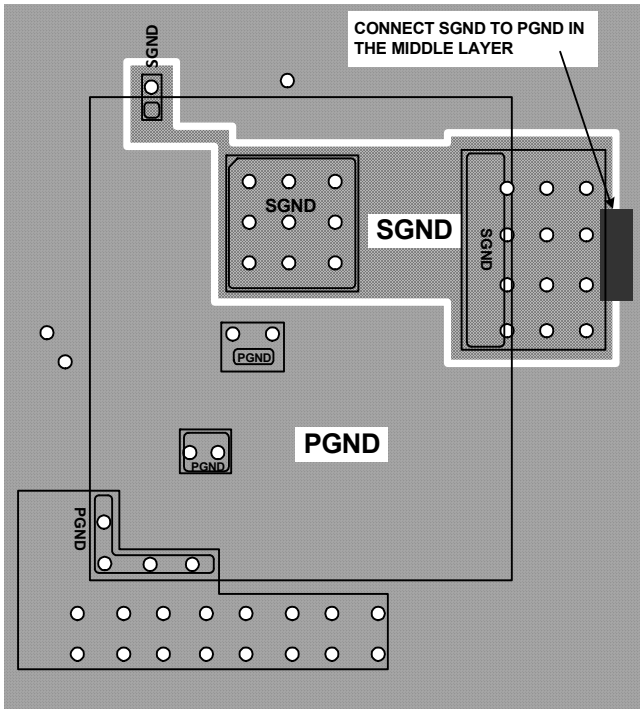


FIGURE 30. RECOMMENDED LAYOUT - CONNECT SGND TO PGND IN THE MIDDLE PCB LAYER AFTER ESTABLISHING SEPARATE SGND AND PGND

Thermal Considerations

Experimental power loss curves, along with θ_{JA} from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margins should be considered.

Package Description

The structure of the ISL8278M belongs to the High Density Array (HDA) no-lead package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8278M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8278M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multi-component assembly is overmolded with polymer mold compound to protect these devices.

The package outline, a typical PCB land pattern design, and a typical stencil opening edge position are shown in the Package Outline Drawing section starting on page 50. The module has a small size of 17mmx19mmx3.6mm. Figure 31 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to their application.

PCB Layout Pattern Design

The bottom of the ISL8278M is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB land pattern is shown in the "Package Outline Drawing" section starting on page page 50.

The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and that your board design rules will allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints.

The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the "Package Outline Drawing" section starting on page page 50.

The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

Reflow Parameters

Due to the low mount height of the HDA, a "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, thus it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 31 is provided as a guideline, to be customized for varying manufacturing practices and applications.

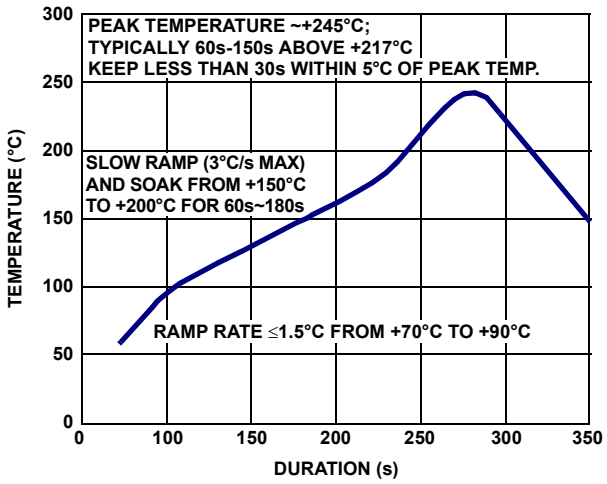


FIGURE 31. TYPICAL REFLOW PROFILE

PMBus Command Summary

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
01h	OPERATION	Sets Enable, Disable, and V_{OUT} Margin modes.	R/W BYTE	BIT			28
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF.	R/W BYTE	BIT	17h	Hardware Enable, Immediate Off	28
03h	CLEAR_FAULTS	Clears fault indications.	SEND BYTE				28
15h	STORE_USER_ALL	Stores all PMBus values written since last restore at user level.	SEND BYTE				28
16h	RESTORE_USER_ALL	Restores PMBus settings that were stored using STORE_USER_ALL.	SEND BYTE				29
20h	VOUT_MODE	Preset to defined data format of V_{OUT} commands.	READ BYTE	BIT	13h	Linear Mode, Exponent = -13	29
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W WORD	L16u		Pin-strap	29
23h	VOUT_CAL_OFFSET	Applies a fixed offset voltage to the VOUT_COMMAND.	R/W WORD	L16s	0000h	0V	29
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W WORD	L16u		1.1 * V_{OUT} Pin-strap	29
25h	VOUT_MARGIN_HIGH	Sets the value of the V_{OUT} during a margin high.	R/W WORD	L16u		1.05 * V_{OUT} Pin-strap	30
26h	VOUT_MARGIN_LOW	Sets the value of the V_{OUT} during a margin low.	R/W WORD	L16u		0.95 * V_{OUT} Pin-strap	30
27h	VOUT_TRANSITION_RATE	Sets the transition rate during margin or other change of V_{OUT}.	R/W WORD	L11	BA00h	1V/ms	30
28h	VOUT_DROOP	Sets the loadline (V/I Slope) resistance for the rail.	R/W WORD	L11	0000h	0mV/A	30
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W WORD	L11		Pin-strap	30
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W WORD	BIT		Set based on PMBus Address	31
38h	IOUT_CAL_GAIN	Sense resistance for inductor DCR current sensing.	R/W WORD	L11	B2AEh	0.67mΩ	31
39h	IOUT_CAL_OFFSET	Sets the current-sense offset.	R/W WORD	L11	0000h	0A	31
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W WORD	L16u		1.15 * V_{OUT} Pin-strap	31
41h	VOUT_OV_FAULT_RESPONSE	Configures the V_{OUT} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	31
42h	VOUT_OV_WARN_LIMIT	Sets the V_{OUT} overvoltage warn threshold.	R/W WORD	L16u		1.1 * V_{OUT} Pin-strap	32
43h	VOUT_UV_WARN_LIMIT	Sets the V_{OUT} undervoltage warn threshold.	R/W WORD	L16u		0.9 * V_{OUT} Pin-strap	32
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W WORD	L16u		0.85 * V_{OUT} Pin-strap	32
45h	VOUT_UV_FAULT_RESPONSE	Configures the V_{OUT} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	32
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W WORD	L11	E280h	40A	32

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W WORD	L11	E57Fh	-40A	33
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W WORD	L11	EBE8h	+125°C	33
50h	OT_FAULT_RESPONSE	Configures the over -temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	33
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W WORD	L11	EB70h	+110°C	33
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W WORD	L11	DC40h	-30°C	33
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W WORD	L11	E530h	-45°C	34
54h	UT_FAULT_RESPONSE	Configures the under-temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	34
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W WORD	L11	D3A0h	14.5V	34
56h	VIN_OV_FAULT_RESPONSE	Configures the V_{IN} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	34
57h	VIN_OV_WARN_LIMIT	Sets the input overvoltage warning limit.	R/W WORD	L11	D343h	13.05V	35
58h	VIN_UV_WARN_LIMIT	Sets the input undervoltage warning limit.	R/W WORD	L11		1.10 * V_{IN} UV Fault Limit	35
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W WORD	L11		Pin-strap	35
5Ah	VIN_UV_FAULT_RESPONSE	Configures the V_{IN} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	35
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-Good indication.	R/W WORD	L16u		0.9 * V_{OUT} Pin-strap	35
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W WORD	L11		Pin-strap	36
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W WORD	L11		Pin-strap	36
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W WORD	L11		Pin-strap	36
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W WORD	L11		Pin-strap	36
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	READ BYTE	BIT	00h	No Faults	36
79h	STATUS_WORD	Returns information with a summary of the units's fault condition.	READ WORD	BIT	0000h	No Faults	37
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	READ BYTE	BIT	00h	No Faults	37
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	READ BYTE	BIT	00h	No Faults	38
7Ch	STATUS_INPUT	Returns specific status specific to the input.	READ BYTE	BIT	00h	No Faults	38
7Dh	STATUS_TEMPERATURE	Returns the temperature specific status.	READ BYTE	BIT	00h	No Faults	38

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
7Eh	STATUS_CML	Returns the Communication, Logic, and Memory specific status.	READ BYTE	BIT	00h	No Faults	39
80h	STATUS_MFR_SPECIFIC	Returns the VMON and External Sync clock specific status.	READ BYTE	BIT	00h	No Faults	39
88h	READ_VIN	Returns the input voltage reading.	READ WORD	L11			39
8Bh	READ_VOUT	Returns the output voltage reading.	READ WORD	L16u			39
8Ch	READ_IOUT	Returns the output current reading.	READ WORD	L11			40
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	READ WORD	L11			40
8Eh	READ_EXTERNAL_TEMP	Returns the temperature reading from external monitor source.	READ WORD	L11			40
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	READ WORD	L11			40
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	READ WORD	L11			40
99h	MFR_ID	Sets a user defined identification.	R/W BLOCK	ASCII		Null	40
9Ah	MFR_MODEL	Sets a user defined model.	R/W BLOCK	ASCII		Null	41
9Bh	MFR_REVISION	Sets a user defined revision.	R/W BLOCK	ASCII		Null	41
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W BLOCK	ASCII		Null	41
9Dh	MFR_DATE	Sets a user defined date.	R/W BLOCK	ASCII		Null	41
9Eh	MFR_SERIAL	Sets a user define d serialized identifier.	R/W BLOCK	ASCII		Null	41
A8h	LEGACY_FAULT_GROUP	Broadcast faults when mixed with old generation modules	R/W BLOCK	BIT	00000000h		42
B0h	USER_DATA_00	Sets a user defined data.	R/W BLOCK	ASCII		Null	42
D0h	ISENSE_CONFIG	Configures ISENSE related features.	R/W BYTE	BIT	05h	256ns Blanking Time, Mid Range	42
D1h	USER_CONFIG	Configures several user-level features.	R/W BYTE	BIT	00h	Open-Drain PG, XTEMP Disabled	43
D3h	DDC_CONFIG	Configures the DDC bus.	R/W BYTE	BIT	00h	Set based on PMBus Address	43
D4h	POWER_GOOD_DELAY	Sets the delay between V_{OUT} > PG threshold and asserting the PG pin.	R/W WORD	L11	CA00h	4ms	43
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W BLOCK	CUS		Pin-strap	44
E0h	SEQUENCE	Identifies the Rail DDC ID to perform multi-rail sequencing.	R/W WORD	BIT	0000h	Prequel and Sequel Disabled	44
E2h	DDC_GROUP	Sets rail DDC IDs to obey faults and margining spreading information.	R/W BLOCK	BIT	000000h	Broadcast Disabled	45
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	READ BLOCK	ASCII		Reads Device Version	45
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W BYTE	BIT	80h	Disable and No Retry	45

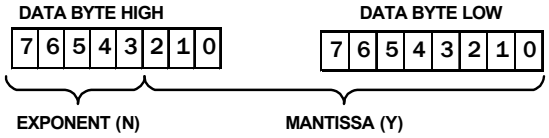
PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W BYTE	BIT	80h	Disable and No Retry	46
E9h	SYNC_CONFIG	Configures the Sync pin.	R/W BYTE	BIT	00h		46
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	READ BLOCK	BIT			47
EBh	BLANK_PARAMS	Returns recently changed parameter values.	READ BLOCK	BIT	FF...FFh		47
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	W BYTE	BIT			47
F4h	RESTORE_FACTORY	Restores device to the factory default values.	WRITE ONLY				48
F5h	MFR_VMON_OV_FAULT_LIMIT	Returns the VMON overvoltage threshold.	READ WORD	L11	CB00h	6V	48
F6h	MFR_VMON_UV_FAULT_LIMIT	Returns the VMON undervoltage threshold.	READ WORD	L11	CA00h	4V	48
F7h	MFR_READ_VMON	Returns the VMON voltage reading. VMON is used to monitor VDRVOUT (Pin 8) voltage through an internal 16:1 resistor divider.	READ WORD	L11			48
F8h	VMON_OV_FAULT_RESPONSE	Returns the VMON overvoltage response.	READ BYTE	BIT	80h	Disable and No Retry	48
F9h	VMON_UV_FAULT_RESPONSE	Returns the VMON undervoltage response.	READ BYTE	BIT	80h	Disable and No Retry	48

PMBus Data Formats

Linear-11 (L11)

The L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent a real world decimal value (X).



The relation between real world decimal value (X), N, and Y is: $X = Y \bullet 2^{N}$

Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \bullet 2^{-13}$

Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hardcoded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X).
The relation between real world decimal value (X), N, and Y is: $X = Y \bullet 2^{-13}$

Bit Field (BIT)
A breakdown of the Bit Field format is provided in PMBus on "PMBus Commands Description" on page 28.

Custom (CUS)
A breakdown of the custom data format is provided in PMBus "PMBus Commands Description" on page 28. A combination of Bit Field and integer are a common type of Custom data format.

ASCII (ASC)
A variable length string of text characters that uses the ASCII data format.

PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL, and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable.

PMBus Commands Description

OPERATION (01h)

Definition: Sets Enable, Disable, and V_{OUT} Margin settings. Data values of OPERATION that force margin high or low only take effect when the MGN pin is left open (i.e., in the NOMINAL margin state).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

SETTINGS	ACTIONS
04h	Immediate off (no sequencing)
44h	Soft off (with sequencing)
84h	On - Nominal.
94h	On - Margin low
A4h	On - Margin high

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 17h (Device starts from ENABLE pin with immediate off)

Units: N/A

SETTINGS	ACTIONS
00h	Device starts any time power is present regardless of ENABLE pin or OPERATION command states
16h	Device starts from ENABLE pin with soft off
17h	Device starts from ENABLE pin with immediate off
1Ah	Device starts from OPERATION command

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Send only

Default Value: N/A

Units: N/A

Reference: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send only

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send only

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings. Fixed with linear mode with default exponent (N) = -13

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 13h (Linear Mode, N = -13)

Units: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than either VOUT_MAX or 110% of the pin-strap V_{OUT} setting.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W

Default Value: 0000h

Units: Volts

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. Default value can be changed through PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10 x VOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to 6V

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W word

Default value: 1.05 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default value: 0.95 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default value: BA00h (1.0V/ms)

Units: V/ms

Range: 0.1V/ms to 4V/ms

VOUT_DROOP (28h)

Definition: Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with Adaptive Voltage Positioning schemes.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default value: 0000h (0mV/A)

Units: mV/A

Range: 0mV/A to 40mV/A

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command through PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 300kHz to 1066MHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A value of 0 for the number in group field is interpreted as 16, to allow for phase spreading groups of up to 16 devices.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Set based on PMBus address

Units: kHz

BITS	PURPOSE	VALUE	DESCRIPTION
15:2	Reserved	0	Reserved
11:8	Group Number	0 to 15	Sets a number to a group of interleaved rails.
7:4	Number in Group	0 to 15	Sets the number of rails in the group A value of 0 is interpreted as 16.
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: B2AEh (0.67mΩ)

Units: mΩ

IOUT_CAL_OFFSET (39h)

Definition: Used to null out any offsets in the output current-sensing circuit, and to compensate for delayed measurements of current ramp due to I_{SENSE} blanking time.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 0000h (0A)

Units: A

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

VOUT_OV_WARN_LIMIT (42h)

Definition: Sets the V_{OUT} overvoltage wring threshold. Power-good signal is pulled low when output voltage goes higher than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.1 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_WARN_LIMIT (43h)

Definition: Sets the V_{OUT} undervoltage warning threshold. Power-good signal is pulled low when output voltage goes lower than this threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. Device will automatically calculate peak inductor overcurrent fault limit.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E280h (40A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} average undercurrent fault threshold. Device will automatically calculate valley inductor undercurrent fault limit.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E57Fh (-40A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EBE8h (+125˚C)

Units: Celsius

Range: 0°C to +175°C

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Fault Value: 80h (Disable and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB70h (+110°C)

Units: Celsius

Range: 0°C to +175°C

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: DC40h (-30°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above UT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0h (14.5V)

Units: V

Range: 0V to 16V

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the VIN overvoltage warning threshold as defined by the table below. In response to the OV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Protectable: Yes

Default Value: D343h (13.05V)

Units: V

Range: 0V to 16V

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the VIN undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: 1.1 x VIN_UV_FAULT_LIMIT pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x VOUT_COMMAND pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: ms
Range: 0ms to 500ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: ms
Range: 0ms to 200ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: s
Range: 0s to 500s

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W
Default Value: Pin-strap setting
Units: ms
Range: 0 to 200ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.
Data Length in Bytes: 1
Data Format: BIT
Type: Read only
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read only

Default Value: 0000h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT/POUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	FANS	A fan or airflow fault or warning has occurred.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any Communications, Logic, and/or Memory errors.
Data Length in Bytes: 1
Data Format: BIT
Type: Read only
Default Value: 00h
Units: N/A

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4:2	Not used
1	A PMBus command tried to write to a read only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.
Data Length in Bytes: 1
Data Format: BIT
Type: Read only
Default Value: 00h
Units: N/A

BIT NUMBER	FIELD NAME	MEANING
7:6	Reserved	
5	VMON UV Warning	The voltage on the VDRVOUT pin has dropped below 4.4V.
4	VMON OV Warning	The voltage on the VDRVOUT pin has risen above 5.5V.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Reserved	
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Data Length in Bytes: 2
Data Format: L16u
Type: Read only
Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Default Value: N/A
Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: °C

READ_EXTERNAL_TEMP (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP pins.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.
Data Length in Bytes: 2
Data Format: L11
Type: Read only
Units: kHz

MFR_ID (99h)

Definition: Sets user defined identification. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.
Data Length in Bytes: User defined
Data Format: ASCII
Type: Block R/W
Default Value: null
Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

Reference: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

LEGACY_FAULT_GROUP (A8h)

Definition: This command is used only when the power system is created by mixing the ISL8278M module with old generation digital modules (ZL9101M, ZL9117M, ZL9006M, ZL9010M) to power various rails. This command provides an ability to power down the system by broadcast faults between old and new generation digital modules.

New generation modules use group ID to broadcast faults between each other. Refer to DDC_GROUP(E2h) command. Old generation modules use rail ID to broadcast fault. When new and old modules are mixed, ISL8278M can use GROUP-ID (new generation module) and/or RAIL-ID (old generation module) to execute shutdown as response to fault to selected GROUP_ID or RAIL-ID. A module can listen to multiple RAIL-IDs by writing 1 to a bit location representing RAIL-ID of old generation modules.

NOTE: Bit-5 in DDC_GROUP command should be programmed 1 to activate fault broadcast.

Data length in Bytes: 4

Data Format: BIT

Type: R/W Block

Default Value: 00000000h

Units: N/A

BIT	DESCRIPTION	BIT	DESCRIPTION	BIT	DESCRIPTION	BIT	DESCRIPTION
31	Listen to Rail-31	23	Listen to Rail-23	15	Listen to Rail-15	7	Listen to Rail-7
30	Listen to Rail-30	22	Listen to Rail-22	14	Listen to Rail-14	6	Listen to Rail-6
29	Listen to Rail-29	21	Listen to Rail-21	13	Listen to Rail-13	5	Listen to Rail-5
28	Listen to Rail-28	20	Listen to Rail-20	12	Listen to Rail-12	4	Listen to Rail-4
27	Listen to Rail-27	19	Listen to Rail-19	11	Listen to Rail-11	3	Listen to Rail-3
26	Listen to Rail-26	18	Listen to Rail-18	10	Listen to Rail-10	2	Listen to Rail-2
25	Listen to Rail-25	17	Listen to Rail-17	9	Listen to Rail-9	1	Listen to Rail-1
24	Listen to Rail-24	16	Listen to Rail-16	8	Listen to Rail-8	0	Listen to Rail-0

USER_DATA_00 (B0h)

Definition: Sets a user defined data. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command, then perform a STORE/RESTORE.

Data Length in Bytes: User defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W byte

Default Value: 05h

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7:4	Reserved	000		
3:2	Current Sense Blanking Time	00	192ns	Sets the blanking time current sense blanking time.
		01	256ns	
		10	412ns	
		11	640ns	
1:0	Current Sense Range	00	Low Range	±25mV
		01	Mid Range	±35mV
		10	HIgh Range	±50mV
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features. This command overrides the CONFIG pin settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W byte

Default Value: 00h

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7:5	Reserved	0		Reserved
4:3	Ramp-Up and Ramp-Down Minimum Duty Cycle	00	0.39%	Sets the minimum duty-cycle during start-up and shutdown ramp. Must be enabled with Bit 10.
		01	0.78%	
		10	1.17%	
		11	1.56%	
2	Minimum Duty Cycle Control	0	Disable	Control for minimum duty cycle.
		1	Enable	
1	Power-Good Pin Configuration	0	Open Drain	0 = PG is open-drain output. 1 = PG is push-pull output.
		1	Push-Pull	
0	XTEMP Enable	0	Disable	Enable external temperature monitoring.
		1	Enable	

DDC_CONFIG (D3h)

Definition: Configures DDC addressing.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 00h

Units: N/A

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7:5	Reserved	00	Reserved	Reserved
4:0	Rail ID	0 to 31 (00 to 1Fh)	0	Configures DDC address

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: CA00h (4ms)

Units: ms

Range: 0s to 5s

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

BIT	PURPOSE	DATA FORMAT	VALUE	DESCRIPTION
31:25	Unused		0000000h	Unused
24	ASCR Enable	BIT	1	Enable
			0	Disable
23:16	ASCR Residual Setting	Integer		
15:0	ASCR Gain Setting	Integer		

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multi-rail sequencing. The device will enable its output when its EN or OPERATION enable states, as defined by ON_OFF_CONFIG, are set and the prequel device has issued a power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus.

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 0000h (Prequel and Sequel disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8.
14:13	Reserved	0	Reserved	Reserved
12:8	Prequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0.
6:5	Reserved	0	Reserved	Reserved
4:0	Sequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the sequel rail.

DDC_GROUP (E2h)

Definition: Configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable.

Data Length in Bytes: 3

Data Format: BIT

Type: R/W

Default Value: 000000h (Ignore BROADCAST VOUT_COMMAND and OPERATION, Sequence shutdown on POWER_FAIL event)

BITS	PURPOSE	VALUE	DESCRIPTION
23:22	Reserved	0	Reserved
21	BROADCAST_VOUT_COMMAND Response	1	Responds to BROADCAST_VOUT_COMMAND with same Group ID.
		0	Ignores BROADCAST_VOUT_COMMAND.
20:16	BROADCAST_VOUT_COMMAND Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_VOUT_COMMAND events.
15:14	Reserved	0	Reserved
13	BROADCAST_OPERATION Response	1	Responds to BROADCAST_OPERATION with same Group ID.
		0	Ignores BROADCAST_OPERATION.
12:8	BROADCAST_OPERATION Group ID	0-31d	Group ID sent as data for broadcast BROADCAST_OPERATION events.
7:6	Reserved	0	Reserved
5	POWER_FAIL Response	1	Responds to POWER_FAIL events with same Group ID by shutting down immediately.
		0	Responds to POWER_FAIL events with same Group ID with sequenced shutdown.
4:0	POWER_FAIL group ID	0-31d	Group ID sent as data for broadcast POWER_FAIL events.

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASCII

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable, and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 80h (Disable and no retry)

Units: N/A

SETTINGS	ACTIONS
80h	Disable with no retry.
BFh	Disable and continuous retry with 70ms delay.

SYNC_CONFIG (E9h)

Definition: Sets options for SYNC output configurations.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 00h

SETTINGS	ACTIONS
00h	Use Internal clock. Clock frequency is set by pin-strap or PMBus command.
02h	Use internal clock and output internal clock.
04h	Use external clock.

SNAPSHOT (EAh)

Definition: A 32-byte readback of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, the most recently updated values are stored to the flash memory. When SNAPSHOT STATUS byte 22 is set stored, the device will no longer automatically capture parametric and status values following a fault until stored data are erased. Use the SNAPSHOT_CONTROL command to erase stored data and clear the status bit before the next ramp up. Data erased is not allowed when the module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

BYTE NUMBER	VALUE	PMBUS COMMAND	FORMAT
31:23	Reserved	Reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	N/A	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	External Temperature	READ_EXTERNAL_TEMP (8Eh)	L11
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Highest Measured Output Current	N/A	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string indicating which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A “1” indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16

Data Format: BIT

Type: Block Read

Default Value: FF...FFh

SNAPSHOT_CONTROL (F3h)

Definition: Erases parametric and status values stored at SNAPSHOT, flash memory location.

Data Length in Bytes: 1

Data Format: Bit field

Type: W byte

VALUE	DESCRIPTION
03h	Erase parametric and status values stored in SNAPSHOT.

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VMON OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CB00h (6V)

Units: V

Range: 4V to 6V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VMON UV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CA00h (4V)

Units: V

Range: 4V to 6V

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: V

Range: 4V to 6V

VMON_OV_FAULT_RESPONSE (F8h)

Definition: Reads the VMON OV fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 80h (Disable and no retry)

Units: N/A

VMON_UV_FAULT_RESPONSE (F9h)

Definition: Reads the VMON UV fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 80h (Disable and no retry)

Units: N/A

Datasheet Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 17, 2017	FN8924.1	Updated Figures 10 through 15. Updated Table 2 on page 14 with new values. In Table 5 on page 17, changed the R_{SET} for the 5 entry to 13.3, 28.7, 61.9, or OPEN. Updated Table 7 on page 17 with new values. In Table 8 on page 18, changed the UVLO value for the last seven entries to 10.8 Changed the type for “DEVICE_ID (E4h)” on page 45 from ASC to ASCII. Changed the range for “VOUT_MAX (24h)” on page 29 from “0V to 4V” to “0V to 6V”. Updated the descriptions for bits 4 and 5 in “STATUS_MFR_SPECIFIC (80h)” on page 39. Changed the default value for “SYNC_CONFIG (E9h)” on page 46 from 0000h to 00h. For “Firmware Revision History” on page 49, added firmware version ISL8278-0-G0100. In “Monitoring Through SMBus” on page 20, changed “READ_VMON” to “MFR_READ_VMON”. In “SNAPSHOT_CONTROL (F3h)” on page 47, changed “R/W Byte” to “W Byte”.
Feb 28, 2017	FN8924.0	Initial release

Firmware Revision History

FIRMWARE REVISION CODE	CHANGE DESCRIPTION	NOTE
ISL8278-0-G0100	Initial release	

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit: www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

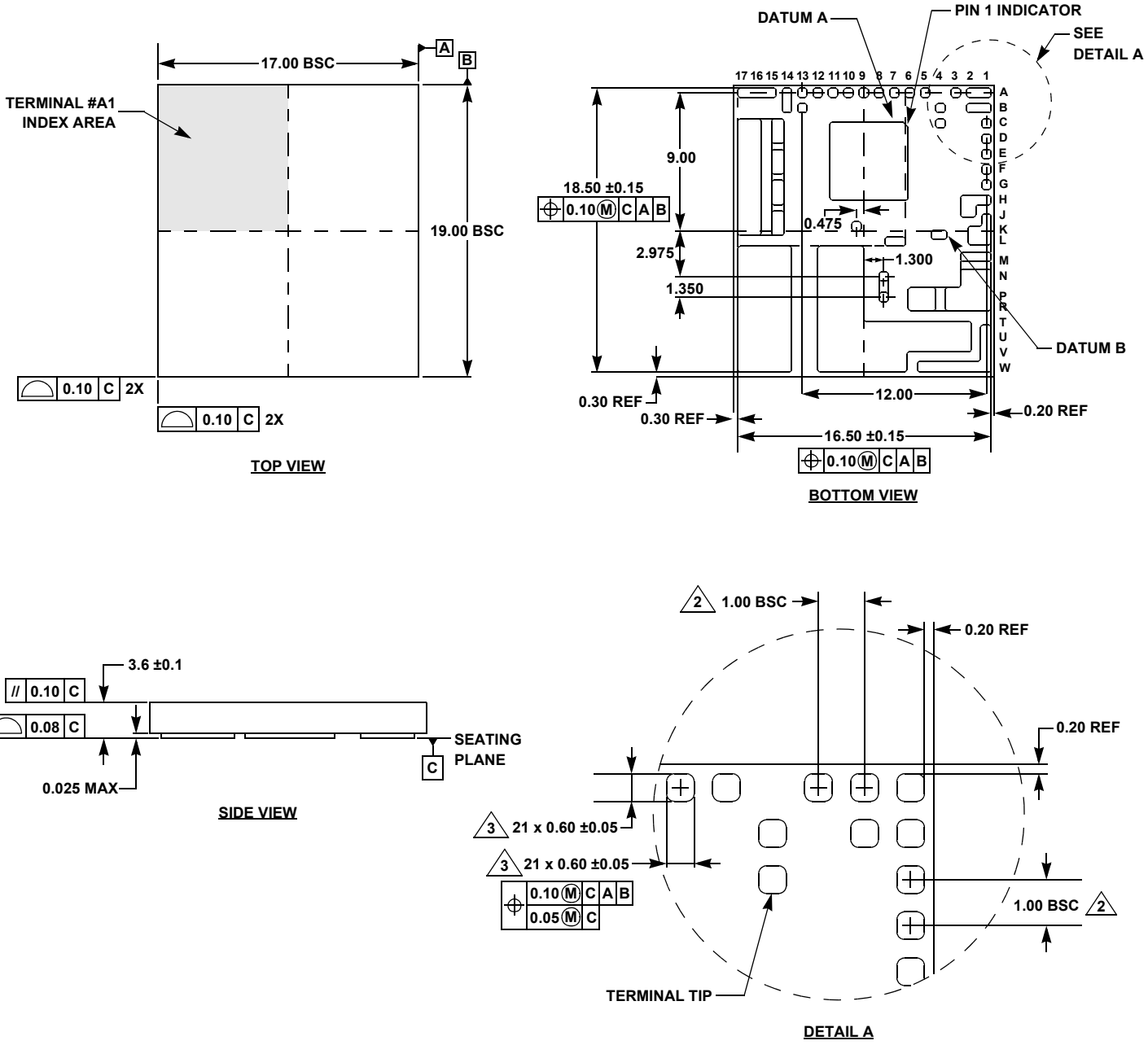
Package Outline Drawing

For the most recent package outline drawing, see Y41.17x19.

Y41.17x19

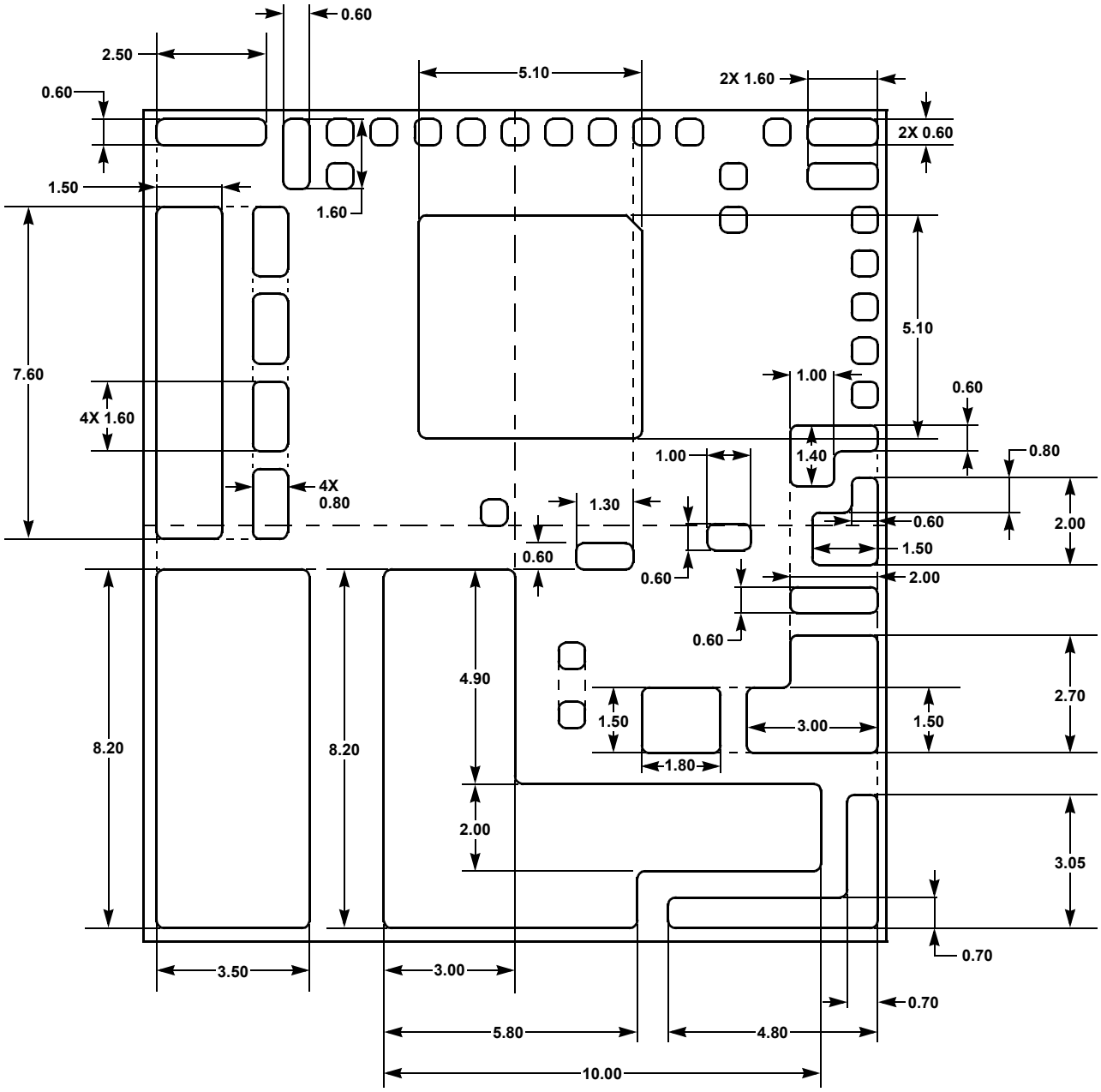
41 I/O 17.0mm x 19.0mmx3.6mm HDA MODULE

Rev 1, 5/16

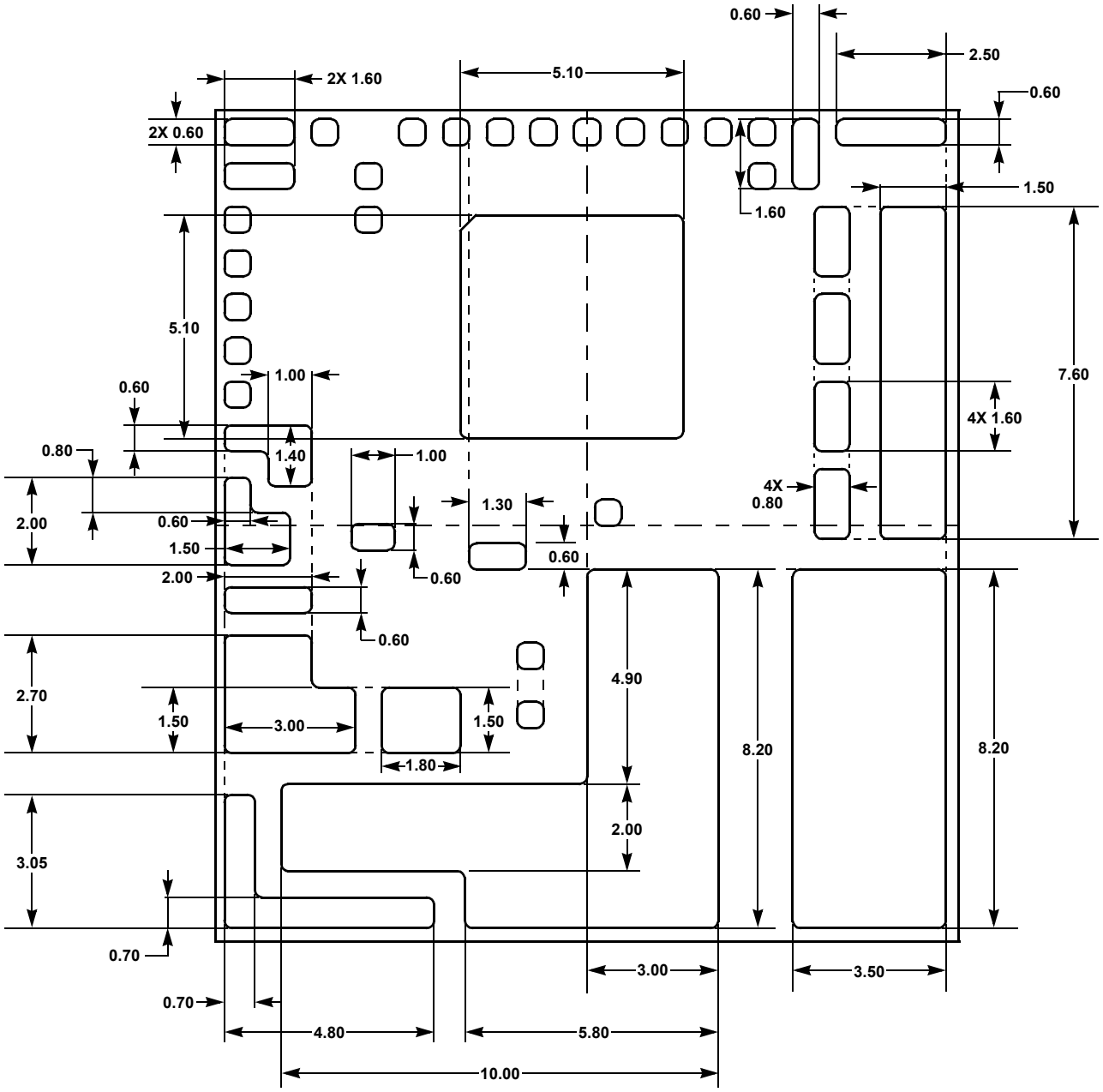


NOTES:

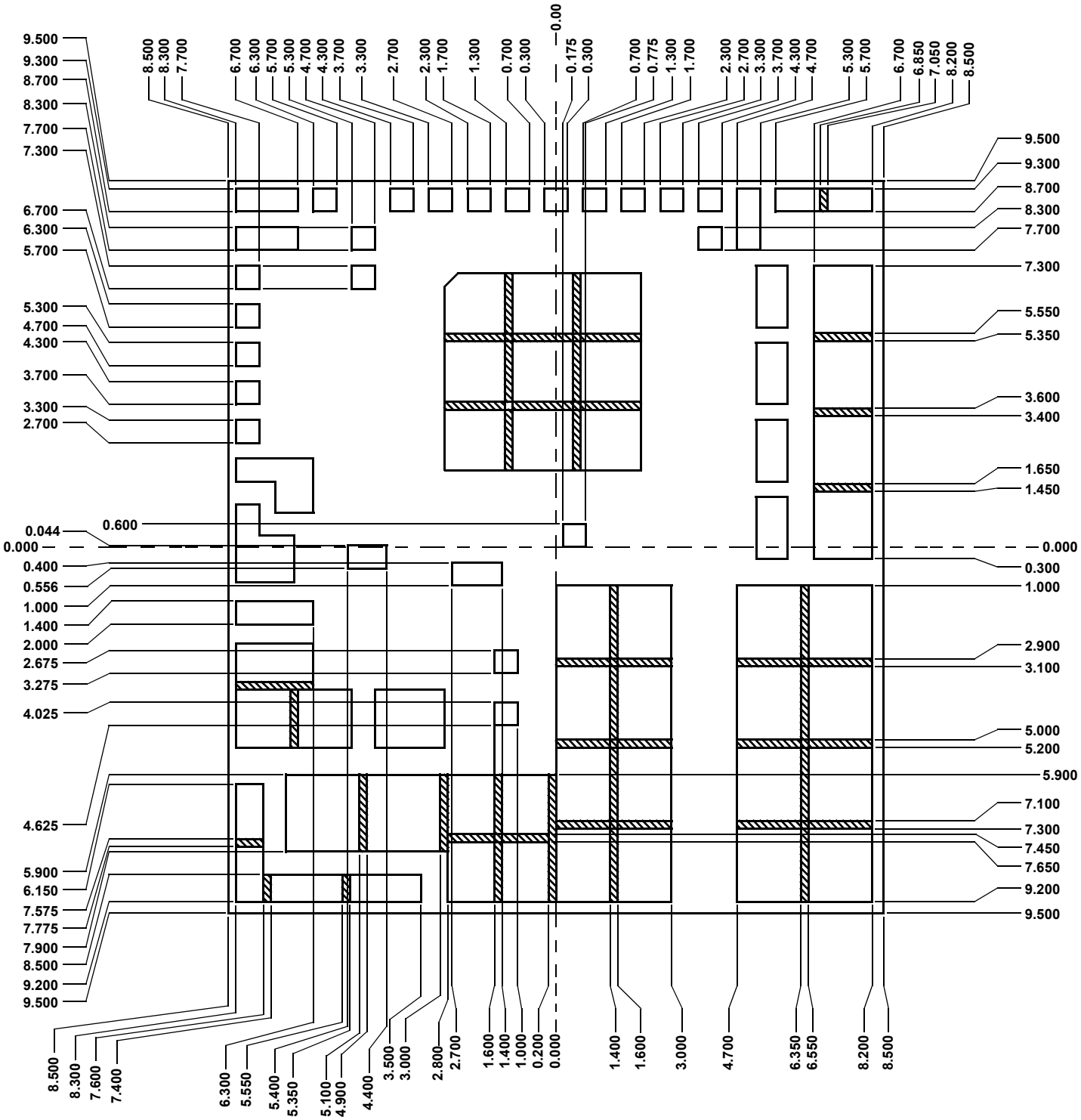
1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. The total number of I/O (excluding dummy pads).
4. Unless otherwise specified, tolerance: decimal ±0.10.
5. Dimensioning and tolerancing per ASME Y14.M-2009.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



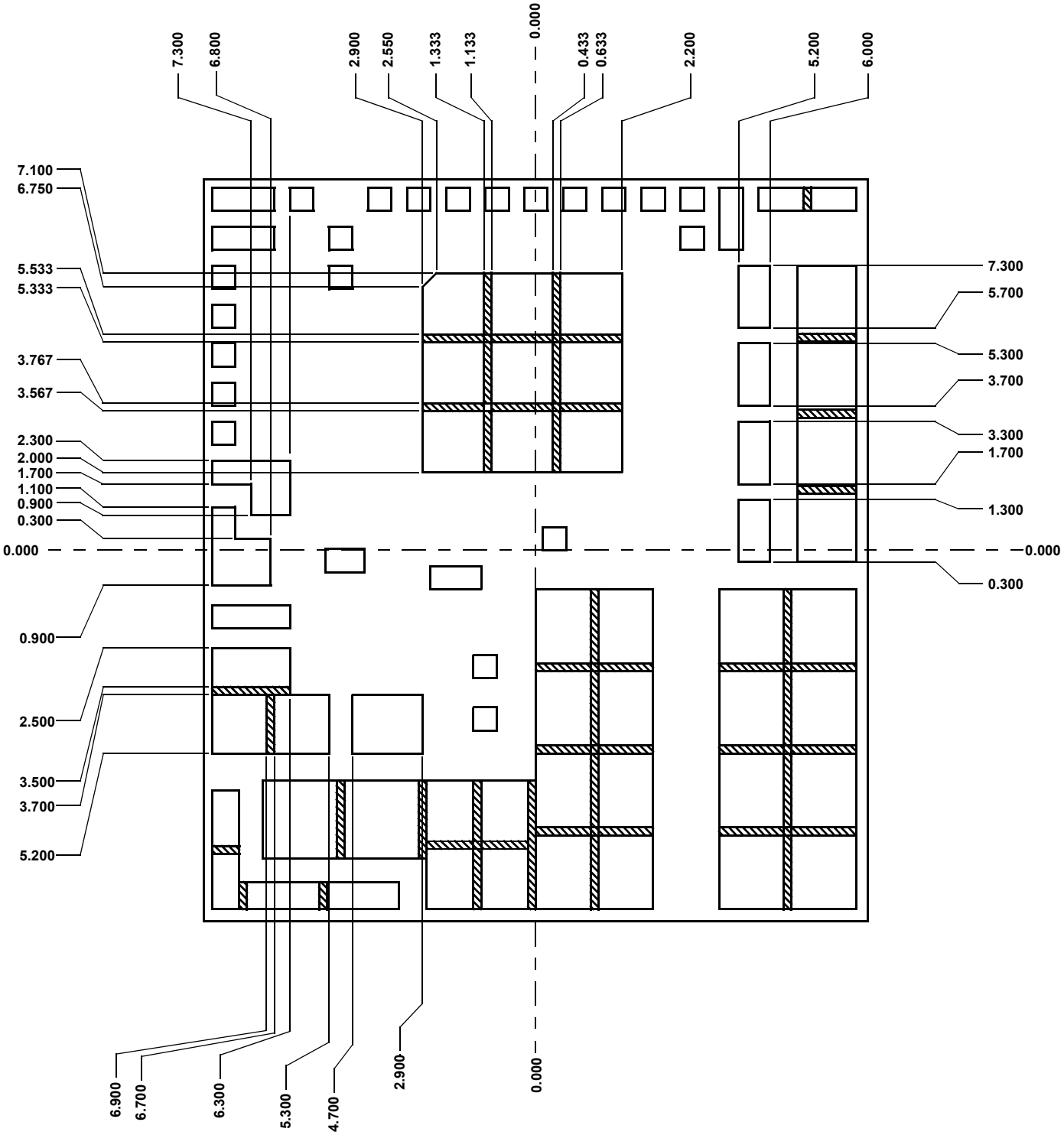
SIZE DETAILS FOR THE 16 EXPOSED DAPS
BOTTOM VIEW



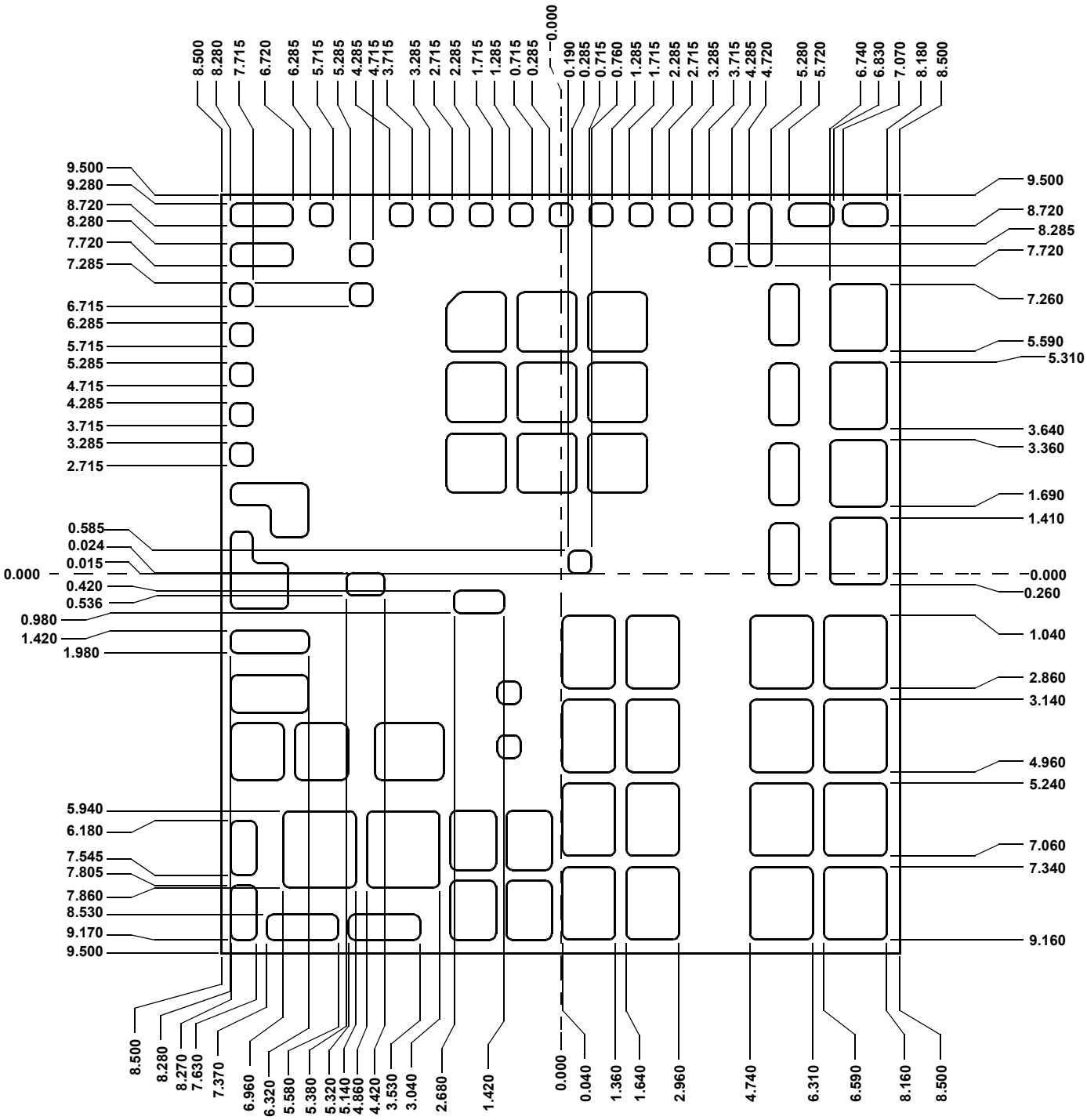
SIZE DETAILS FOR THE 16 EXPOSED DAPS
TOP VIEW



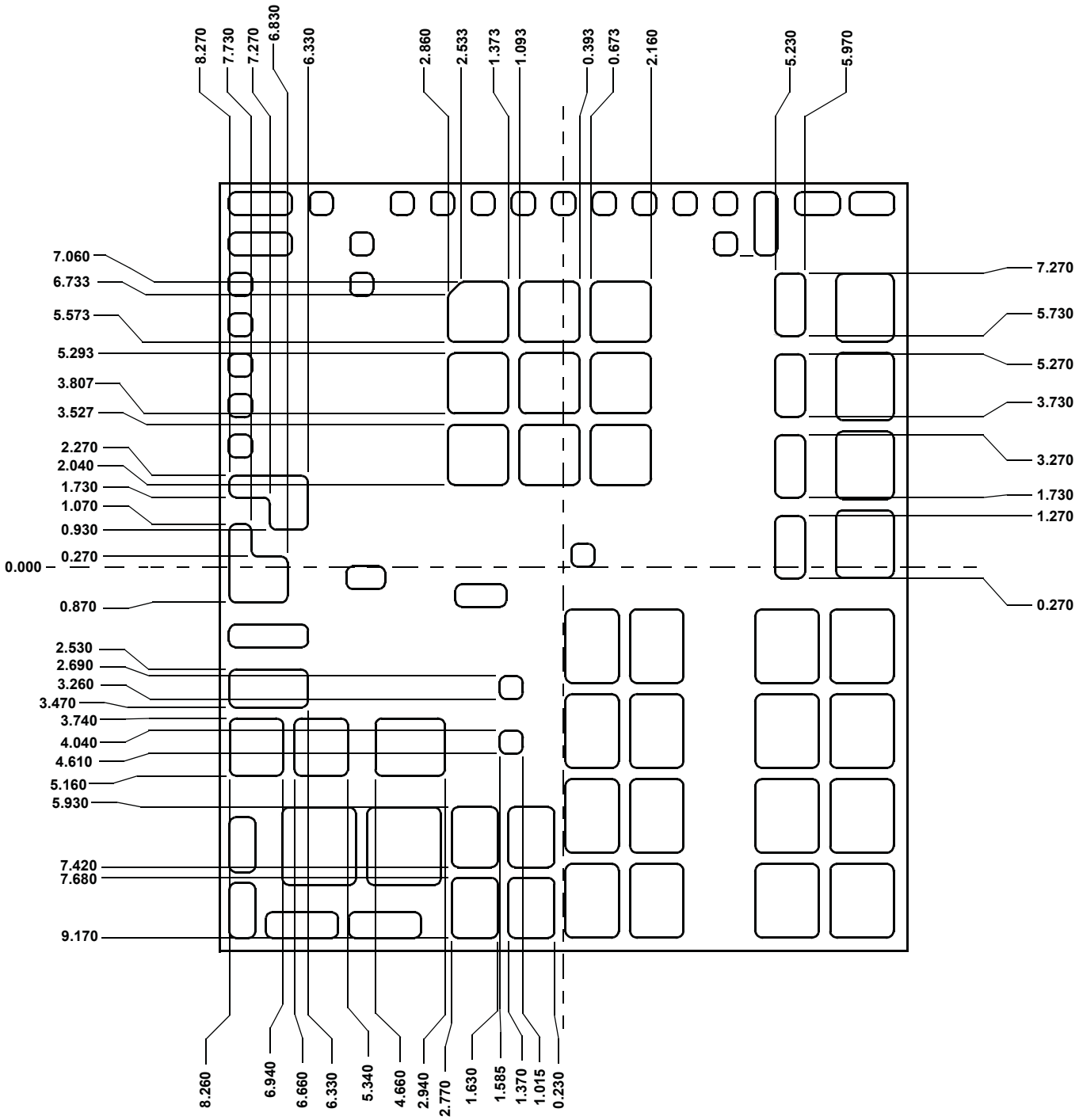
RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (1)
TOP VIEW



RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (2)
TOP VIEW



RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (1)
TOP VIEW



RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (2)
TOP VIEW