Power Supply IC for High Fidelity Audio

Negative Voltage Linear Regulator for High Fidelity Audio

BD37215MUV

General Description

BD37215MUV is a linear regulator of low noise (5.1µVrms) which is most suitable to high quality audio system. It operates at -16V to -3V and capable of supplying a maximum load of 1000mA.

In addition to the low noise, BD37215MUV has a high PSRR and good input transient fluctuation characteristic which makes it suitable for the stabilization of DC/DC converter output, and an ideal power supply to high precision analog circuits such as operational amplifier and headphone amplifier for audio.

Furthermore, when BD37215MUV is placed in standby mode, the supply current can be as small as 9.2µA(Typ) which can greatly reduce power consumption.

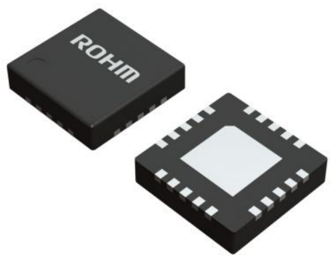
Key Specifications

- Input Voltage Range: -16.0V to -3.0V
- Output Voltage Range: -15.0V to -1.0V
- Output Current: 1.0A(Max)
- Output Voltage Noise*(Note 1)*: 5.1µVrms(10Hz to 100kHz, Typ)
- PSRR*(Note 2)*: 90dB(1kHz, Typ), 55dB(1MHz, Typ)
- Input Transient Response: 3mV(1.0V/µs, Typ)
- Standby Current: 9.2µA(Typ)
- Operating Temperature Range: -40°C to +85°C

(Note 1) C_{BC}=10µF, V_{OUT}= -1.0V, I_{OUT}=0.5A setting
(Note 2) C_{OUT}=47µF, V_{OUT}= -1.0V, I_{OUT}=0.5A setting

Package

Package	W(Typ) x D(Typ) x H(Max)
VQFN020V4040	4.00mm x 4.00mm x 1.00mm



VQFN020V4040

Features

- Ultra Low Noise, High PSRR
- Standby Mode controlled by Enable Pin using the positive voltage
- Soft Start Function controlled by External Capacitor
- Under Voltage Lockout Protection, Over Current Protection, Thermal Shutdown Protection

Applications

- High Quality Audio Equipment
- Power Supply for Operational Amplifier and Headphone Amplifier

Typical Application Circuit

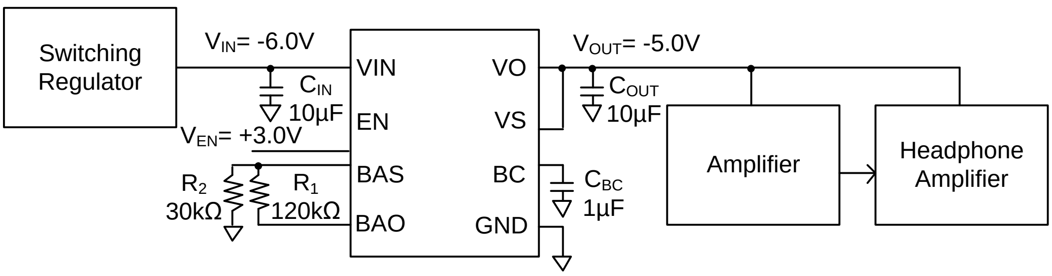


Figure 1. Basic Application Circuit Diagram (V_{OUT}= -5.0V)

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

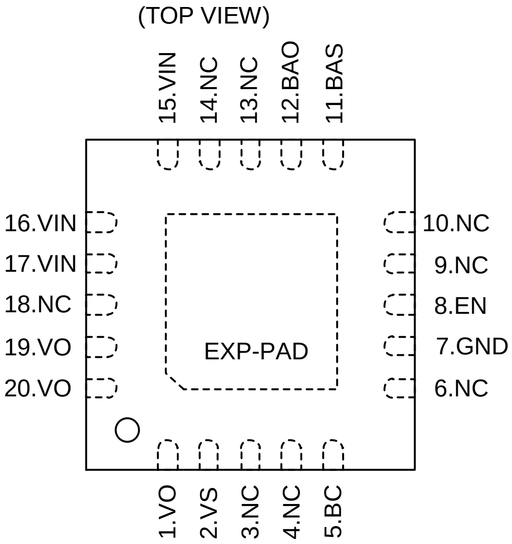


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	VO	Output voltage
2	VS	Output voltage feedback
3	NC	No connect *(Note 3)*
4	NC	No connect *(Note 3)*
5	BC	Bypass capacitor pin connected to ground
6	NC	No connect *(Note 3)*
7	GND	Ground
8	EN	Enable
9	NC	No connect *(Note 3)*
10	NC	No connect *(Note 3)*
11	BAS	Programmed voltage feedback
12	BAO	Programmed voltage output
13	NC	No connect *(Note 3)*
14	NC	No connect *(Note 3)*
15	VIN	Input voltage
16	VIN	Input voltage
17	VIN	Input voltage
18	NC	No connect *(Note 3)*
19	VO	Output voltage
20	VO	Output voltage
-	EXP-PAD	The exposed pad should be connected to VIN pattern.

(Note 3) The NC PINs should not be connected to any pattern or should be connected to GND.

Block Diagram

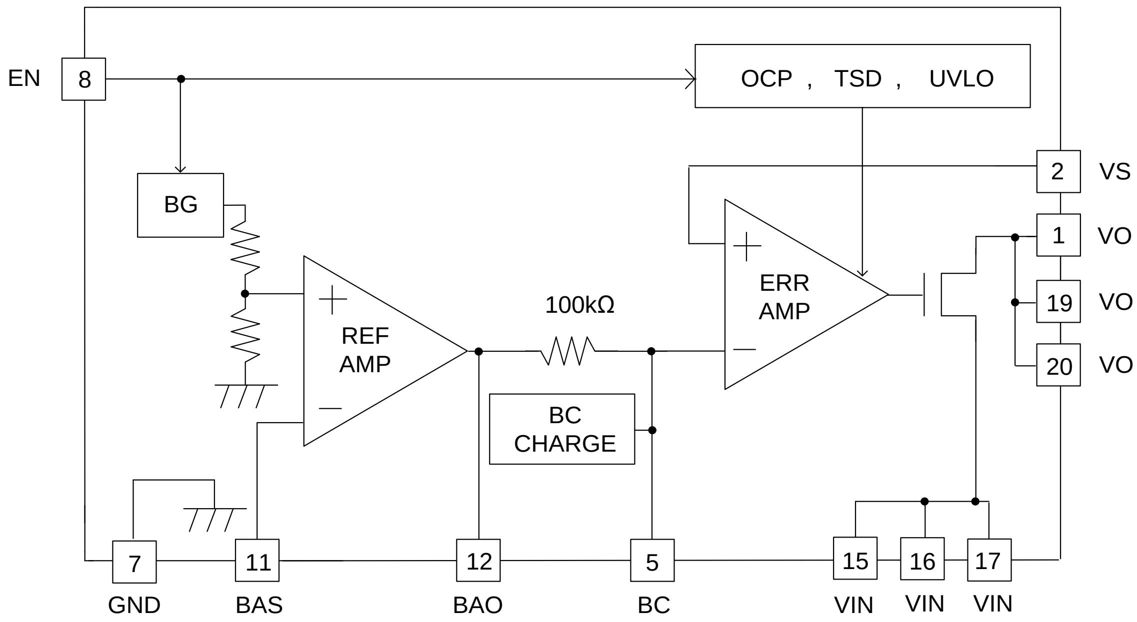


Figure 3. Block Diagram

Description of Block

1. Enable
   Assuming EN is set to L, the IC can be set to standby state. In standby state, the output is OFF and since it will be in static state, the power consumption can be reduced. It is unavailable to input the negative voltage to EN.

2. Rising, Falling, and EN Controlled Timing

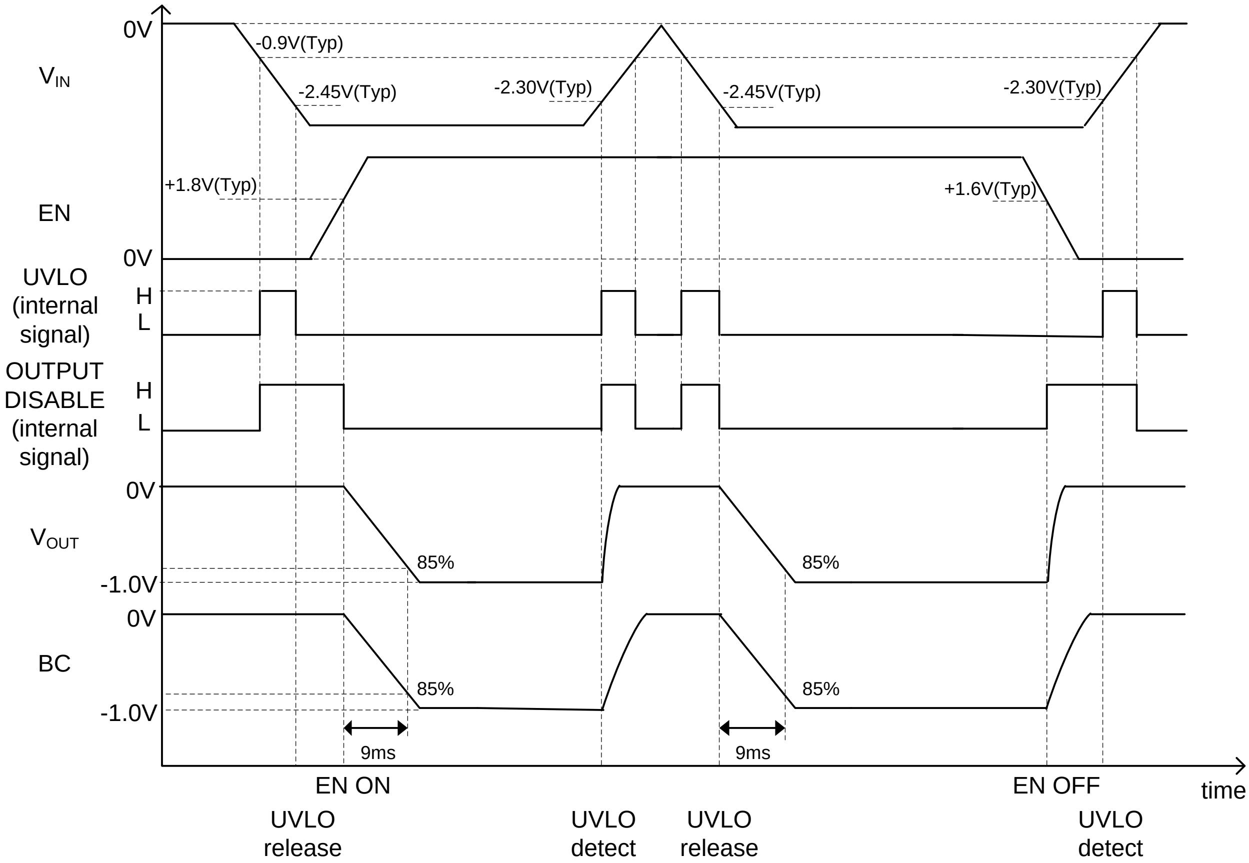


Figure 4. The Sequence Waveform During V_{IN}/EN Rising and Falling
(When at Capacitance of C_{BC} 1µF and Output -1.0V Settings)

It will operate if EN is H and UVLO (Under Voltage Lockout) is released. In addition, when EN is L or UVLO is detected, the regulator operation stops.
V_{IN} does not have the necessity to supply earlier than EN.
The maximum slew rate of input voltage has to be set 1.0V/µs or below.

3. Soft Start Function
   In BD37215MUV, there exists a function that limits the rising speed of output when EN rises by the capacitor connected to BC due to decrease of inrush current of output. The rising speed depends on the internal charging current 100µA(Typ), the capacitance value connected to BC and on the output programmed voltage. It is about 9ms (Typ) if capacitance of C_{BC} is 1µF and output programmed voltage is -1.0V, and almost 40ms (Typ) if output programmed voltage is set to -5.0V. The above is an aim level, and soft start time may change depending on the input and output voltage condition.

4. REFAMP
   REFAMP sets its output voltage. Refer Selection of Components Externally Connected (Page 16) about setting of output voltage.

5. BC
   Noise at the output voltage of REFAMP is reduced because of the internal resistor 100kΩ and the external BC capacitor. In addition to it, the external BC capacitor also has a soft start function so the rising speed can be adjusted by this value. The higher value of capacitor will decrease the noise but the soft start time will be longer.

6. ERRAMP
   The ERRAMP outputs the voltage set in REFAMP at 1 time of closed gain. VS must be connected to VO by all means. In addition, VS can decrease a voltage drop by the pattern resistance on the VO course by returning the voltage from the supply point.

Absolute Maximum Rating (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage (PIN 15, 16, 17)	V_{IN}	-17.5 to +0.3	V
EN Pin Voltage (PIN 8)	V_{EN}	-0.3 to +7.0	V
Pin Voltage (PIN 11)	V_{PIN1}	-7.0 to +0.3	V
Pin Voltage (PIN 1, 2, 5, 12, 19, 20)	V_{PIN2}	-17.5 to +0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.*

Thermal Resistance *(Note 4)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 6)*	2s2p *(Note 7)*	
VQFN020V4040				
Junction to Ambient	θ_{JA}	153.90	37.40	°C/W
Junction to Top Characterization Parameter *(Note 5)*	Ψ_{JT}	13.00	7.00	°C/W

(Note 4) Based on JESD51-2A(Still-Air)

(Note 5) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 6) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 7) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 8)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm (Square)	35µm	74.2mm (Square)	70µm

(Note 8) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{IN}	-16.0	-	-3.0	V
Output Voltage Setting is within a Possible Range	V_{OUT}	-15.0	-	-1.0	V
Output Current *(Note 9)*	I_{OUT}	-	-	1.0	A
Operating Temperature	Topr	-40	+25	+85	°C

(Note 9) Tjmax should not be exceeded.

Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitor (Note 10)	C_{IN}	2.2	10	-	µF	Film capacitors are recommended
Output Capacitor (Note 10, 11)	C_{OUT}	1	10	-	µF	Film capacitors are recommended
BC Capacitor (Note 10, 11)	C_{BC}	0.01	1	-	µF	Film capacitors are recommended

(Note 10) Set the capacity of the capacitor not to be less than the minimum in consideration of temperature or DC bias properties.
(Note 11) Refer the Selection of Components Externally Connected written in Page 16 and Page 17, and decide the value of each capacitor.

Electrical Characteristics

(Unless otherwise specified, V_{IN}= V_{OUT}-1.0V or -3.0V whichever is smaller V_{OUT}= -1.0V Ta=25°C C_{OUT}=10µF C_{BC}=1µF I_{OUT}=5mA V_{EN}= +3V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current (Note 12)	I_{CC}	-	2.0	4.0	mA	-
Standby Current (Note 12)	I_{STB}	-	9.2	22.5	µA	V_{IN}= -16V, V_{EN}=0V
Reference Voltage	V_{REF}	-1.01	-1.00	-0.99	V	BAO voltage
Line Regulation	D_{VI}	-20	-1	-	mV	V_{IN}= -3V to -16V
Load Regulation (Note 13)	D_{VL}	-20	-3	-	mV	I_{OUT}=0A to 1000mA
Dropout Voltage (Note 13)	V_{SAT}	-0.5	-0.3	-	V	I_{OUT}=1000mA, V_{OUT}= -3.3V
PSRR 1kHz	$PSRR_{1kHz}$	-	90	-	dB	f=1kHz , C_{OUT}=47µF
PSRR 1MHz	$PSRR_{1MHz}$	-	55	-	dB	f=1MHz, C_{OUT}=47µF
Output Noise Voltage (Note 13)	V_{NOISE}	-	5.1	-	µVrms	BW=10Hz to 100kHz, C_{BC}=10µF, I_{OUT}=500mA
Over Current Protection Detect Current (Note 13)	I_{OCP}	1000	-	-	mA	-
UVLO Detect Voltage	V_{UVLOH}	-2.50	-2.30	-2.10	V	-
UVLO Release Voltage	V_{UVLOL}	-2.65	-2.45	-2.25	V	-
EN Input H Level	V_{THENH}	2.5	-	5.5	V	-
EN Input L Level	V_{THENL}	0.0	-	0.8	V	-
EN Input Current	I_{EN}	-	1.23	2.20	µA	-

(Note 12) The polarity of I_{CC} and I_{STB} are defined that the direction of current flowing from VIN are positive.
(Note 13) The polarity of I_{OCP} and I_{OUT} are defined that the direction of current flowing to VO are positive.
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Typical Performance Curves

(Unless otherwise specified, V_{IN}= V_{OUT}-1.0V or -3.0V whichever is smaller V_{OUT}= -1.0V Ta=25°C C_{OUT}=10µF C_{BC}=1µF I_{OUT}=5mA V_{EN}= +3V)

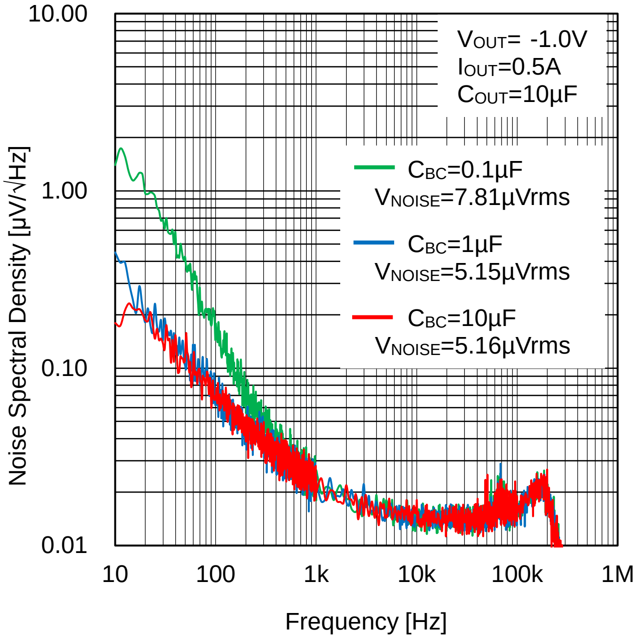


Figure 5. Noise Spectral Density vs Frequency (V_{OUT}= -1.0V)

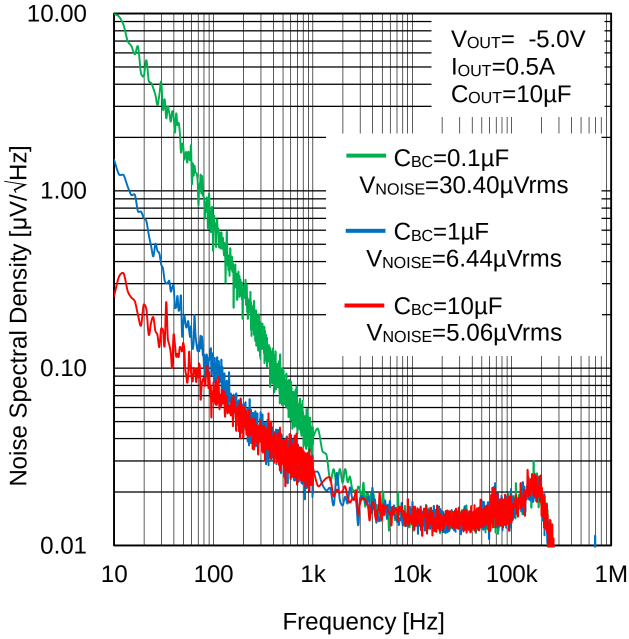


Figure 6. Noise Spectral Density vs Frequency (V_{OUT}= -5.0V)

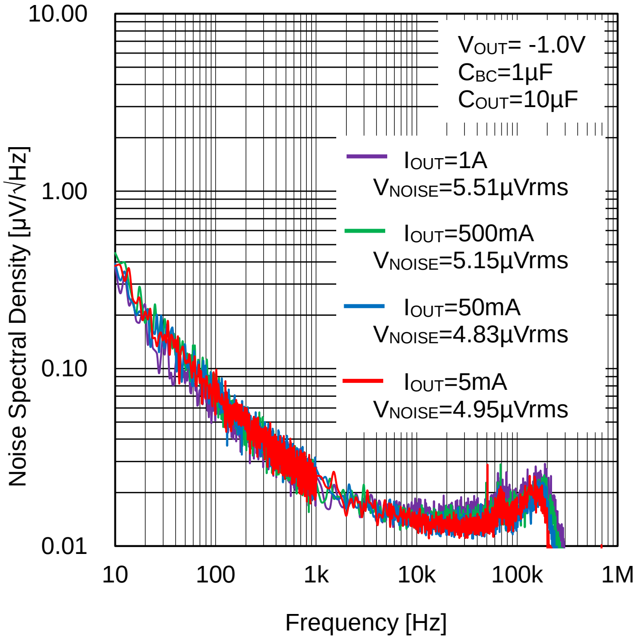


Figure 7. Noise Spectral Density vs Frequency (V_{OUT}= -1.0V)

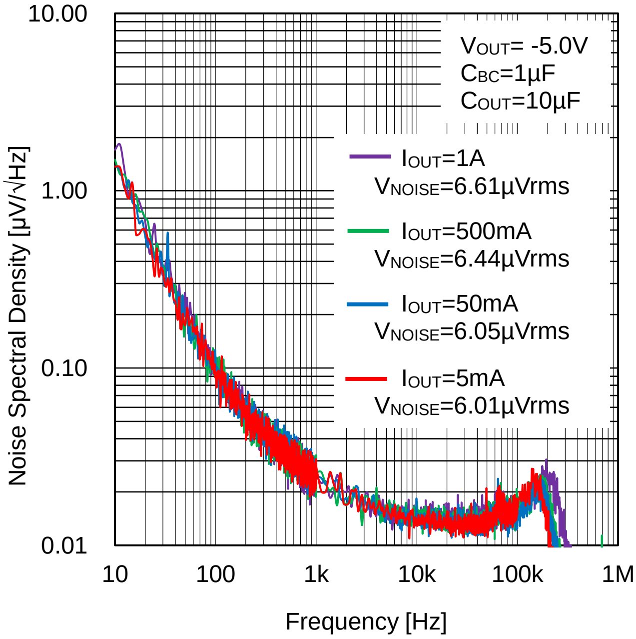


Figure 8. Noise Spectral Density vs Frequency (V_{OUT}= -5.0V)

Typical Performance Curves – continued

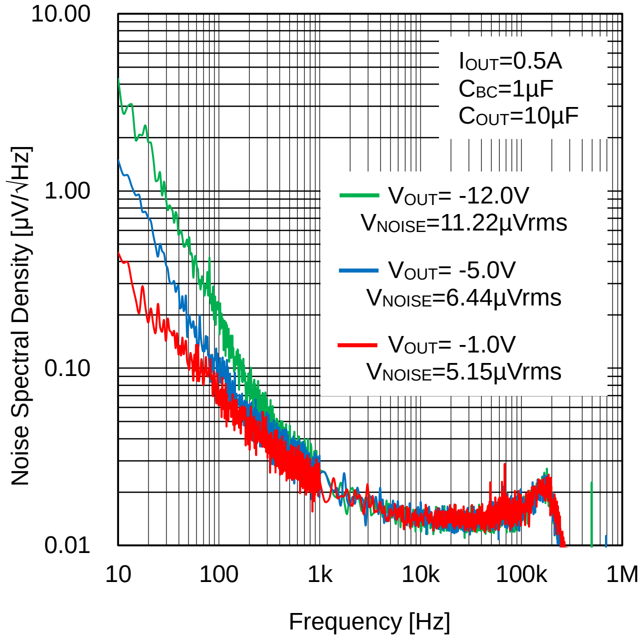


Figure 9. Noise Spectral Density vs Frequency

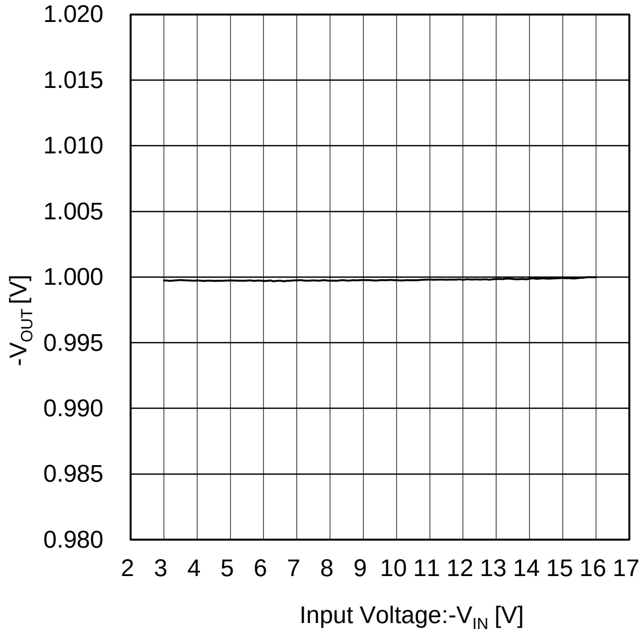


Figure 10. Line Regulation (D_{VI})
(V_{OUT}= -1.0V)

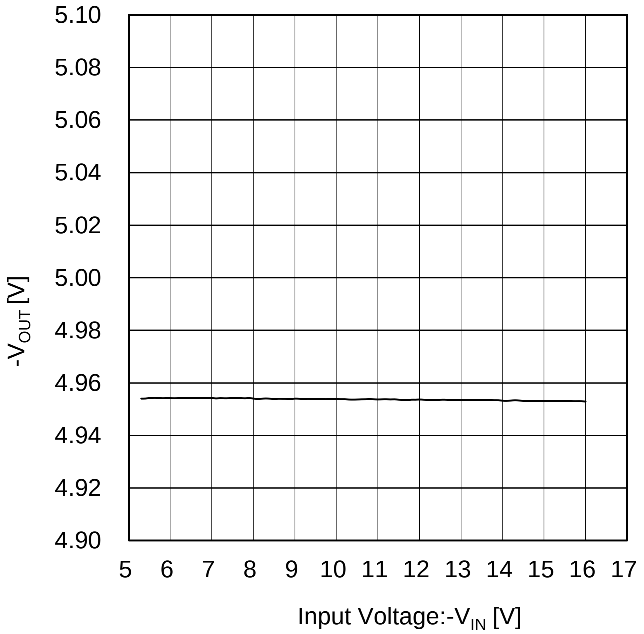


Figure 11. Line Regulation (D_{VI})
(V_{OUT}= -5.0V)

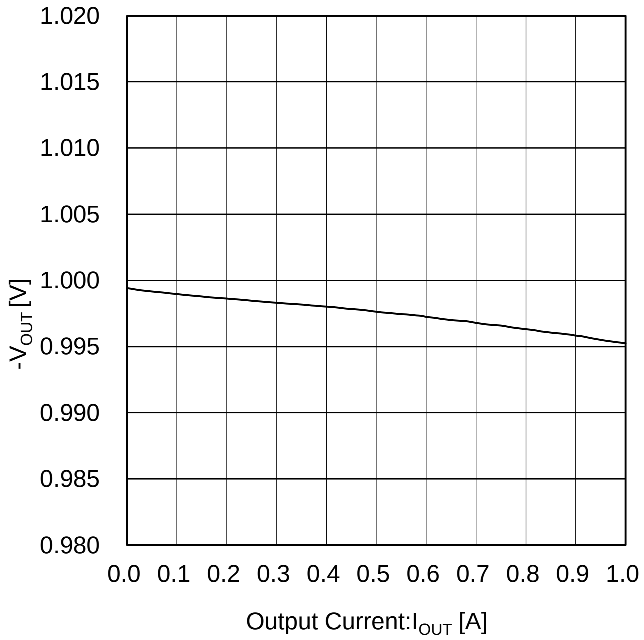


Figure 12. Load Regulation (D_{VL})
(V_{OUT}= -1.0V)

Typical Performance Curves – continued

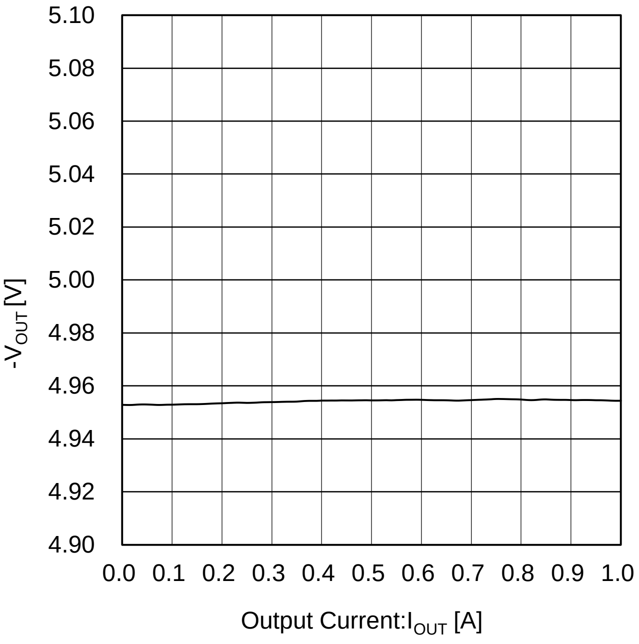


Figure 13. Load Regulation (D_{VL})
(V_{OUT}= -5.0V)

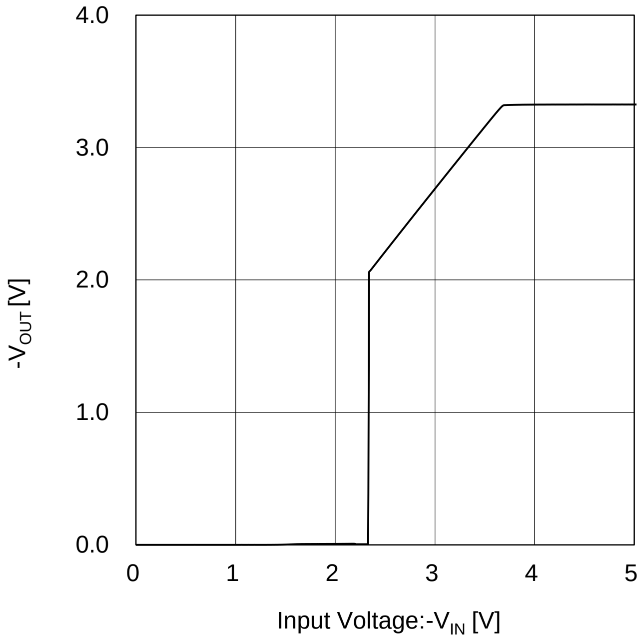


Figure 14. V_{OUT} vs V_{IN}
(V_{OUT}= -3.3V)

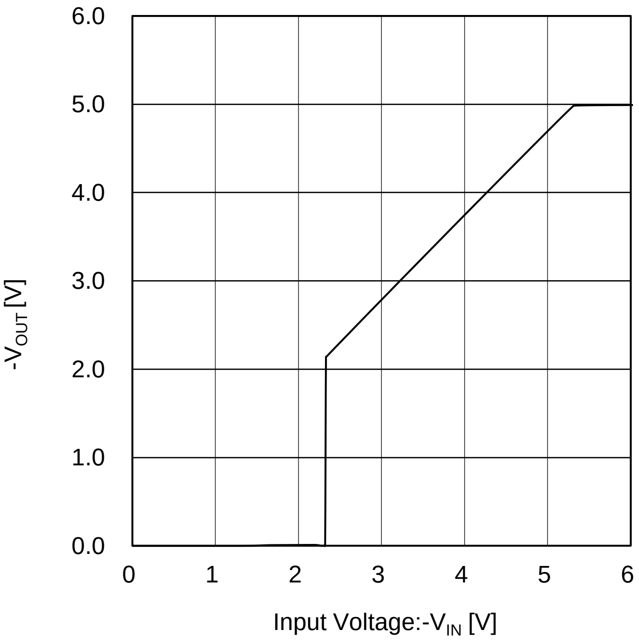


Figure 15. V_{OUT} vs V_{IN}
(V_{OUT}= -5.0V)

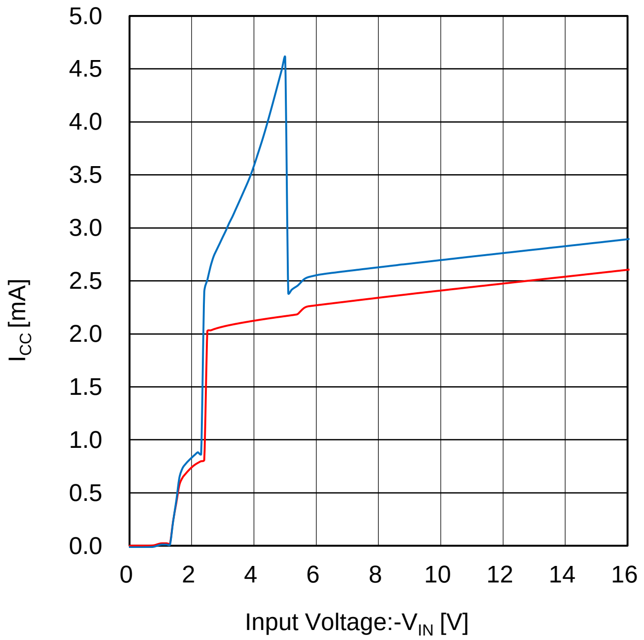


Figure 16. I_{CC} vs V_{IN}

Typical Performance Curves – continued

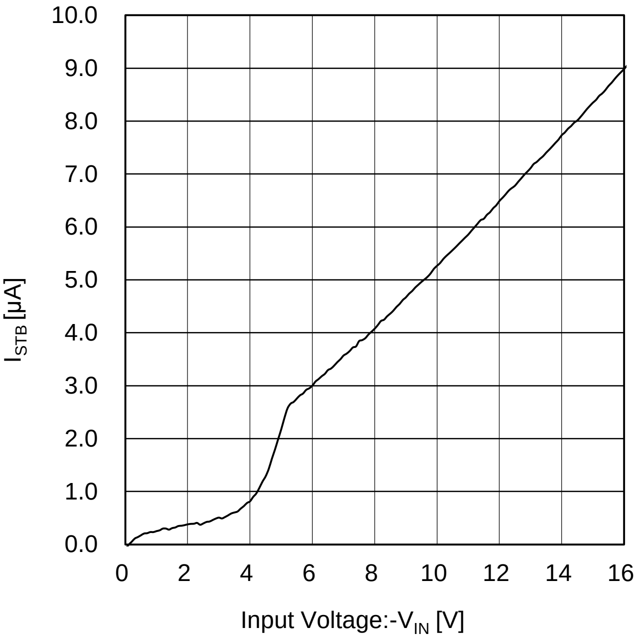


Figure 17. I_{STB} vs V_{IN}

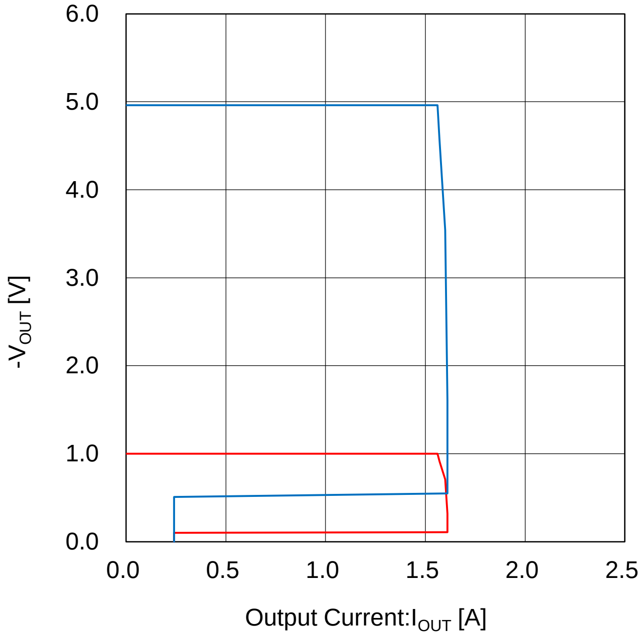


Figure 18. V_{OUT} vs I_{OUT}

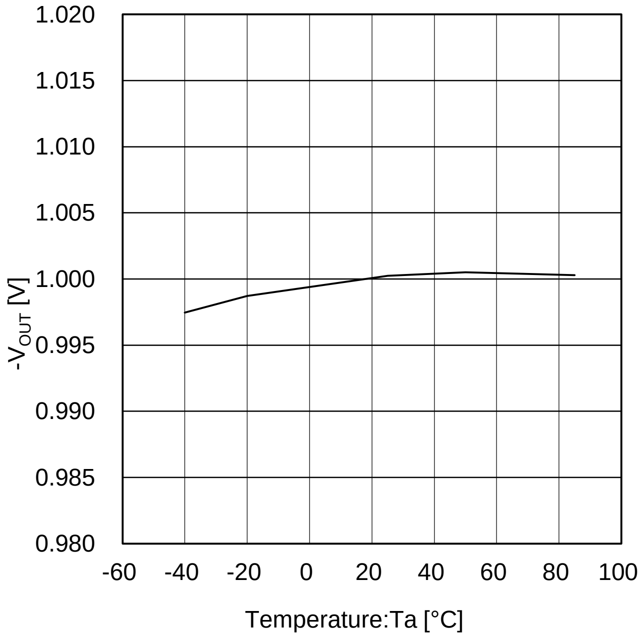


Figure 19. V_{OUT} vs Ta
(V_{OUT}= -1.0V)

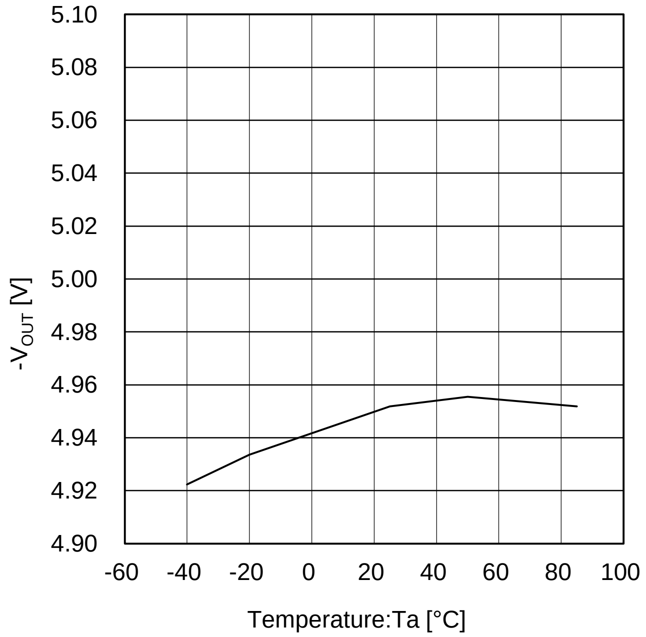


Figure 20. V_{OUT} vs Ta
(V_{OUT}= -5.0V)

Typical Performance Curves – continued

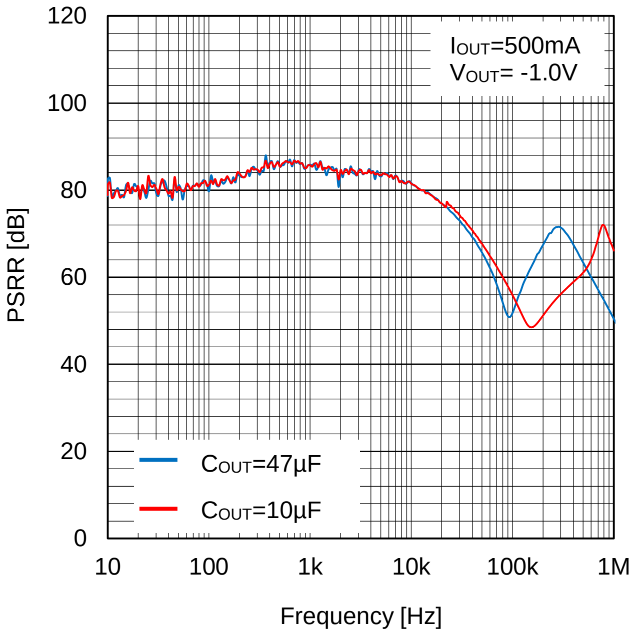


Figure 21. Power-Supply Rejection Ratio (V_{OUT}= -1.0V)

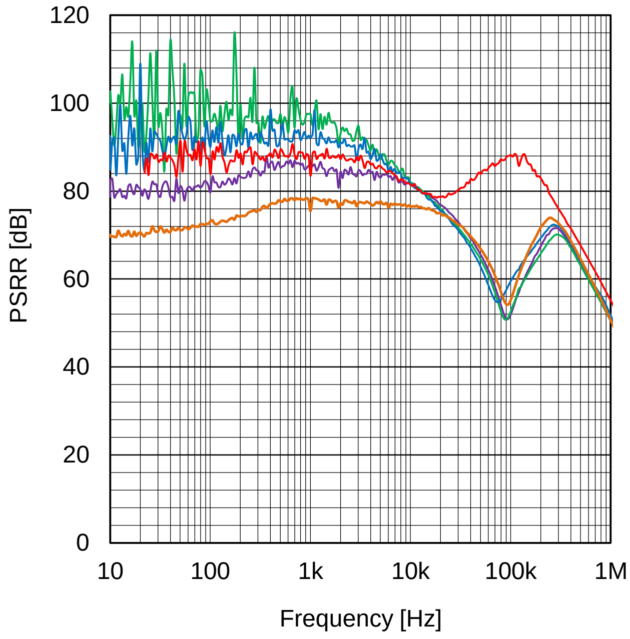


Figure 22. Power-Supply Rejection Ratio (V_{OUT}= -1.0V)

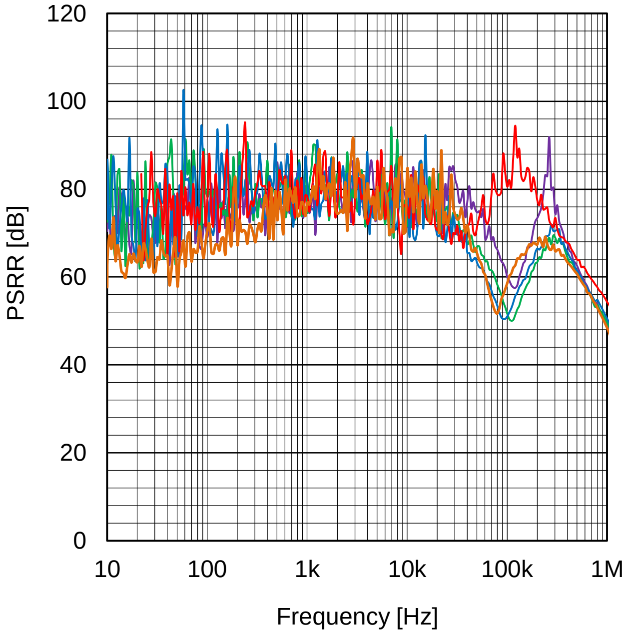


Figure 23. Power-Supply Rejection Ratio (V_{OUT}= -5.0V)

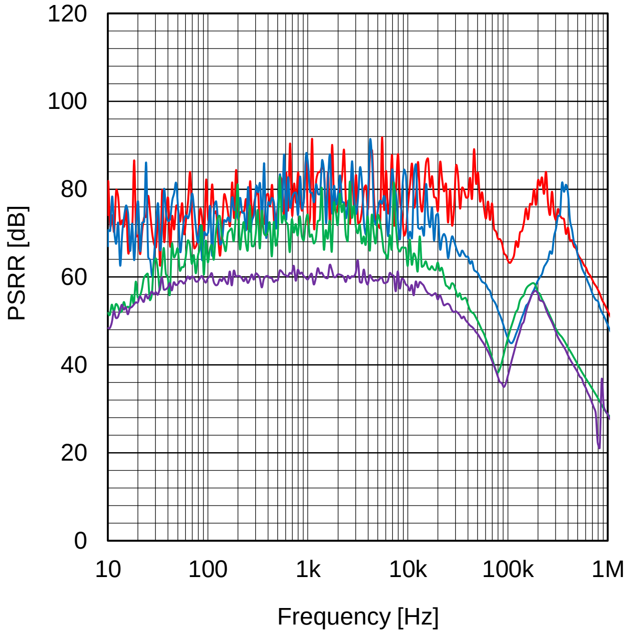


Figure 24. Power-Supply Rejection Ratio (V_{OUT}= -3.3V)

Typical Performance Curves – continued

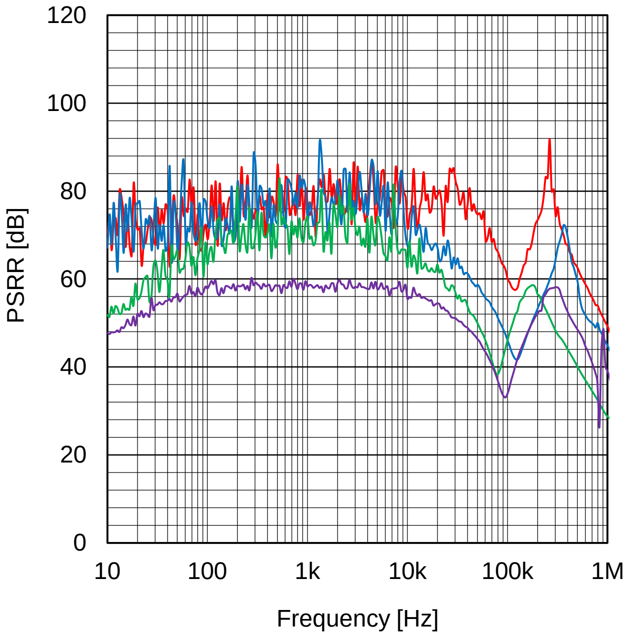


Figure 25. Power-Supply Rejection Ratio
(V_{OUT}= -5.0V)

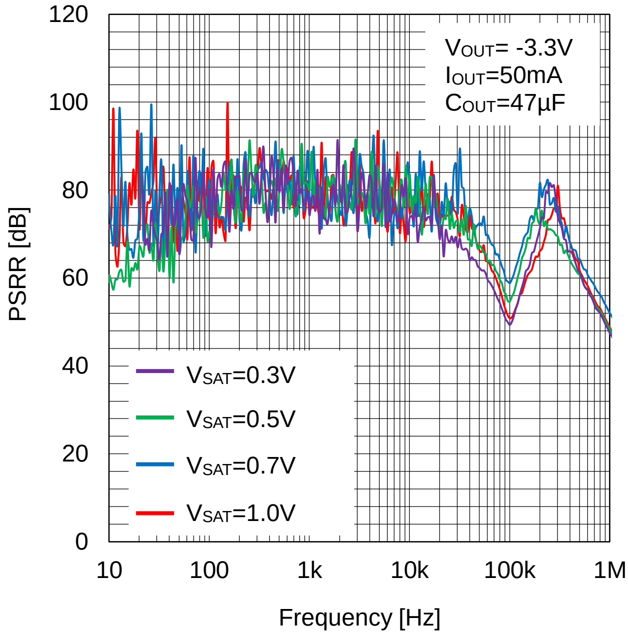


Figure 26. Power-Supply Rejection Ratio
(V_{OUT}= -3.3V)

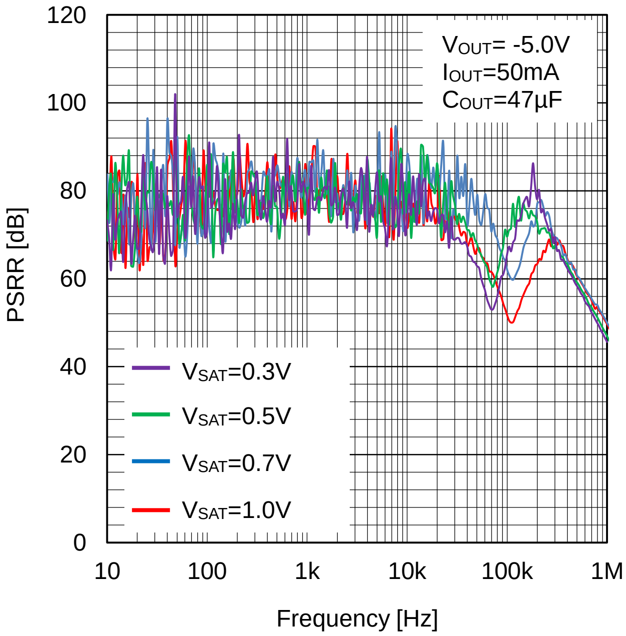


Figure 27. Power-Supply Rejection Ratio
(V_{OUT}= -5.0V)

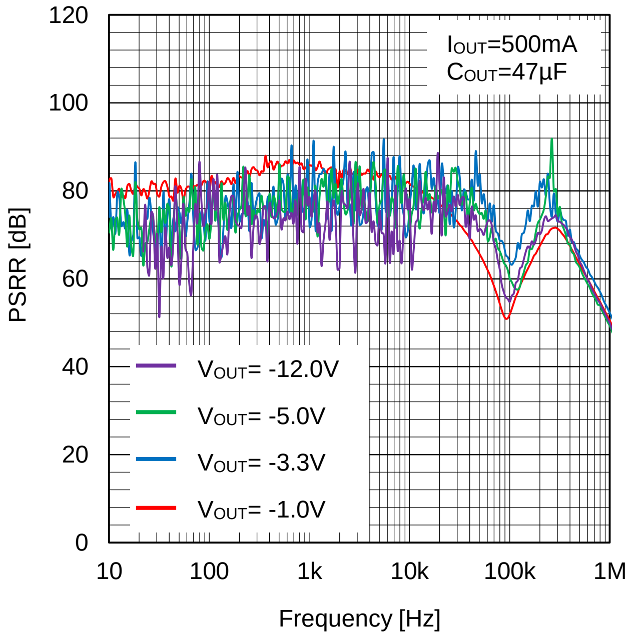


Figure 28. Power-Supply Rejection Ratio

Typical Performance Curves – continued

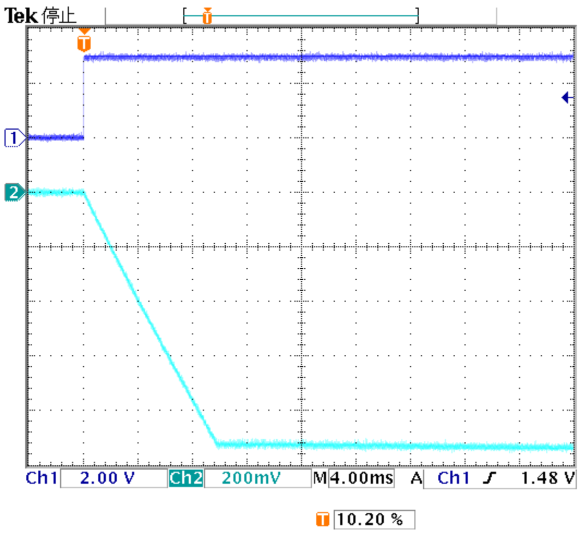


Figure 29. Soft Start
(V_{OUT}= -1.0V)

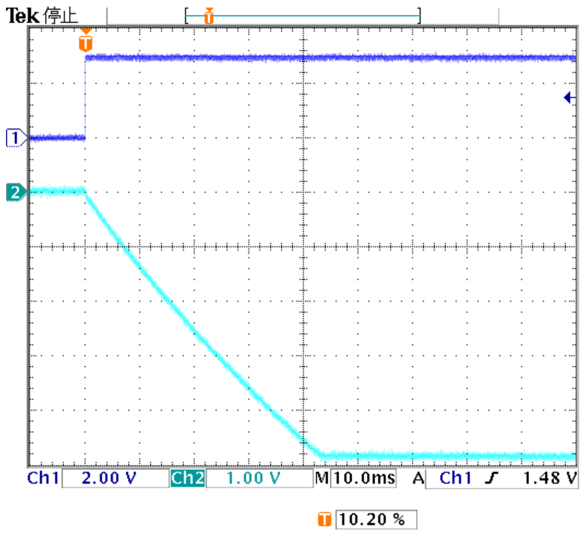


Figure 30. Soft Start
(V_{OUT}= -5.0V)

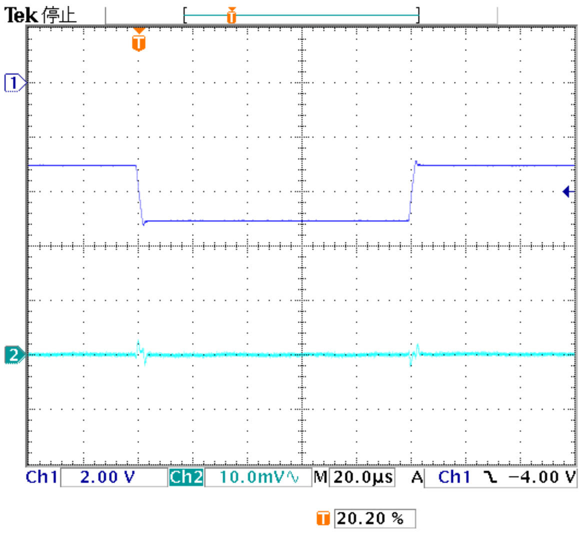


Figure 31. Line Transient
(I_{OUT}=500mA Slew Rate=1.0V/µs V_{OUT}= -1.0V C_{OUT}=2.2µF)

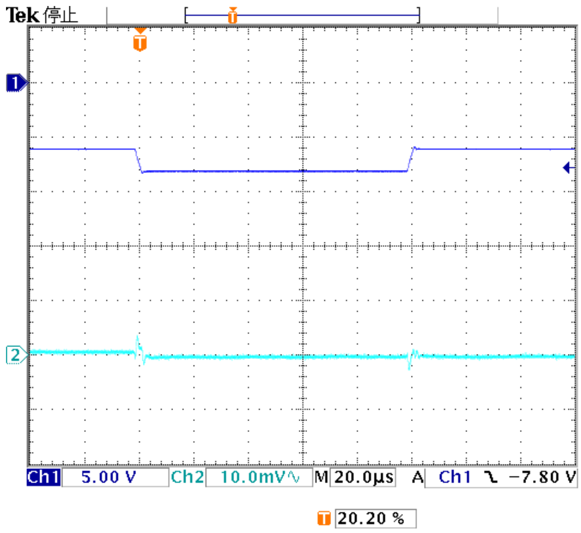


Figure 32. Line Transient
(I_{OUT}=500mA Slew Rate=1.0V/µs V_{OUT}= -5.0V C_{OUT}=2.2µF)

Typical Performance Curves – continued

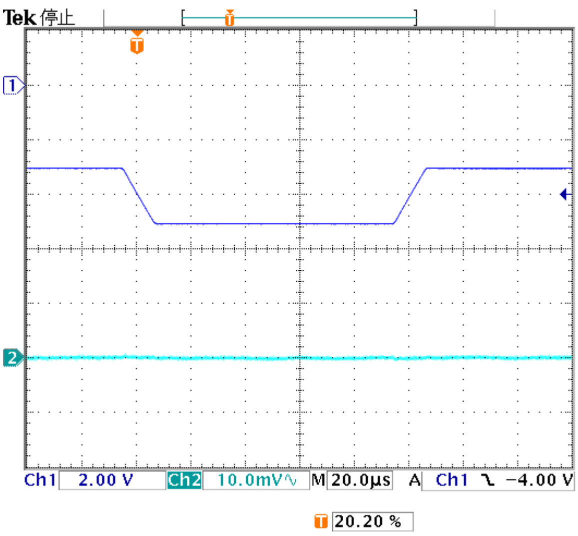


Figure 33. Line Transient
(I_{OUT}=500mA Slew Rate=0.2V/µs V_{OUT}= -1.0V C_{OUT}=2.2µF)

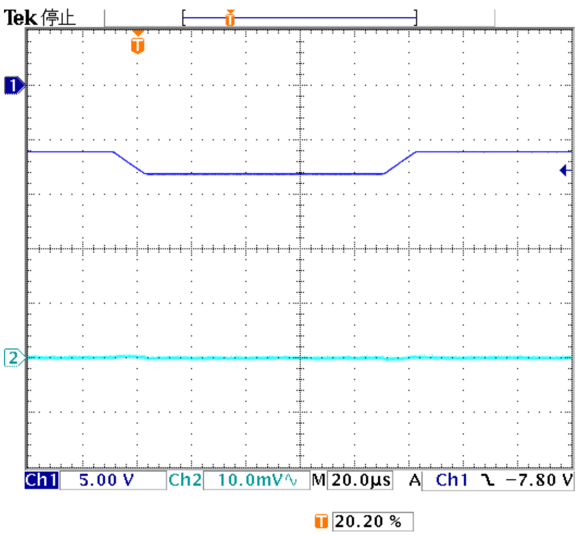


Figure 34. Line Transient
(I_{OUT}=500mA Slew Rate=0.2V/µs V_{OUT}= -5.0V C_{OUT}=2.2µF)

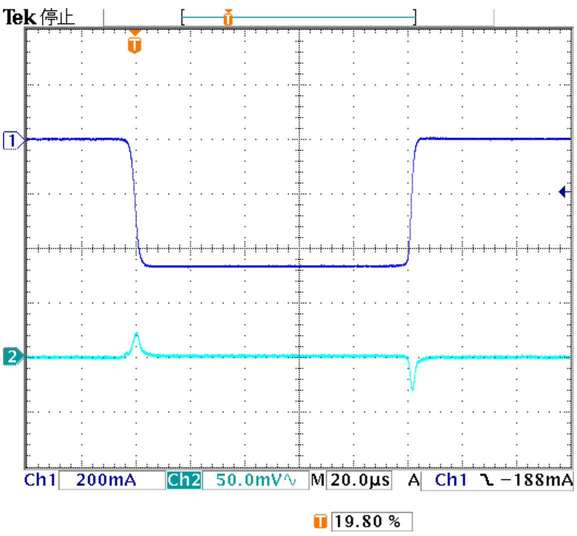


Figure 35. Load Transient
(I_{OUT}=0mA ～ 500mA V_{OUT}= -1.0V C_{OUT}=2.2µF)

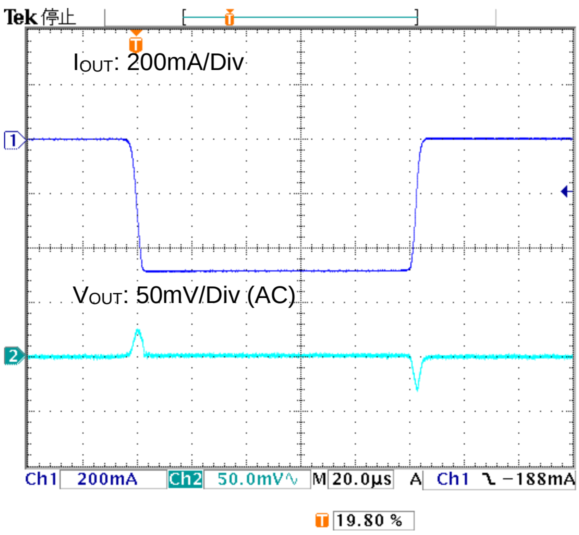
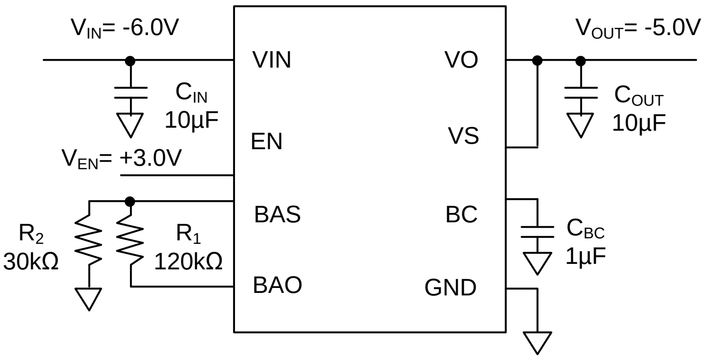


Figure 36. Load Transient
(I_{OUT}=0mA ～ 500mA V_{OUT}= -5.0V C_{OUT}=2.2µF)

Application Examples



Parts	Maker	Value	Parts Number
R_1	ROHM	120kΩ	MCR03EZPD1203
R_2	ROHM	30kΩ	MCR03EZPD3002
C_{IN}	Rubycon	10µF	16MU106M4532
C_{OUT}	Rubycon	10µF	16MU106M4532
C_{BC}	Rubycon	1µF	16MU105M3216

(Note) This application example is just one case. Actual setting will be decided after a thorough evaluation and verification in the set.
(Note) The value of R_1 and R_2 is set that $R_1 + R_2$ becomes 100kΩ or above.
The resistance for voltage setting is recommended the one that is 1% accuracy or below.
(Note) Set the capacity of the capacitor not to be less than the minimum in consideration of temperature or DC bias properties.

Figure 37. Application Circuit (V_{OUT}= -5.0V)

Selection of Components Externally Connected

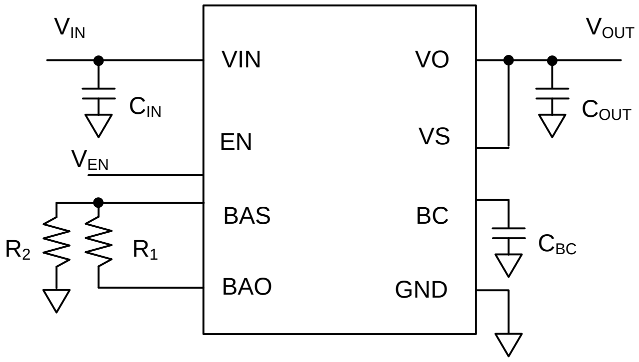


Figure 38. External Components Connection

1. Output Voltage Setting
   To set output voltage, connect resistance of R_1 between BAO-BAS and connect resistance of R_2 in between BAS-GND. The value of R_1 and R_2 is set that R_1 + R_2 becomes 100kΩ or above. In addition, the resistance for voltage setting is recommended the one that is 1% accuracy or below. In the case to use -1.0V setting, short BAS with BAO.

$$V_{OUT} = V_{BAS} \times \frac{R_1+R_2}{R_2} \quad \text{[V]}$$

V_{BAS} = -1.0V (Typ)

2. Output Capacitor C_{OUT}
   Output capacitor should be selected 1µF or above considering about the voltage modulation, thermal characteristics, and distribution of the value. Installation of output capacitor in the position near the pin in between VO and GND is recommended. In addition, the rated voltage of capacitor should be set with enough margins to output voltage.
   The ESR of Output Capacitor effect the stability of IC operation. Refer the stable operation range for the selection of Output Capacitor which is given in the reference data of Figure 39. This reference data is measured in combination of the ceramic capacitor of 2.2µF and resistance in series to Output. The Stable operation range of this graph is given by only the IC and load resistance. For actual applications the stable operating range is influenced by the wiring impedance of the PCB panel, input supply impedance and load impedance. Therefore verification of the final operating environment is needed.

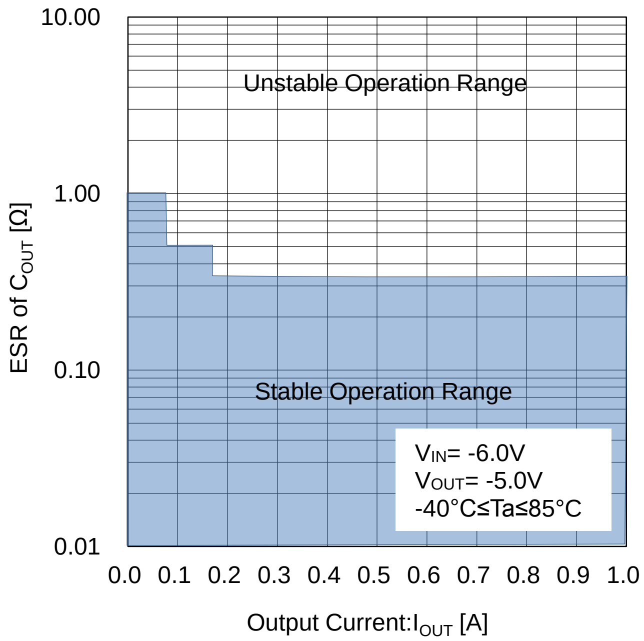


Figure 39. ESR of C_{OUT} vs I_{OUT}

Selection of Components Externally Connected – continued

3. Input Capacitor C_{IN}
   Input capacitor should be selected 2.2µF or above considering about the voltage modulation, thermal characteristics, and distribution of the value. Installation of input capacitor in the position close to the pin in between VIN and GND is recommended also. In addition, the rated voltage of capacitor shall be set with enough margins with respect to input voltage.

4. Filter Capacitor C_{BC}
   Filter capacitor C_{BC} and built-in resistance formed a low pass filter that reduces the noise that appears in output voltage. In addition, the filter capacitor C_{BC} also has a soft start function because it limits the rush current of output when it starts. The rising speed depends on the internal charging current 100µA (Typ), the capacitance value connected to BC and on the output programmed voltage. The time of the soft start is about 9ms (Typ) if capacitance is 1µF and output programmed voltage is -1.0V, and almost 40ms (Typ) if output programmed voltage is set to -5.0V.
   Because the higher value of capacitor will decrease the noise but the soft start time will be longer, it should be decided that the proper value of the capacitance.
   Refer the following calculation for C_{BC} capacitance. Depending on the output capacitor, there is a possibility not to operate properly.

$$C_{BC} \geq \frac{C_{OUT}}{1000} \quad [F]$$

I/O Equivalence Circuits

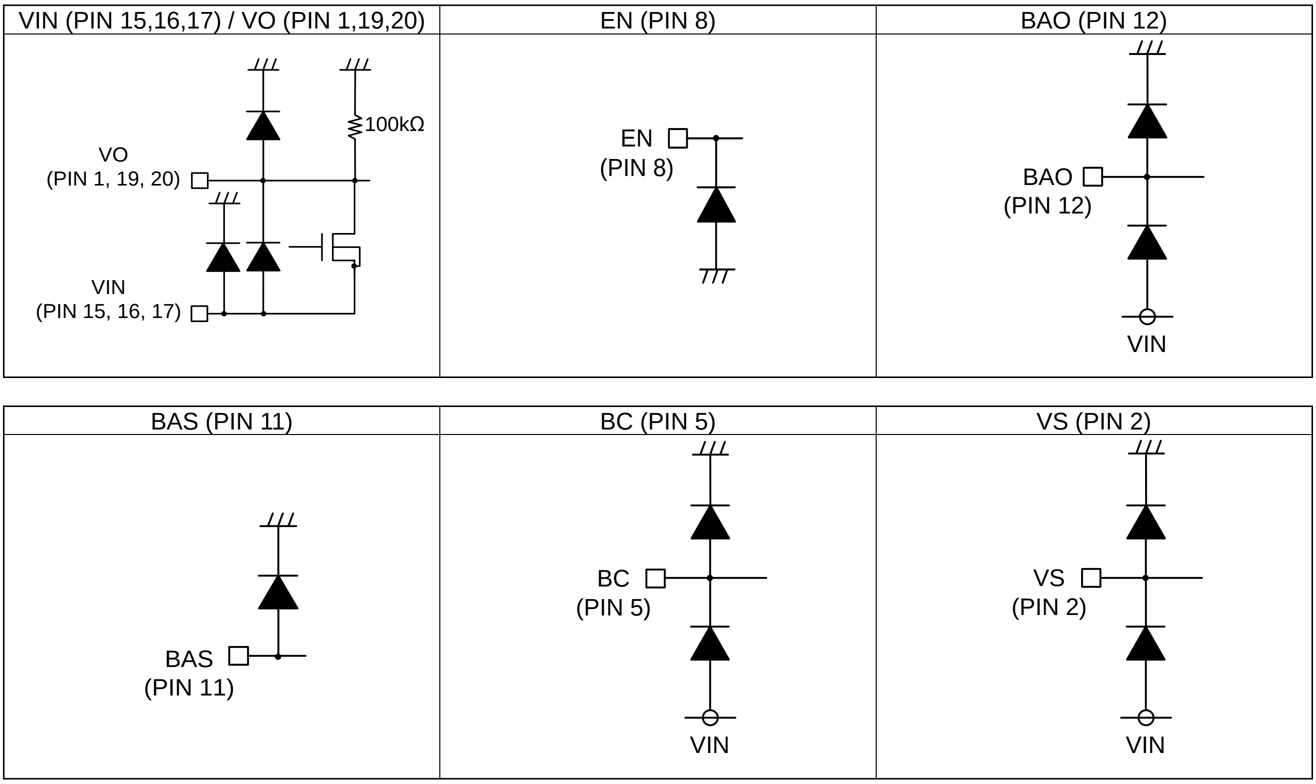
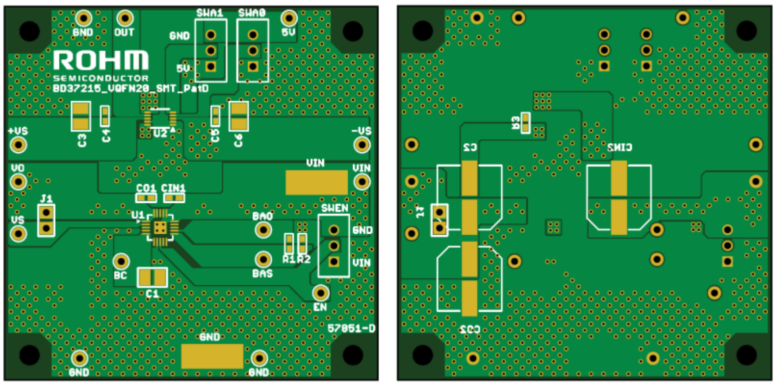


Figure 40. I/O Equivalence Circuits

PCB Layout Example



TOP BOTTOM
(Board Size 60mm x 60mm, Board Thickness 1.6mm, Material FR-4)

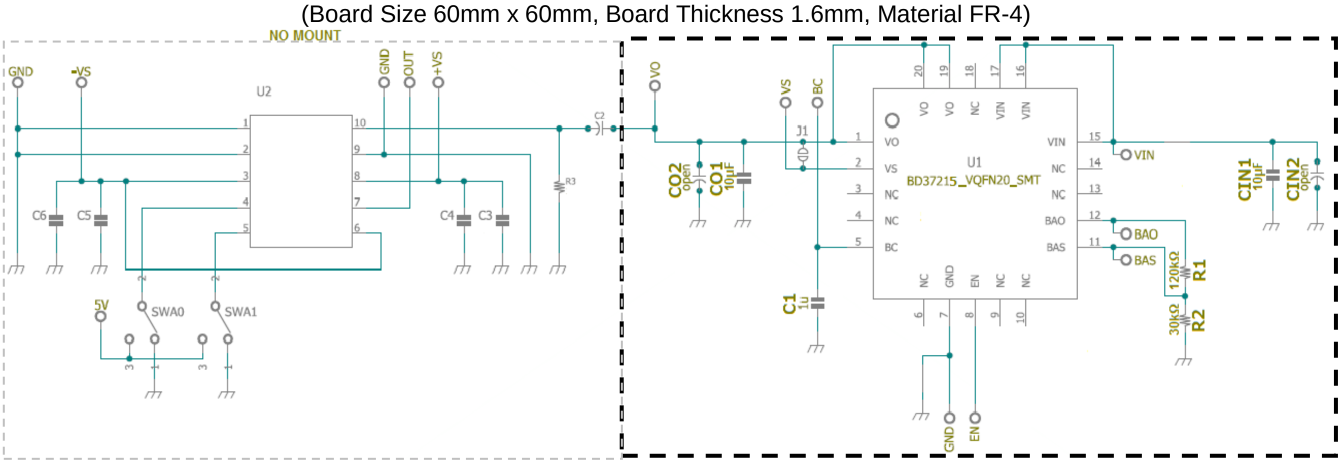


Figure 41. Circuit Diagram of Evaluation Board (Typical Application Circuit setting)

(Note) This PCB Layout example includes the other device pattern also. This IC position is U1.

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for EN pin, ensure that no pins are at a voltage above that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When VIN > Pin A and VIN > Pin B, the P-N junction operates as a parasitic diode.
When VIN > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the VIN voltage to an input pin (and thus to the P substrate) should be avoided.

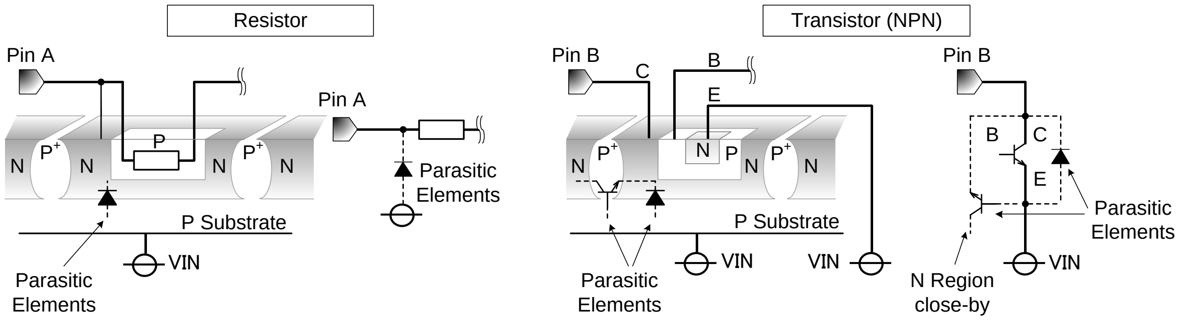


Figure 42. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B	D	3	7	2	1	5	M	U	V	-	E 2

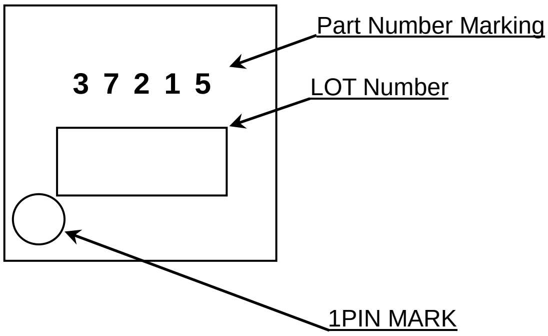
Part Number

Package
MUV:VQFN020V4040

Packaging and forming specification
E2: Embossed tape and reel
(VQFN020V4040)

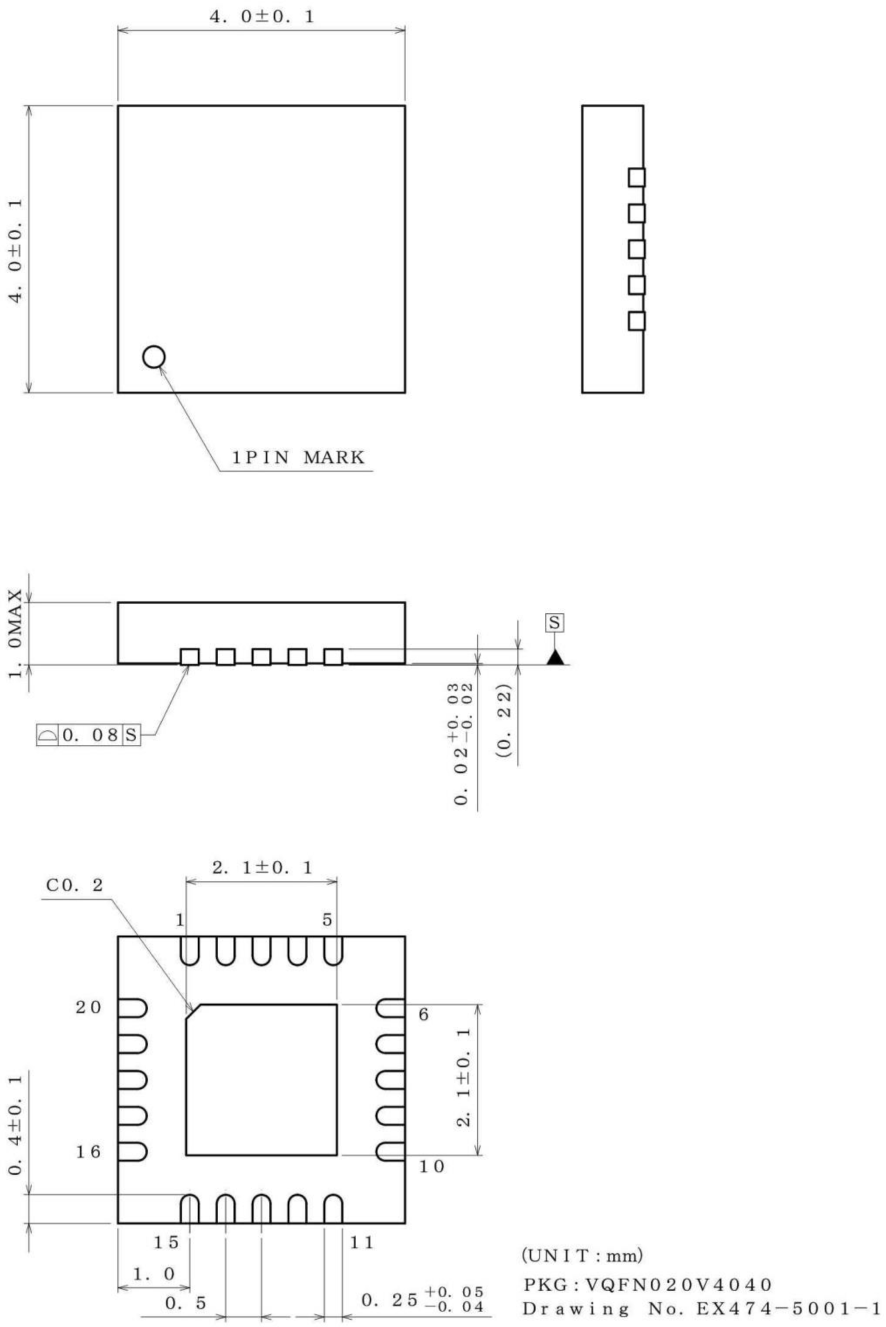
Marking Diagram

VQFN020V4040 (TOP VIEW)



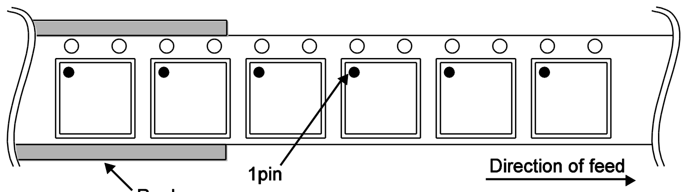
Physical Dimension, Tape and Reel Information

Package Name	VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
02.May.2017	001	New Release
16.Feb.2018	002	Renewed the title Renewed Typical Performance Curves

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BD37215MUV - Web Page

Part Number	BD37215MUV
Package	VQFN020V4040
Unit Quantity	2500
Minimum Package Quantity	2500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes