

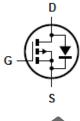


Features

- Voltage Controlled P-Channel Small signal switch
- High Density Cell Design for Low RDS(ON)
- **High Saturation Current**
- Lead Free

Applications

- · Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers





Maximum Ratings

Ratings at 25°C unless otherwise specified.

Parameter	Symbol	Value	Units
Drain-source voltage	VDS	-50	V
Gate-source voltage	Vgso	±20	V
Drain current continuous (Note 1) Pulse	lo	-130 -520	mA
Power dissipation (Note 1)		0.36	W
Derate above 25°C	PD	2.9	mW/°C
Thermal resistance, Junction-to-ambient	Reja	350	°C/W
Operating junction and storage temperature	TJ, Tstg	-55 to +150	°C
Maximum Lead Temperature For Soldering Purposes, 1/16" from case for 10 seconds	TL	300	°C

Note 1 ReJA is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Reuc is guaranteed by design while Reca is determined by the user's board design.

Electrical Characteristics

Ratings at 25°C unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-source breakdown voltage	V(BR)DSS	Vgs=0V, In=-250µA	-50	-	-	V
Breakdown voltage temperature coefficient	ΔV(BR)DSS / ΔTJ	I _D = –250 μA,Referenced to 25°C	-	-48	-	mV/°C
Gate threshold voltage	VGS(th)	V _{DS} =V _{GS} , I _D =-1mA	-0.8	-1.7	-2	V
Gate threshold voltage temperature coefficient	$\Delta V_{GS(th)}/\Delta T_{J}$	I _D = -1mA, Referenced to 25°C	-	3	-	mV/°C
Gate-body leakage	Igss	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero gate voltage drain current	lane	V _{DS} =-50V, V _{GS} =0V	-		-15	μΑ
	loss	V _{DS} =-50V, V _{GS} =0V T _J = 125°C	-	-	-60	μΑ
Drain-source on-resistance	Dagger	V _{GS} = -5V, I _D = -0.1A	-	1.2	10	
	RDS(ON)	V _{GS} = -5V, I _D = -0.1A, T _J =125°C	-	1.9	17	Ω





Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
On-state drain current	I _{D(on)}	V _{GS} =-5V, V _{DS} =-10V	-0.6	-	-	Α
Forwards transfer admittance	yfs	V _{DS} =-25V, I _D =-0.1A	0.05	0.6	-	S
Input capacitance	Ciss		-	73	-	
Output capacitance	Coss	V _{DS} =-25V, V _{GS} =0V, f=1MHz	-	10	-	pF
Reverse transfer capacitance	Crss		-	5	-	
Gate resistance	Rg	V _{GS} =-15mV, f=1MHz	-	9	-	Ω
Turn-on delay time	td(on)	Vdd=-30V, Id=-0.27A, Vgs=-10V, Rgen=6Ω	-	2.5	5	
Turn-on rise time	tr		-	6.3	13	20
Turn-off delay time	tD(OFF)		-	10	20	ns
Turn-off fall time	tf		-	4.8	9.6	
Total gate charge	Qg		-	0.9	1.3	
Gate-source charge	Qgs	V _{DS} =-25V, I _D =-0.1A, V _{GS} =-5 V	-	0.2	-	nC
Gate-drain charge	Qgd]	-	0.3	-	
Maximum continuous drain-source diode forward current	Is	-	-	-	-0.13	А
Drain-source diode forward voltage	VsD	V _{GS} =0V, I _S =-0.26A (Note 2)		-0.8	-1.4	V
Diode reverse recovery time	trr	I==-0.1A		10	-	nS
Diode reverse recovery charge	Qrr	di⊧/dt =100A/µs (Note 2)	-	3	-	nC

Note 2 Pulse Test: Pulse Width δ300us, Duty Cycle ≤2%.

Typical Characteristics:

TA = 25°C unless otherwise specified

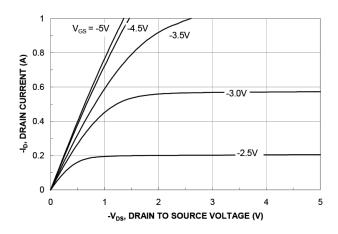


Figure 1. On-Region Characteristics.

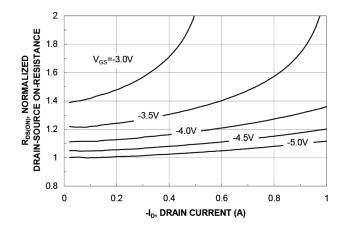
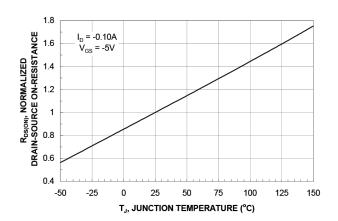


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



P-Channel MOSFET Transistor



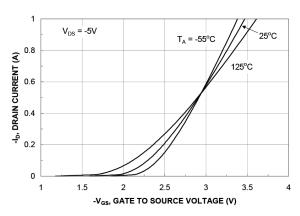


T_A = 125°C

T_A = 25°C

Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



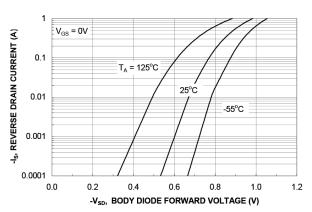
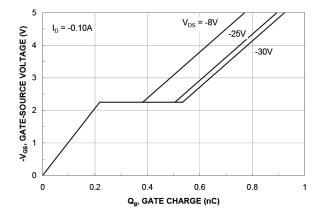


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



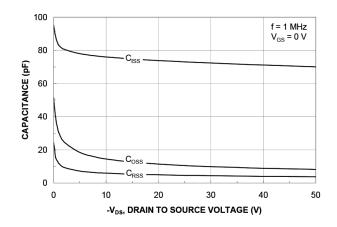


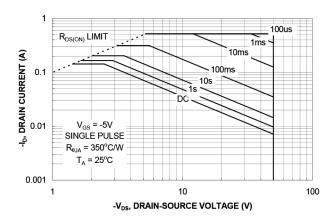
Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



P-Channel MOSFET Transistor multicomp





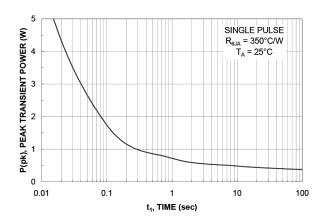


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

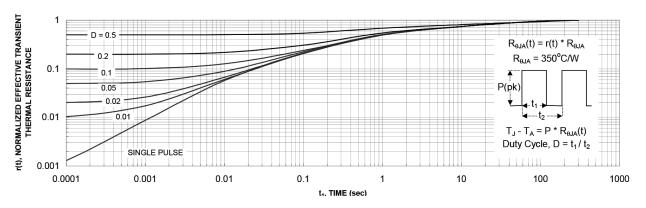


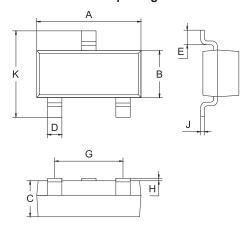
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1a.

Transient thermal response will change depending on the circuit board design.

Package Outline:

Plastic surface mounted package



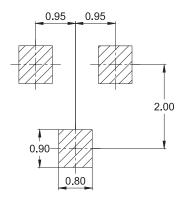
SOT-23				
Dim.	Min. Max.			
А	2.7	3.1		
В	1.1	1.5		
С	1 Typ.			
D	0.4 Typ.			
Е	0.35	0.48		
G	1.8	2		
Н	0.02	0.1		
J	0.1 Typ.			
K	2.2	2.6		

Dimensions: Millimetres





Soldering Footprint:



Package Information:

Device	Package	Shipping	Marking Code
BSS84-7-F	SOT-23	3,000 / Tape & Reel	SP

Dimensions: Millimetres

Part Number Table

Description	Part Number	
MOSFET Transistor, P-Channel, -130mA, -50V, 1.2Ω, -5V, -1.7V	BSS84-7-F	

Important Notice: This data sheet and its contents (the "Information") belong to the members of the Premier Farnell group of companies (the "Group") or are licensed to it. No licence is granted for the use of it other than for information purposes in connection with the products to which it relates. No licence of any intellectual property rights is granted. The Information is subject to change without notice and replaces all data sheets previously supplied. The Information supplied is believed to be accurate but the Group assumes no responsibility for its accuracy or completeness, any error in or omission from it or for any use made of it. Users of this data sheet should check for themselves the Information and the suitability of the products for their purpose and not make any assumptions based on information included or omitted. Liability for loss or damage resulting from any reliance on the Information or use of it (including liability resulting from negligence or where the Group was aware of the possibility of such loss or damage arising) is excluded. This will not operate to limit or restrict the Group's liability for death or personal injury resulting from its negligence. Multicomp is the registered trademark of the Group. © Premier Farnell Limited 2016.

