Vishay Siliconix

P-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY	
V _{DS} (V)	-40
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.0120
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0175
Q _g typ. (nC)	74.3
I _D (A)	42 ^d
Configuration	Single

FEATURES

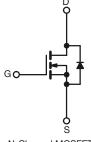
- TrenchFET® Gen IV p-channel power MOSFET
- Maximum 175 °C junction temperature
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912



ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

- Motor drive control
- LED backlighting
- · Load switch
- Industrial



MOSFET

ORDERING INFORMATION				
Package	TO-252			
Lead (Pb)-free and halogen-free	SUD40151EL-GE3			

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	40	
Gate-source voltage		V _{GS}	± 20	V
Continuous drain current	T _C = 25 °C		42 ^d	
	T _C = 125 °C	I _D	28.6	
Pulsed drain current (t = 100 μs)		I _{DM}	100	A
Continuous source-drain diode current		I _S	41.7	
Single pulse avalanche current ^a	L = 0.1 mH	I _{AS}	25	
Single pulse avalanche energy a	L = 0.1 mn	E _{AS}	31.25	mJ
Maximum power dissipation	T _C = 25 °C		50 b	w
	T _C = 125 °C	P _D	16.7 b	VV
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) c			260	-0

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	MAXIMUM	UNIT	
Maximum junction-to-ambient (PCB mount) c		R _{thJA}	60	°C/W	
Maximum junction-to-case (drain)	Steady state	R _{thJC}	3		

Notes

- a. Duty cycle ≤ 1 %
- b. See SOA curve for voltage derating
- c. When mounted on 1" square PCB (FR4 material)
- d. Package limited



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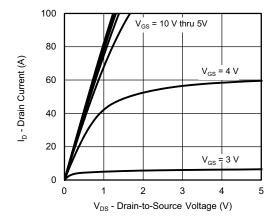
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40	-	-	V	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.5	=	2.5	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	250	nA	
Zero gate voltage drain current		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1		
	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 125 °C	V, T _J = 125 °C 150		150	μA	
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 175 °C	-	-	5	mA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	Α	
Drain-source on-state resistance ^a	_	V _{GS} = 10 V, I _D = 17.5 A	-	0.0100	0.0120	Ω	
	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 14.5 A	-	0.0135	0.0175		
Forward transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 17.5 \text{ A}$	-	70	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	5340	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	335	-		
Reverse transfer capacitance	C _{rss}		-	303	-		
Total gate charge	Qg		-	74.3	112	nC	
Gate-source charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 17.5 \text{ A}$	-	12.7	-		
Gate-drain charge	Q_{gd}		-	11.1	-		
Gate resistance	R_{g}	f = 1 MHz	0.86	4.3	8.6	Ω	
Turn-on delay time	t _{d(on)}		-	15	30		
Rise time	t _r	V_{DD} = 20 V, R_L = 1.4 Ω , $I_D \cong$ 14 A,	-	10	20	nc	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	75	113	ns	
Fall time	t _f		-	75	113		
Drain-Source Body Diode Characteristi	cs						
Pulse diode forward current (t = 100 μs)	I _{SM}		-	-	42	Α	
Body diode voltage	V_{SD}	$I_F = 14 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.85	1.5	٧	
Body diode reverse recovery time	t _{rr}		-	30	45	ns	
Body diode reverse recovery charge	Q _{rr}	$I_F = 14 \text{ A, di/dt} = 100 \text{ A/µs}$	-	0.02	0.04	μC	
Reverse recovery fall time	t _a	i _F = 14 A, αι/αι = 100 A/μS	-	15.3	-		
Reverse recovery rise time	t _b		-	14.7	-	ns	
Body diode peak reverse recovery charge	I _{RM(REC)}		-	-	2.8	Α	

Notes

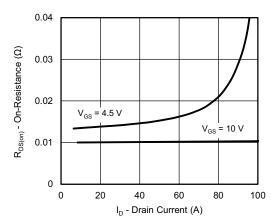
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

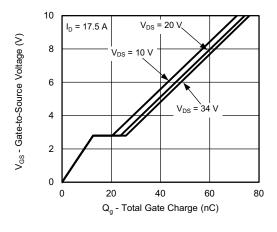




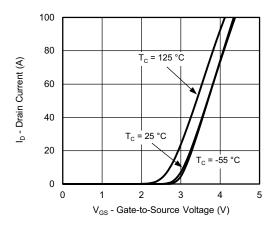
Output Characteristics



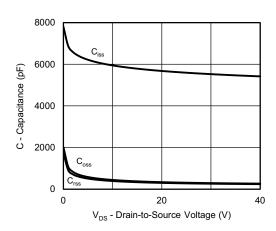
On-Resistance vs. Drain Current and Gate Voltage



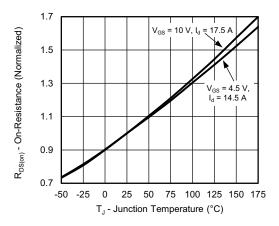
Gate Charge



Transfer Characteristics

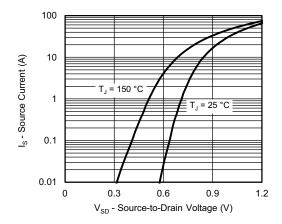


Capacitance

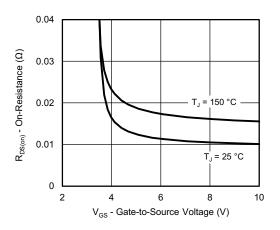


On-Resistance vs. Junction Temperature

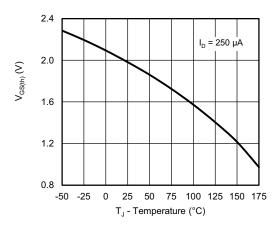




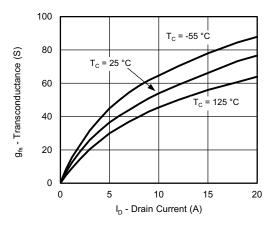
Source-Drain Diode Forward Voltage



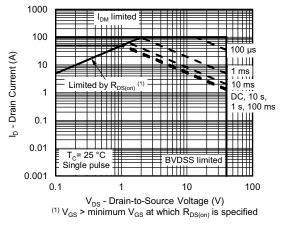
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

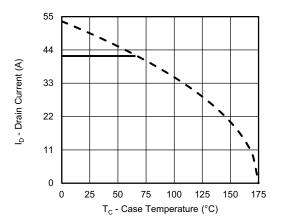


Transconductance

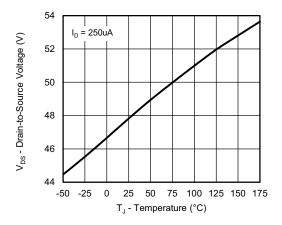


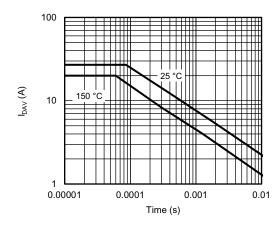
Safe Operating Area, Junction-to-Ambient





Current Derating a





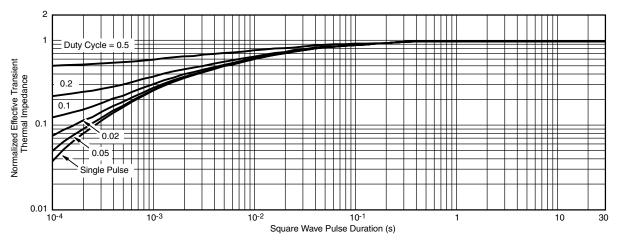
Drain Source Breakdown vs. Junction Temperature

I_{DAV} vs. Time

Note

a. The power dissipation P_D is based on T_J max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75668.



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