

## Battery Disconnect Switch

### FEATURES

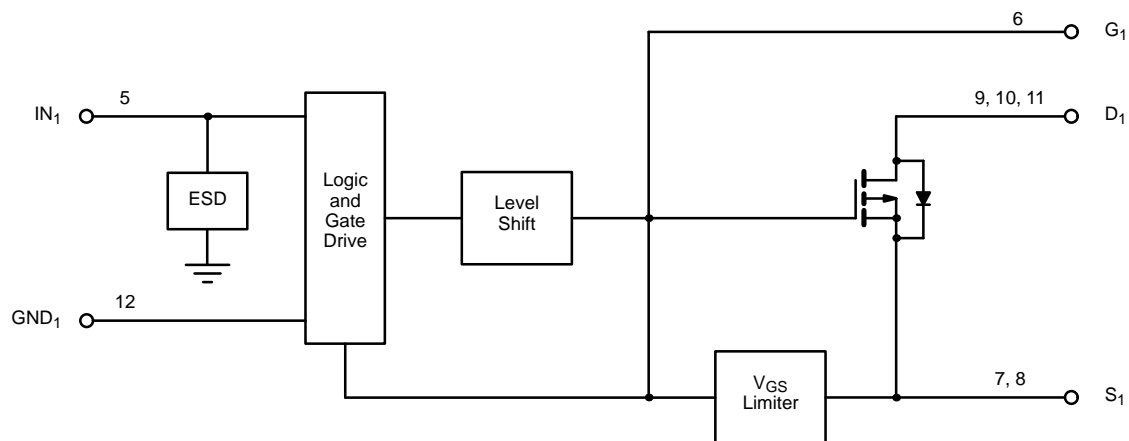
- Solution for Bi-Directional Blocking  
Bi-Directional Conduction Switch
- 6- to 30-V Operation
- Ground Referenced Logic Level Inputs
- Integrated Low  $r_{DS(on)}$  MOSFET
- Level-Shifted Gate Drive with Internal MOSFET
- Two Independent Inputs
- Ultra Low Power Consumption in Off State  
(Leakage Current Only)
- Logic Supply Voltage is Not Required

### DESCRIPTION

The Si4720CY is two level-shifted p-channel MOSFETs. Operating together, these MOSFETs can be used as a reverse blocking switch for battery disconnect applications. It is a solution for multiple battery technology designs or designs that require isolation from the power bus during charging.

The Si4720CY is available in a 16-pin SOIC package and is rated for the commercial temperature range of  $-25$  to  $85^{\circ}\text{C}$ .

### FUNCTIONAL BLOCK DIAGRAM



Half a circuit shown here.



**ABSOLUTE MAXIMUM RATINGS**

Voltage Referenced to GND  
 $V_S, V_D^a$  ..... -0.3 V to 32 V  
 $V_{SD}$  ..... -0.3 V to 30 V  
 $V_{IN1}, V_{IN2}$  ..... -0.3 V to 15 V  
 $V_{GS}$  ..... 20 V

Storage Temperature ..... -55 to 150°C  
 Power Dissipation<sup>b</sup> (t = 10 sec) ..... 2.5 W  
 (t = steady state) ..... 1.5 W

Notes  
 a.  $V_{SD} \leq 30 V_{DC}$   
 b. Device mounted with all leads soldered to 1" x 1" FR4 with laminated copper PC board.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**RECOMMENDED OPERATING RANGE**

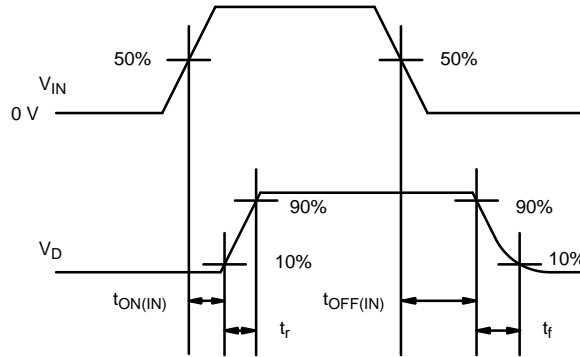
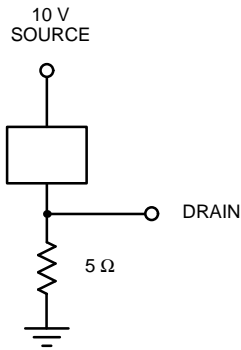
$V_S, V_D$  ..... 6 V to 30 V  
 $V_{IN1}, V_{IN2}$  ..... 0 V to 13.2 V  
 $I_{DS}$  ..... 0 A to 6 A

Operating Temperature Range ..... -25 to 85°C  
 Junction Temperature ..... -25 to 150°C

<b>SPECIFICATIONS</b>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified	Limits				Unit
			Temp <sup>a</sup>	Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
On-Resistance	$r_{DS}$	$V_S = 10 V, I_D = 1 A, V_{IN} = H$	Room		0.0155	0.020	$\Omega$
Leakage Current	$I_{DS(off)}$	$V_{DS} = 10 V$	Room			1	$\mu A$
Supply Current	$I_{S(off)}$	$V_S = 21 V$	Room			1	
	$I_{S(on)}$		Room		1.1	6	
Input Voltage Low	$V_{INL}$	$V_S = 10 V$ and $V_S = 21 V$	Full			1	V
Input Voltage High	$V_{INH}$		Full	2.5			
Input Leakage Current	$I_{INH}$	$V_{IN} = 5.0 V$	Full			5	$\mu A$
Turn-On Delay	IN to D or S	$V_S = 10 V, R_L = 5 \Omega, \text{Figure 1}$	Room	2.2	2.9	10	$\mu s$
Turn-Off Delay			Room		1.5	2.1	
Break-Before-Make <sup>d</sup>	$t_{BBM}$		Room		1.05		
Rise Time	$t_{RISE}$	$V_S = 10 V, R_L = 5 \Omega, \text{Figure 1}$	Room		1.3	2.5	ns
Fall Time	$t_{FALL}$		Room		50	100	
Voltage Across Pin 6 and 7	$V_{GS}$	$V_S = 30 V$	Room		10.2	18	V
Forward Diode	$V_{SD}$	$I_D = -1 A$	Room			1.1	

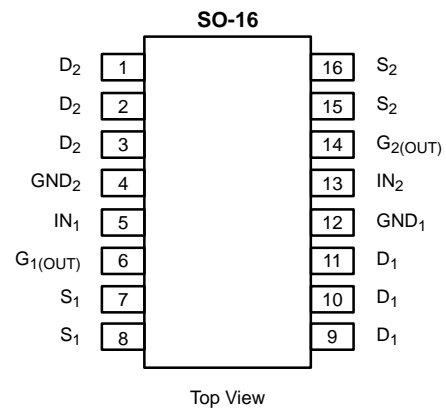
Notes  
 a. Room = 25°C, Full = as determined by the operating temperature suffix.  
 b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.  
 c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.  
 d. Guaranteed by design, not subject to production testing.

**TIMING DIAGRAMS**



**FIGURE 1.**

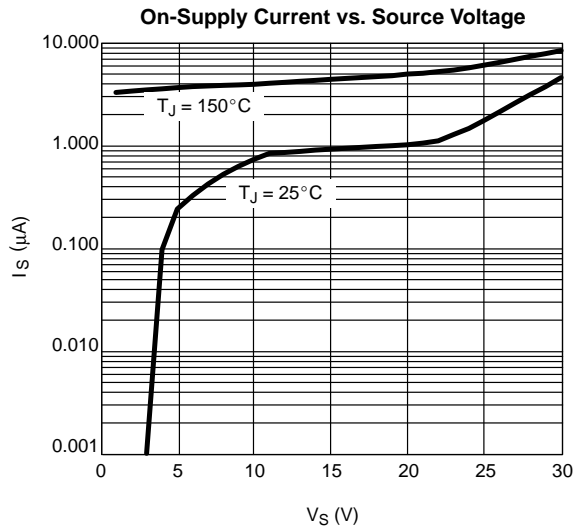
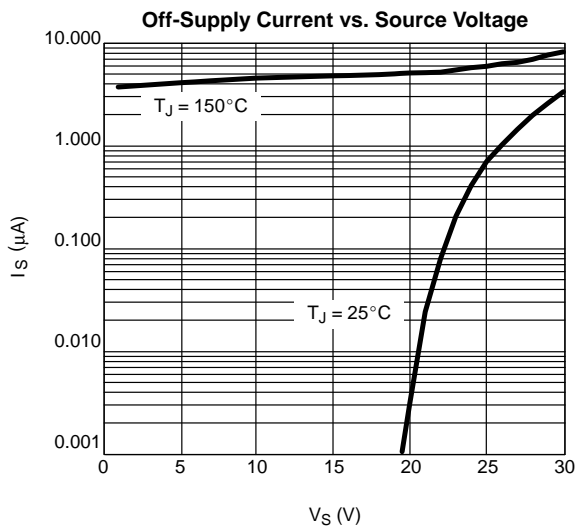
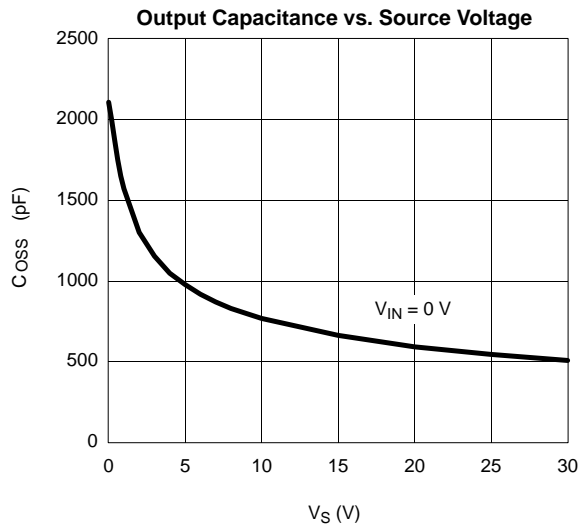
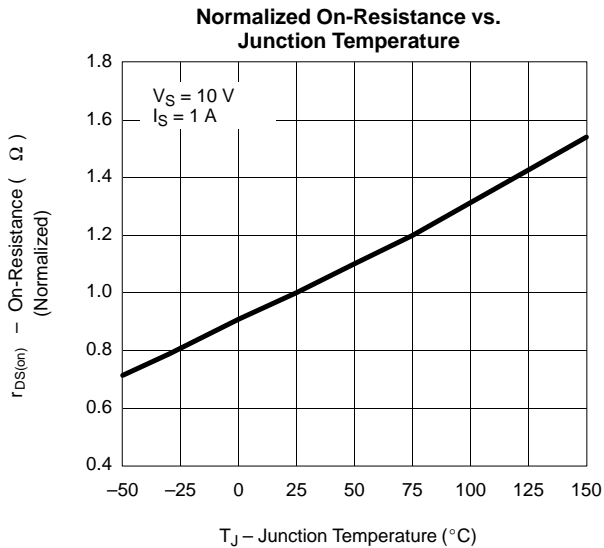
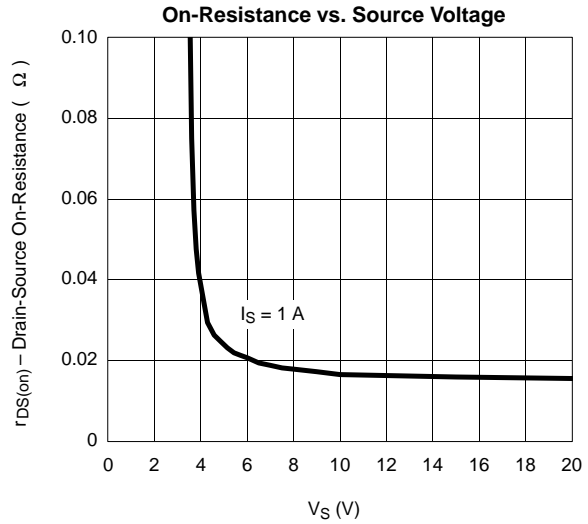
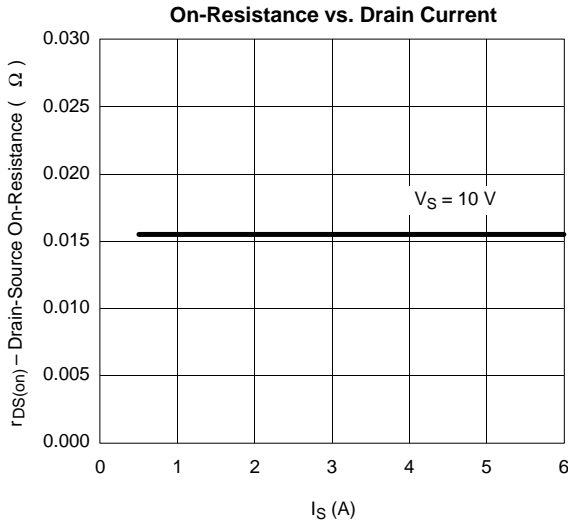
<b>PIN CONFIGURATION AND TRUTH TABLE</b>			
$V_{IN1}$	$V_{IN2}$	Switch 1	Switch 2
0	0	Off	Off
0	1	Off	On
1	0	On	Off
1	1	On	On



Order Number: Si4720CY

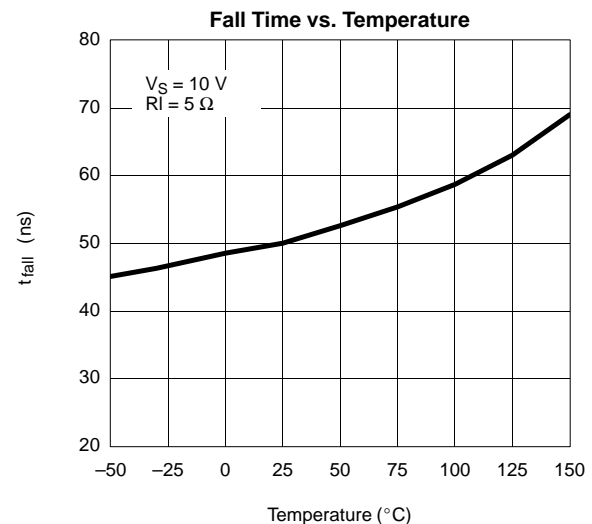
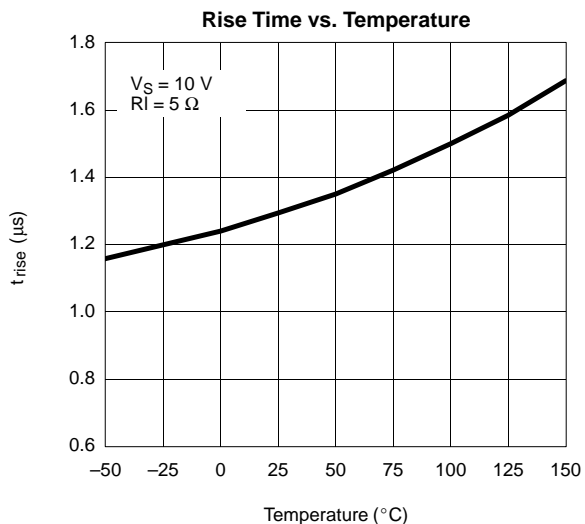
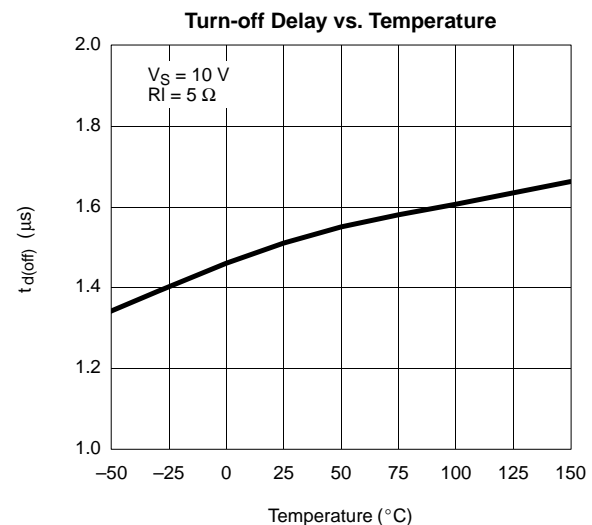
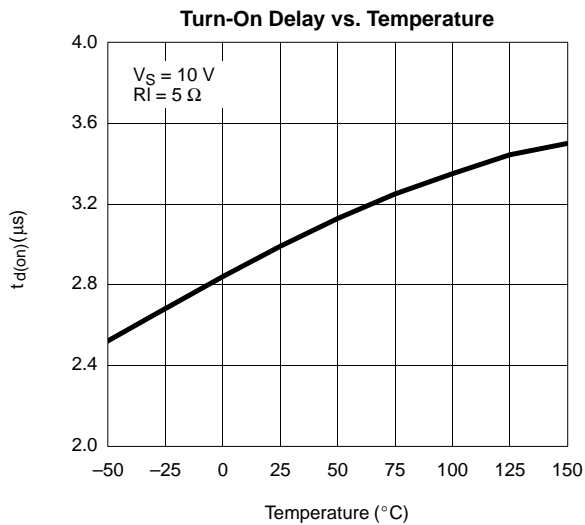
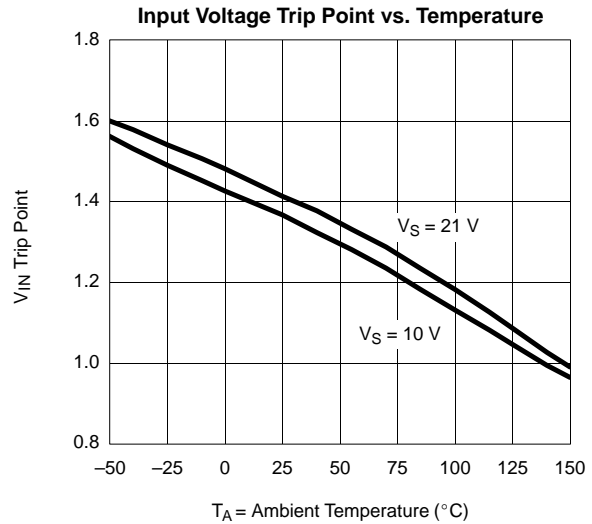
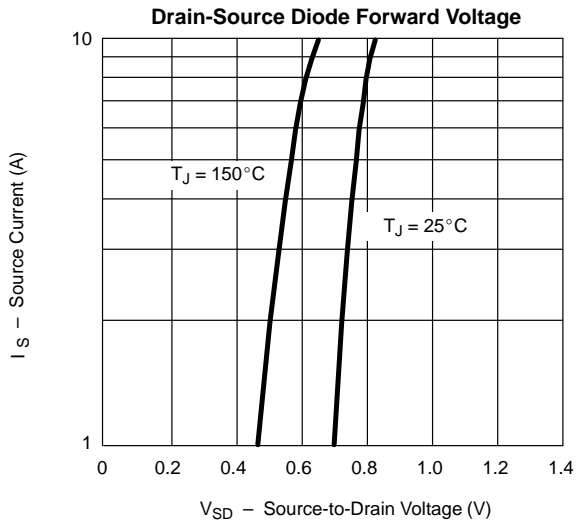
<b>PIN DESCRIPTION (SUBJECT TO CHANGE)</b>		
Pin Number	Symbol	Description
1, 2, 3	$D_2$	Drain connection for MOSFET-2.
4, 12	GND	Ground
5	$IN_1$	Logic input, $IN_1$ . High level turns on the switch.
6	$G_{1(OUT)}$	Gate output to MOSFET-1.
7, 8	$S_1$	Source connection for MOSFET-1
9, 10, 11	$D_1$	Drain connection for MOSFET-1.
13	$IN_2$	Logic input, $IN_2$ . High level turns on the switch.
14	$G_{2(OUT)}$	Gate output to MOSFET-2.
15, 16	$S_2$	Source connection for MOSFET-2.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

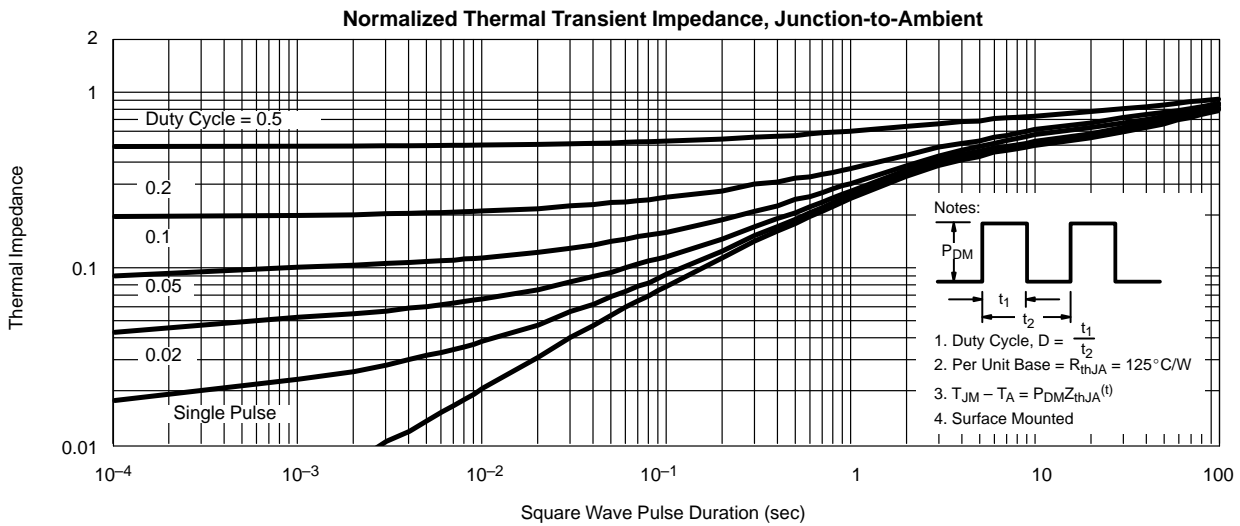
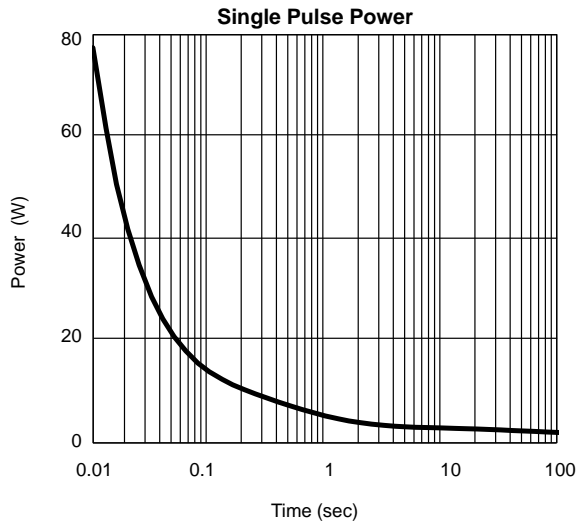




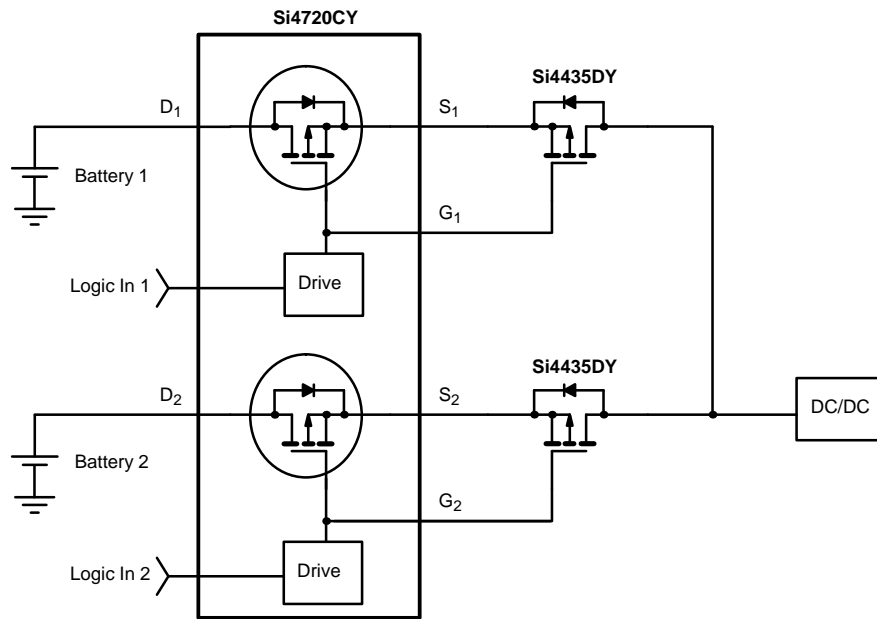
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



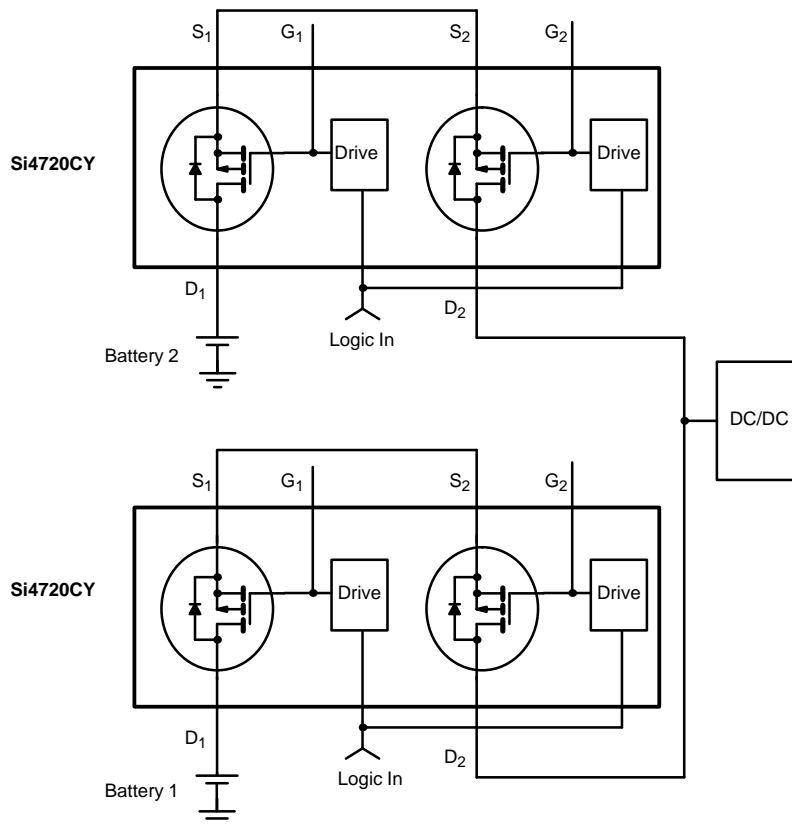
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**APPLICATION DRAWINGS**

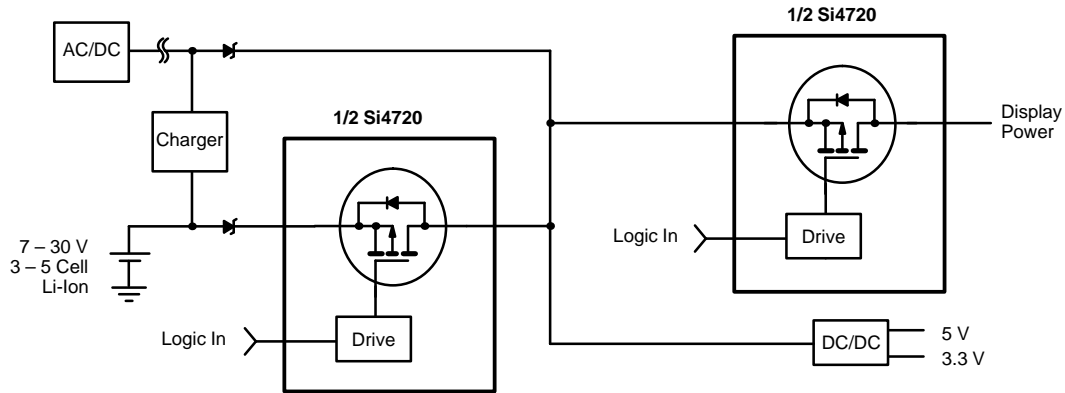


**FIGURE 2.**

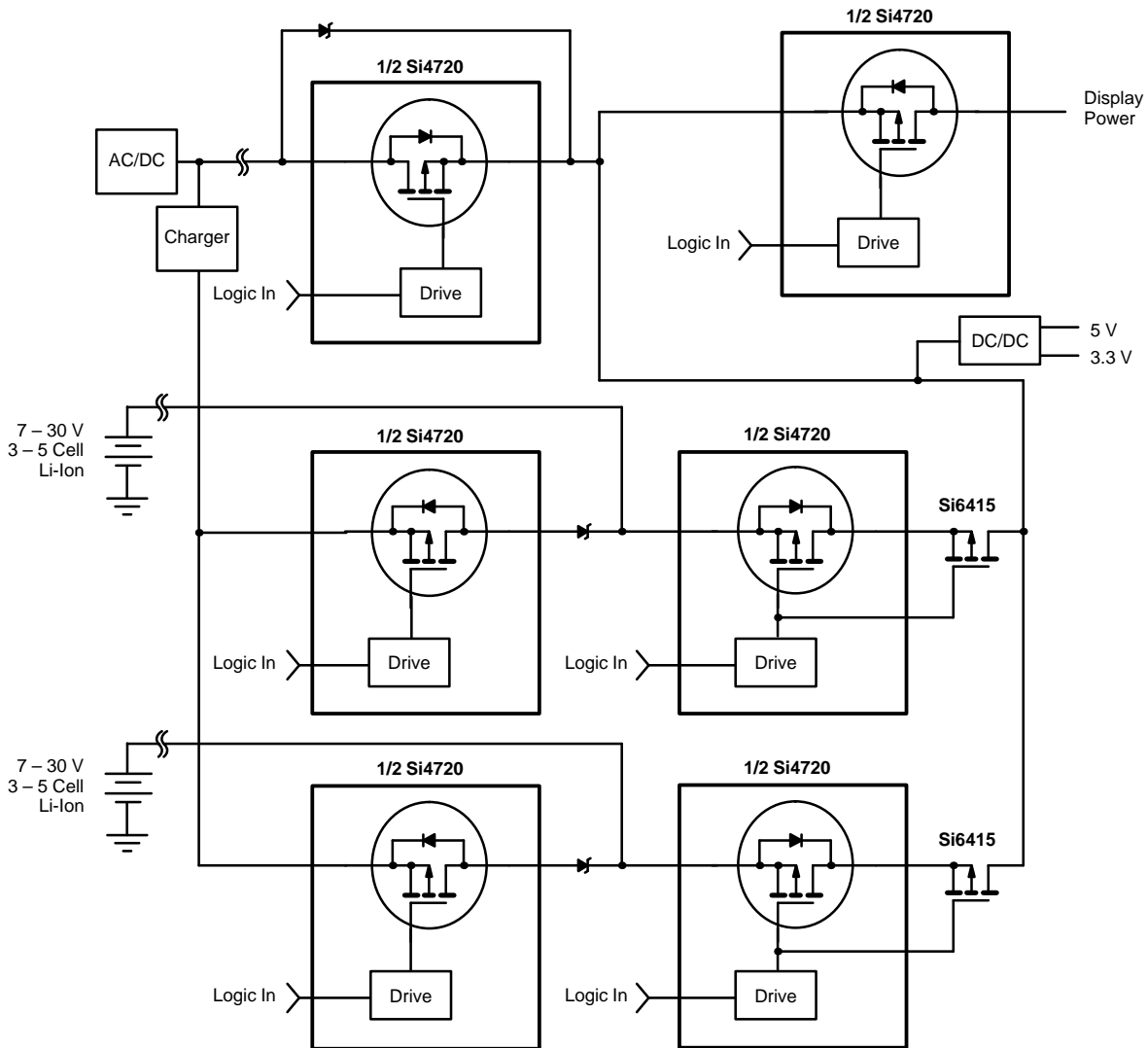


**FIGURE 3.**

**APPLICATION DRAWINGS**



**FIGURE 4.** Low-Cost Laptop PC



**FIGURE 5.** High-Performance Laptop PC





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