



Product Change Notification - SYST-03HLJN826 (convert To PDF)

Date:

10 Apr 2018

Product Category:

32-bit PIC Microcontrollers

Affected CPNs:



Notification subject:

Data Sheet - PIC32MK Motor Control & General Purpose Family Datasheet

Notification text:

SYST-03HLJN826

Microchip has released a new DeviceDoc for the PIC32MK Motor Control & General Purpose Family Datasheet of devices. If you are using one of these devices please read the document located at PIC32MK Motor Control & General Purpose Family Datasheet.

Notification Status: Final

Description of Change:

- 1) 32-bit General Purpose and Motor Control Application MCUs with FPU and up to 1 MB LiveUpdate Flash, 256 KB SRAM, 4 KB EEPROM, and Op amps; The 120 MHz Operating Conditions were updated. Secure boot was removed from the Security Features. The FRC internal oscillator Clock Management operating conditions were updated. The number of ADC channels for 64-pin TQFP and QFN Motor Control devices was
- 2) 1.0 "Device Overview": The I2Cx and PLVD references were removed from the PIC32MK GP/MC Family
- Block Diagram (see Figure 1-1).
 3) 5.0 "Flash Program Memory": The Wait state bits, LPRDWS<_x0034_:_x0030_> (NVMCON2), were updated to include a table with low-power Wait state information (see Register 5-8)
- 4) 10.0 "Prefetch Module": The Wait states table in the PFMWS<_x0032_:_x0030_> bits (CHECON< x0032 : x0030 >) was updated (see Register 10-1)
- 5) 11.0 "Direct Memory Access (DMA) Controller"; A note was added to the CHSIRQ < x0037 : x0030 > bits (DCHxECON<_x0031_5:_x0038_>) (see Register 11-8).
- 6) 14.0 "Timer1": The Timer1 Block Diagram was updated (see Figure 14-1).
- 7) 15.0 "Timer2: Through Timer9" The Timer2-Timer9 Block Diagram was updated (see Figure 15-1).
- 8) 25.0 "12-bit High-Speed Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC)": The Step 7 was updated (see 25.1 "Activation Sequence"). Table 25-1: "PIC32MKXXX Based on a 60 MHz TAD clock (16.667 ns)" was updated. IVTEMP references were removed from the: • ADC Block Diagram (see Figure 25-1) • S&H Block Diagram (see Figure 25-2) • ADC Register Map (see Table 25-2) The ADCDATA51 register was removed (see Table 25-2). The ADCCON2 register was updated (see Register 25-12). The following bits were removed: • CSS51 (see Table 25-2 and Register 25-12) • ARDY51 (see Table 25-2 and Register 25-14) • EIRDY51 (see Table 25-2 and Register 25-37) • AN51 (see Table 25-2 and Register 25-41) The definition for bit value '110011' in the ADINSEL<_x0035_:_x0030_> bits in the ADC Control Register 3 was updated to Reserved (see Register 25-3). A Note was added to the TRGSRC3<_x0034_:_x0030_> bits in the ADC Trigger Source x Registers (see Register 25-18 through Register 25-24). The definition for bit value '110101' in the AINID<_x0035_:_x0030_> bits in the ADC Digital Comparator 1 Control Register 3 was updated to Reserved (see Register 25-25). The definition for the LVL27:LVL0 bits in the ADC Trigger Level/Edge Sensitivity Register was updated (see Register 25-32)

- 9) 27.0 "Op Amp/Comparator Module": The Digital Filter Interconnect Block Diagram was updated (see Figure 27-7). The PSIDL bit was renamed SIDL, and the C5EVT-C1EVT bits were removed in the register summary (see Table 27-2). The bit value '010' definition was updated to from Reserved to PWM Secondary Special Event in the CFSEL<_x0032_:_x0030_> bits of the Op amp/Comparator 'x' Control Register (see Register 27-2).
- 10) 28.0 "Charge Time Measurement Unit (CTMU)": The bit value definitions were updated in the IRNG<_x0031_:_x0030_> bits of the CTMU Control Register and Notes 5 and 6 were added (see Register
- 11) 32.0 "Power-Saving Features" :The All Resets value in the register summary for bits 15:0 of the PMD2 register was changed to '0000' (see Table 32-2).
- 12) 36.0 "Electrical Characteristics": The Maximum value of the Power-Down Current DC Characteristics parameter DC41 was updated (see Table 36-8). The Minimum value of the Internal LPRC Accuracy for parameter F21 was updated (see Table 36-18). The Temperature Sensor Specifications were removed (was Table 36-43). Parameter AD51 in the Analog-to-Digital Conversion Timing Requirements was updated (see Table 36-40). The CTMU Current Source Specification conditions were updated (see Table 36-43). 13) 37.0 "AC and DC Characteristics Graphs": The Typical CTMU Temperature Sensor Voltage graph was removed (was Figure 37-5).

Impacts to Data Sheet: None

Reason for Change: To Improve Manufacturability

Change Implementation Status: Complete

Date Document Changes Effective: 10 Apr 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC32MK Motor Control & General Purpose Family Datasheet

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